SIEMENS

ICs for Industrial Electronics

Data Book 1985/86

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HKZ 101	Q67000-S64	Hall-effect vane switch	546
HKZ 101 S	Q67000-S64-E10	Hall-effect vane switch	546
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S 187 C	Q67100-Y868	Digital frequency synthesizer	478
S 353	Q67000-R109	Programmable diode matrix	487
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▼S 360 B 114	Q67000-Y555-V114	Universal programmable counter with signal edge evaluation circuit	592
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SAB 4209	Q67100-Y460	Infrared remote control system – receiver (4 analog functions)	422
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■SAS 241	Q67000-S50	Magnetically operated, contactless switch with dynamic outputs	537
■SAS 241 S4	Q67000-S50-S4	Magnetically operated, contactless switch with dynamic outputs	537

▼ New type
■ Not for new design

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▼ SDA 5200 N	Q67000-A2242	6 bit analog/digital converter	369
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S 360 B 110; C	Triple 16 bit up/down counter with 8 bit data bus	582
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S 1531 G	AF amplifier for 1 V	605
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General Information

2.1 Type-designation code for ICs

IC type designations are based on the European Pro Electron system. The code system is explained in the Pro Electron brochure D 15*), edition 1982.

*) Available from Pro Electron, Boulevard de Waterloo 103,
1000 Brussels, Belgium.

2.2 Mounting instructions

2.2.1 Plastic plug-in package with 4, 6, 8, 14, 16, 18, 20, 22, 24, 28, 36, 40, or 48 pins

The pins of the cases are bent downwards by an angle of 90° and fit into holes with a diameter of between 0.7 and 0.9 mm spaced 2.54 mm apart. The dimension x is given in the corresponding drawing.

The bottom of the package will not touch the PC board after insertion because the pins have shoulders just below the package (see figure 1).

After insertion of the package into the PC board it is advisable to bend the ends of two pins at an angle of approx. 30° to the board so that the package does not have to be pressed down during soldering. Plastic plug-in packages are soldered on that side of the PCB facing away from the package.

The maximum permissible soldering temperature is 265 °C (max. 10 s) for manual soldering and 240 °C (max. 4 s) for dip soldering.

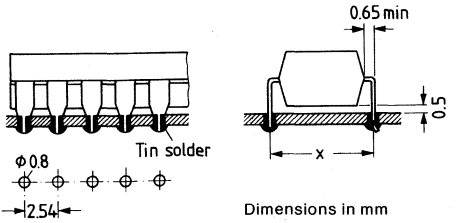


Figure 1

2.2.2 Power plug-in package with 5, 7, or 9 pins

Power packages generally have wider pins than stated in paragraph 2.2.1, meaning that the hole diameter on the PCB must be between 1.1 and 1.8 mm. If the pins are bent, there should be no stress between the pins and the package. The minimum distance between the package and the bending point is 2 mm.

Refer to paragraph 2.2.1 for soldering temperatures.

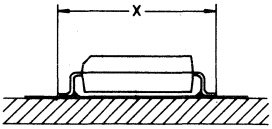
2.2.3 Miniature plastic package with 6, 8, 14, or 20 pins

The pins of the miniature packages are prepared for surface mounting. If the pins are bent, there should be no stress between the pins and the package. The minimum distance between the package and the bending point is 0.4 mm; the bending radius is 0.5 mm.

Iron soldering: soldering temperature 245 °C for max. 10 s;
minimum distance between package and soldering point 1.5 mm;
package temperature max. 150 °C;
no mechanical stress on the pins

Dip soldering: soldering temperature 245 °C for max. 4 s

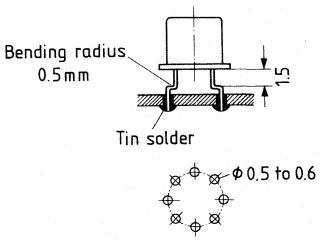
Flow soldering: no mechanical stress on the pins;
minimum distance between package and soldering point 1.5 mm;
package temperature max. 150 °C



2.2.4 5 H 8 DIN 41 873 and similar packages

The package may be mounted in any position. The ends of the pins may be kinked up to a distance of 1.5 mm from the bottom of the package to suit the hole spacing (fig. 2). Pins that are too long should be clipped before soldering. Iron or dip soldering may be employed.

Maximum soldering duration for dip soldering at 250 °C bath temperature t_{max} = 5 s
at 300 °C bath temperature t_{max} = 4 s
for iron soldering at 250 °C iron temperature t_{max} = 15 s
at 300 °C iron temperature t_{max} = 12 s
at 350 °C iron temperature t_{max} = 8 s
(does not apply to MOS components)



Dimensions in mm

Figure 2

2.2.5 Other points to note

Ensure that no current is able to flow between the solder bath or soldering iron and the PCB. It is advisable to ground the pins that are to be soldered as well as the solder bath or soldering iron.

When they are being prepared and inserted in a PCB, circuits should be protected against static charging. Under no circumstances may the components be removed or inserted whilst the operating voltage is switched on.

The increase in chip temperature during the soldering process results in a temporary increase in electrostatic sensitivity of integrated circuits. Special precautions should therefore be taken against line transients, e.g. through the switching of inductances on magnetic chutes, etc.

2.2.6 MICROPACK

MICROPACK components are delivered on film reels.

Mounting suggestions

a) For prototypes and small quantities (up to approximately 50.0 items/y) we suggest hot-table soldering (figure 3).

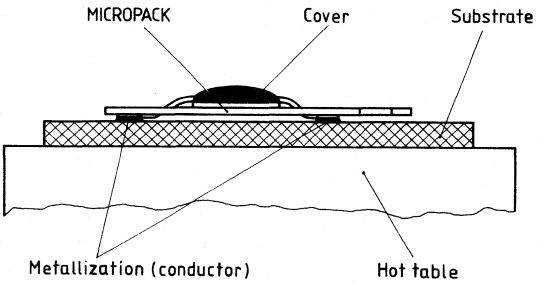


Figure 3

Required equipment and accessories

- cutting device
- hot table, temperature regulated (e.g. Weld-Equip, Unitek)
- stereo microscope (e.g. Wild, Zeiss, magnification 6 · · · 40 times)
- substrate material: epoxy resin; hard paper; ceramic (thick thin film)

Soldering data

- soldering temperature: 210 °C max.
- solder coating on substrate: Pb/Sn (e.g. 60/40) wave-tinned or electrodeposited
- soldering time: approx. 10 s
- flux: e.g. colophony, dissolved in alcohol
- cleaning agents (as required): e.g. Freon TP-35, TE, TF

b) For large quantities (e.g. more than 50.0 items/y) we recommend bar soldering (figure 4).

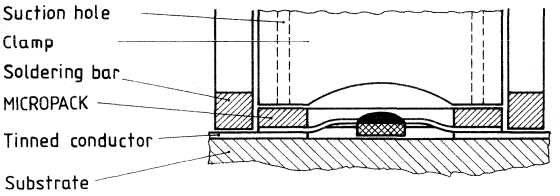


Figure 4

Required equipment

- soldering equipment (e.g. Weld-Equip, Farco, Jade)
- substrate material: epoxy resin; hard paper; flexible materials, e.g. polyamide

Soldering data

- soldering temperature: 210 °C max.
- solder coating on the substrate: Pb/Sn (e.g. 60/40), wave-tinned or electro-deposited
- soldering time: approx. 2 s
- flux: e.g. colophony dissolved in alcohol
- cleaning agents (as required): e.g. Freon TP-35, TE, TF

2.2.7 Permissible power dissipation at T_{amb} = 0 °C to 70 °C

Substrate material	P_{tot} mW	$R_{th\,SA}$ K/W
Epoxy resin/hard paper (chip not fastened)	300	270
Ceramics (chip not fastened)	600	140
Ceramics (chip glued to substrate)	900	90

2.3 Processing guidelines for ICs

Integrated circuits (ICs) are **e**lectro**s**tatic-**s**ensitive (ESS) devices. The requirement for greater packing density has led to increasingly small structures on semiconductor chips, with the result that today every IC, whether bipolar, MOS, or CMOS, has to be protected against electrostatics.

MOS and CMOS devices generally have integrated protective circuits and it is hardly possible any more for them to be destroyed by purely static electricity. On the other hand, there is acute danger from **e**lectro**s**tatic **d**ischarges (ESD).

Of the multitude of possible sources of discharge, charged devices should be mentioned in addition to charged persons. With low-resitive discharges it is possible for peak power amounting to kilowatts to be produced.

For the protection of devices the following principles should be observed:

a) Reduction of charging voltage, below 200 V if possible.
   Means which are effective here are an increase in relative humidity to $\geq 60\%$ and the replacement of highly charging plastics by antistatic materials.
b) With every kind of contact with the device pins a charge equalization is to be expected. This should always be highly resistive (ideally $R = 10^6$ to $10^8\ \Omega$).

All in all this means that ICs call for special handling, because uncontrolled charges, voltages from ungrounded equipment or persons, surge voltage spikes and similar influences can destroy a device. Even if devices have protective circuits (e.g. protective diodes) on their inputs, the following guidelines for their handling should nevertheless be observed.

2.3.1 Identification

The packing of ESS devices is provided with the following label by the manufacturer: 

2.3.2 Scope

The guidelines apply to the storage, transport, testing, and processing of all kinds of ICs, equipped and soldered circuit boards that comprise such components.

2.3.3 Handling of devices

1. ICs must be left in their containers until they are processed.
2. ICs may only be handled at specially equipped work stations. These stations must have work surfaces covered with a conductive material of the order of 10^6 to $10^9\ \Omega$/cm.
3. With humidity of $> 50\%$ a coat of pure cotton is sufficient. In the case of chargeable synthetic fibers the clothing should be worn close-fitting. The wrist strap must be worn snugly on the skin and be grounded across a resistor of 50 to 100 kΩ.

4. If conductive floors, $R = 5 \times 10^4$ to $10^7\ \Omega$ are provided, further protection can be achieved by using so-called MOS chairs and shoes with a conductive sole ($R \approx 10^5$ to $10^7\ \Omega$).
5. All transport containers for ESS devices and assembled circuit boards must first be brought to the same potential by being placed on the work surface or touched by the operator before the individual devices may be handled. The potential equalization should be across a resistor of 10^6 to $10^8\ \Omega$.
6. When loading machines and production devices it should be noted that the devices come out of the transport magazine charged and can be damaged if they touch metal, e.g. machine parts.

   Example 1) conductive (black) tubes.
   The devices may be destroyed in the tube by charged persons or come out of the tube charged if this is emptied by a charged person.
   Conductive tubes may only be handled at ESS work stations (high-resistance work-station and person grounding).

   Example 2) anti-static (transparent) tubes.
   The devices cannot be destroyed by charged persons in the tube (there may be a rare exception in the case of custom ICs with unprotected gate pins). The devices can be endangered as in 1) when the tube is emptied if the latter, especially at low humidity, is no longer sufficiently anti-static after a long period of storage (> 1 year).

   In both cases damage can be avoided by discharging the devices across a grounded adapter of high-resistance material ($\approx 10^6$ to $10^8\ \Omega$/cm) between the tube and the machine.

   The use of metal tubes – especially of anodized aluminum – is not advisable because of the danger of low-resistance device discharge.

2.3.4 Storage

ESS devices should only be stored in identified locations provided for the purpose. During storage the devices should remain in the packing in which they are supplied. The storage temperature should not exceed 60 °C.

2.3.5 Transport

ESS devices in approved packing tubes should only be transported in suitable containers of conductive or longterm anti-static-treated plastic or possibly unvarnished wood. Containers of high-charging plastic or very low-resistance materials are in like manner unsuitable.

Transfer cars and their rollers should exhibit adequate electrical conductivity ($R < 10^6\ \Omega$). Sliding contacts and grounding chains will not reliably eliminate charges.

2.3.6 Incoming inspection

In incoming inspection the above guidelines should be observed. Otherwise any right to refund or replacement if devices fail inspection may be lost.

2.3.7 Material and mounting

1. The drive belts of machines used for the processing of the devices, in as much as they come into contact with them (e.g. bending and cutting machines, conveyor belts), should be treated with anti-static spray (e.g. anti-static spray 100 from Kontaktchemie). It is better, however, to avoid the contact completely.
2. If ESS devices have to be soldered or desoldered manually, soldering irons with thyristor control may not be used. Siemens EMI-suppression capacitors of the type B 81711-B31...-B36 have proven very effective against line transients.
3. Circuit boards fitted and soldered with ESS devices are always to be considered as endangered.

2.3.8 Electrical tests

1. The devices should be processed with observation of these guidelines. Before assembled and soldered circuit boards are tested, remove any shorting rings.
2. Test receptacles must not be conducting any voltage when individual devices or assembled circuit boards are inserted or withdrawn, unless works specifications state otherwise. Ensure that the test devices do not produce any voltage spikes, either when being turned on and off in normal operation or if the power fuse blows or other fuses respond.
3. Signal voltages may only be applied to the inputs of ICs when or after the supply voltage is turned on. They must be disconnected before or when the supply voltage is turned off.
4. Observe any notes and instructions in the respective data books.

2.3.9 Packing of assembled PC boards or flatpack units

The packing material should exhibit low volume conductivity:
$10^5\ \Omega/cm < \rho < 10^{10}\ \Omega/cm$.

In most cases – especially with humidity of > 40% – this requirement is fulfilled by simple corrugated board. Better protection is obtained with bags of conductive polyethylene foam (e.g. RCAS 1200 from Richmond of Redlands, California).

One should always ensure that boards cannot touch.

In special cases it may be necessary to provide protection against strong electric fields, such as can be generated by conveyor belts for example. For this purpose a sheath of aluminum foil is recommended, although direct contact between the film and the PCB must be avoided. Cardboard boxes with an aluminum-foil lining, such as those used for shipping our devices, are available from Laber of Munich.

2.3.10 Ultrasonic cleaning of ICs

The following recommendation applies to plastic packages. For cavity packages (metal and also ceramic) separate regulations have to be observed.

Freon and isopropyl alcohol (trade name: propanol) can be used as solvents. These solvents can also be used for plastic packages because they do not eat into the plastic material.

An ultrasonic bath in double halfwave operation is advisable because of the low component stress.

The ultrasonic limits are as follows:

sound frequency	$f > 40$ kHz
exposure	$t < 2$ min
alternating sound pressure	$p < 0.29$ bar
sound power	$N < 0.5$ W/cm^2/liter

2.4 Data classification

Maximum ratings

The maximum ratings are absolute limits. The IC may be destroyed if only a single one of these values is exceeded.

Electrical characteristics

The electrical characteristics include the guaranteed tolerances of the values maintained by an IC for the specified operating range.

The typical characteristics are mean values that can be expected on the basis of the production. Unless otherwise specified, the typical characteristics apply to $T_{amb} = 25$ °C and the given supply voltage.

Operating data

The functions stated in the circuit description are fulfilled within the range of the operating data.

2.5 Quality specifications

AQL values and definitions of defects for electronic components

2.5.1 Explanations

AQL (acceptable quality level) agreements specify the sampling conditions for the incoming inspection of consignments (conformance test). AQL values in conjunction with the standard sampling inspection plans determine the acceptance or rejection of delivery lots. The size and maximum permissible number of defects of the samples is based on DIN 40 080 (identical with MIL Standard 105 D and IEC 410), single sampling plan for normal inspection, inspection level II. The sampling instructions of this standard are such that a delivery lot will most probably be accepted (> 90%) if the defect percentage is equal or less than the specified AQL value. Generally, the average defect percentage of the products we deliver is far below the AQL value.

2.5.2 Definition of defects

A component is considered defective if it does not comply with the characteristics specified in the data sheet or in an agreed upon delivery specification. Defects can be divided into inoperatives, which generally exclude a functional application of the component, and defects of less significance.

Inoperatives are:

- open or short circuit
- broken component, package or pins
- missing or incorrect marking
- incorrect identification of pins
- intermixing with other device types
- alternating orientation of ICs in a packaging tube or belt

The remaining defects can be divided into

- electrical defects (maximum ratings exceeded)
- mechanical defects, e.g. dimensions not adhered to, package damaged, illegible marking, bent leads

Grouping into major defects and minor defects according to DIN 40 080 has been purposely avoided here because these terms are defined primarily on the basis of applications and not specifications. In contrast to this the defect classes that we use – for which AQL values are given below – are clearly outlined by the specification and the mentioned inoperatives.

2.5.3 AQL values

The AQL values valid for the different product families are comprised in the following table:

Defect type	AQL values MSI/SSI*	AQL values LSI/VLSI*
Inoperative (mechanical and electrical)	0.065	0.15
Σ electrical defects	0.15	0.25
Σ mechanical defects	0.25	0.25

for switching times and noise measurements an AQL of 1.5 applies.

* SSI/MSI (< 250 gates/IC): bipolar ICs, with a few exceptions
LSI/VLSI (≥ 250 gates/IC): all MOS ICs

2.5.4 Incoming inspection

The tests carried out by the manufacturer are intended to make expensive incoming inspections by the user unnecessary. If the user, nevertheless, wants to carry out incoming inspection, the use of a sampling inspection plan as described in section 5 is recommended. The test method that is applied must be agreed upon between the user and the supplier.

The following information is necessary for judging any claims that may arise: test circuit, sample size, number of defective items found, sample of evidence, packing list.

2.5.5 Sampling plan for normal inspection

in accordance with DIN 40 080 or ABC-Std 105 D, inspection level II

Lot size	Sample size	AQL value										
		0,065	0,10	0,15	0,25	0,40	0,65	1,0	1,5	2,5	4,0	6,5
		A R	A R	A R	A R	A R	A R	A R	A R	A R	A R	A R
2 to 8	2											⇓ 0 1 ⇑
9 to 15	3										⇓ 0 1 ⇑	
16 to 25	5									⇓ 0 1 ⇑		
26 to 50	8								⇓ 0 1 ⇑	⇕	⇓ 1 2 ⇑	1 2
51 to 90	13							⇓ 0 1 ⇑	⇕	⇕	1 2	2 3
91 to 150	20						⇓ 0 1 ⇑	⇕	⇕	1 2	2 3	3 4
151 to 280	32					⇓ 0 1 ⇑	⇕	⇕	1 2	2 3	3 4	5 6
281 to 500	50				⇓ 0 1 ⇑	⇕	⇕	1 2	2 3	3 4	5 6	7 8
501 to 1200	80			⇓ 0 1 ⇑	⇕	⇕	1 2	2 3	3 4	5 6	7 8	10 11
1201 to 3200	125		⇓ 0 1 ⇑	⇕	⇓ 1 2 ⇑	1 2	2 3	3 4	5 6	7 8	10 11	14 15
3201 to 10000	200	⇓ 0 1 ⇑	⇕	⇓ 1 2 ⇑	2 3	2 3	3 4	5 6	7 8	10 11	14 15	21 22
10001 to 35000	315	⇕	⇕	1 2	2 3	3 4	5 6	7 8	10 11	14 15	21 22	⇑
35001–150000	500	⇓	1 2	2 3	3 4	5 6	7 8	10 11	14 15	21 22	⇑	⇕
150001–500000	800	1 2	2 3	3 4	5 6	7 8	10 11	14 15	21 22	⇑	⇕	⇕
500001 and more	1250	2 3	3 4	5 6	7 8	10 11	14 15	21 22	⇑	⇕	⇕	⇕

A = Acceptance number, i.e. maximum number of defective units in a sample up to which a lot is accepted.

R = Rejection number, i.e. the number of defective units which must be found in a sample as a minimum for rejection of the lot.

Additional conditions

As the combination "Acceptance 0/Rejection 1" is not particularly clear, the next largest sample should be taken.

2.5.6 Notes

Stating AQL values is no assurance of characteristics in a legal sense. The agreement of sampling inspections and AQL values does not prevent the customer from carrying out more extensive tests in incoming inspection and claiming replacements for individual defective components under the terms of sale. Any further liability, especially as regards the consequences of component defects, cannot be recognized.

2.5.7 Reliability

ICs provide optimal reliability and service life if the junction temperature does not exceed 125 °C in operation. Operation up to the maximum permissible limit of the junction temperature at 150 °C is possible in principle. It should be noted, however, that exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2.6 Logic functions and symbols

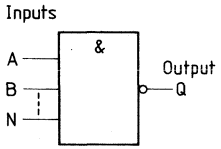
Logic levels

In accordance with DIN 41785, sheet 4, for digital microcircuits, the two possible ranges of the binary electrical quantity are designated L (low) and H (high). The values of the L range are closer to $-\infty$ and those of the H range closer to $+\infty$. Similarly, the index A applies to the upper limit value (closer to $+\infty$) and index B to the lower limit value (closer to $-\infty$).

The previous logic symbols 0 and 1, or **0** and **L**, or logic 0 and logic 1 are no longer used; the statement of positive or negative logic is also no longer necessary.

Gate symbols
in accordance with DIN 40900, part 12

NAND gate

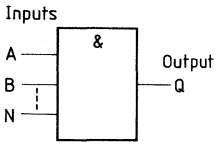


Truth table of NAND gate with two inputs.

Inputs A	Inputs B	Output Q
L	L	H
L	H	H
H	L	H
H	H	L

Logic function: $Q = \overline{A \wedge B \quad \ldots \wedge N}$
Definition: an L signal will only be present at the output if A and B and . . . and N show an H signal.

AND gate

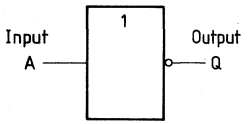


Truth table of AND gate with two inputs.

Inputs A	Inputs B	Output Q
L	L	L
L	H	L
H	L	L
H	H	H

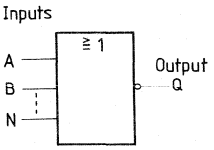
Logic function: $Q = A \wedge B \quad \ldots \wedge N$
Definition: an H signal will only be present at the output if A and B and . . . and N show an H signal.

Inverter



Logic function: $Q = \overline{A}$

NOR gate

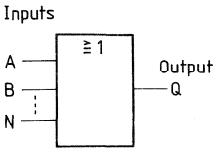


Truth table of NOR gate with two inputs

Inputs A	Inputs B	Output Q
L	L	H
L	H	L
H	L	L
H	H	L

Logic function: $Q = \overline{A \vee B \vee \ldots \vee N}$
Definition: an H signal will only be present at the output if A and B and . . . and N show an L signal.

OR gate

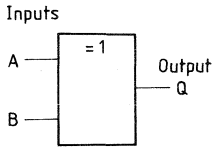


Truth table of OR gate with two inputs

Inputs A	Inputs B	Output Q
L	L	L
L	H	H
H	L	H
H	H	H

Logic function: $Q = A \vee B \vee \ldots \vee N$
Definition: an L signal will only be present at the output if A and B and . . . and N show an L signal.

Exclusive OR gate

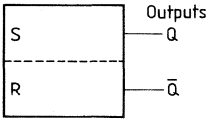


Truth table of exclusive-OR gate with two inputs

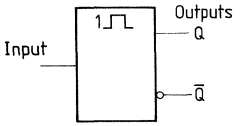
Inputs A	Inputs B	Output Q
L	L	L
L	H	H
H	L	H
H	H	L

Logic function: $Q = (A \wedge \overline{B}) \wedge (\overline{A} \wedge B)$
Definition: an H signal will only be present at the output if either only A or only B shows an H signal.

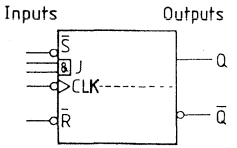
Symbols for bistable and monostable elements



Bistable element (flipflop)

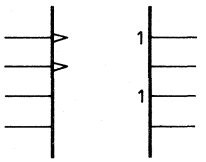


Monostable element (monoflop) with an input acting upon both outputs. The arrow indicates the output which is H when the circuit is stable.



J1, J2 and K are information inputs.
J1 and J2 are ANDed.
Inputs J and K are (clock-) controlled by the input CLK
$\overline{S}$ and $\overline{R}$ are independent set and reset inputs.

Identification of dynamic inputs



Effect at output with transition of input signal from H to L
Effect at output with transition of input signal from L to H
Effect of input signal during H signal
Effect of input signal during L signal

2.7 Introduction to operational amplifiers

Integrated operational amplifiers (op amps) are dc voltage amplifiers with a very broad scope of applications in control technology, industrial electronics, and in audio frequency engineering.

2.7.1 Symbols and terms used

The logic symbol "operational amplifier" shows only signal inputs and outputs. Figure 1 shows the symbol used, with an "inverting" input 1, a "non-inverting" input 2, and an output 3. A positive signal at input 1 results in a negative signal at output 3.

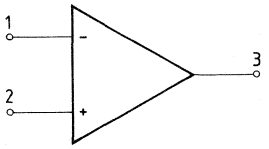


Figure 1

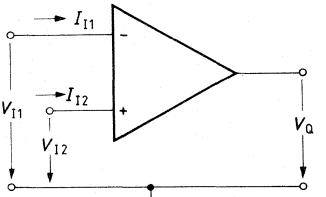


Figure 2

Definitions of the most important terms generally used to characterize an operational amplifier, are listed below. All definitions refer to symmetrical supply voltages.

a) Input offset voltage V_{IO} is that voltage difference which must be applied to the input terminals to achieve an output voltage of 0 V (fig. 2).
$V_{IO} = V_{I1} - V_{I2}$ at $V_Q = 0$ and generator resistance $R_G = 50\ \Omega$.

b) Input current I_I is the average static input current required for op amp operation (fig. 2).

$$I_I = \frac{I_{I1} + I_{I2}}{2}$$

c) Input offset current I_{IO} is the difference between the input currents in the operating range. At high values of generator resistance, I_{IO} may cause difficulties (fig. 2).

d) Open-loop voltage gain G_{V0} is the amplification without feedback (fig. 3).

$$G_{V0} = \frac{V_Q}{V_I}$$

d) Common-mode voltage gain G_{VC} is the amplification of an in-phase signal applied to both inputs (fig. 4).

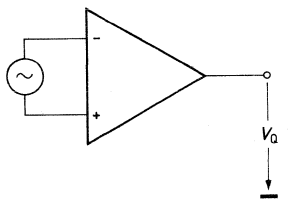


Figure 3

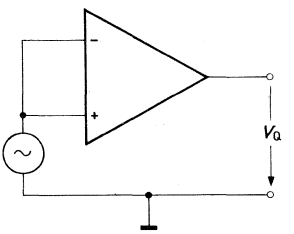
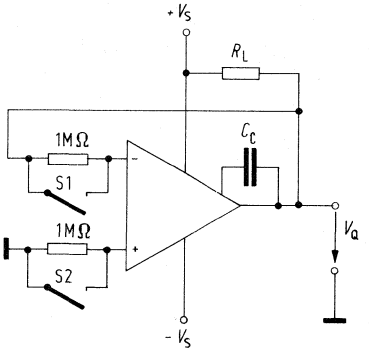


Figure 4

2.7.2 Test circuits for operational amplifiers

Input current, input offset current



S1 open – S2 closed;

$$I_{I-} = \frac{V_Q}{1\,M\Omega}$$

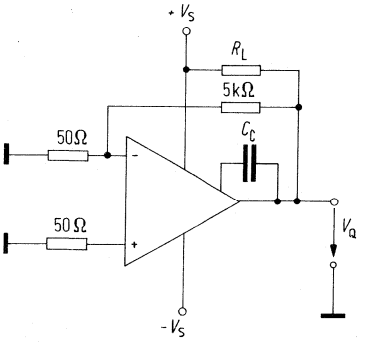
S2 open – S1 closed:

$$I_{I+} = \frac{V_Q}{1\,M\Omega}$$

S1 + S2 open:

I_{IO} approx. $\frac{V_Q}{1\,M\Omega}$

Input offset voltage

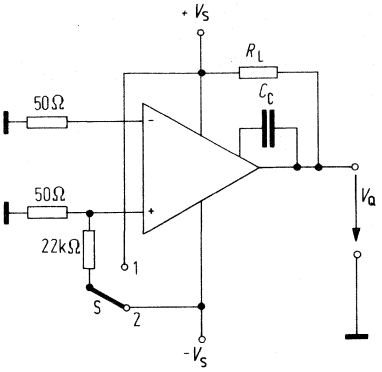


$$-V_{IO} = V_{QO}/G_{V0}$$

$$G_{V0} = 100$$

$$-V_{IO} = \frac{V_{QO}}{100}$$

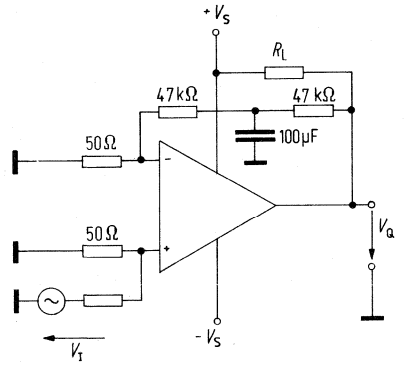
Output voltage, control range



S in position 1: $V_Q = V_{QL}$

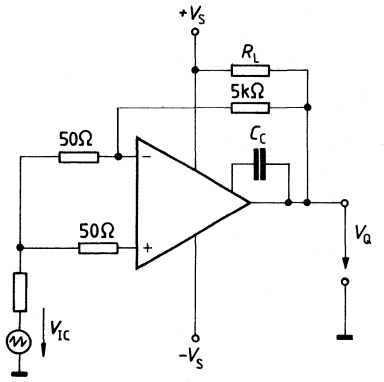
S in position 2: $V_Q = V_{Q0}$

Open-loop voltage gain at $f = 1$ kHz



$$G_{V0} = 20 \log \frac{V_Q}{V_I} \text{ [dB]}$$

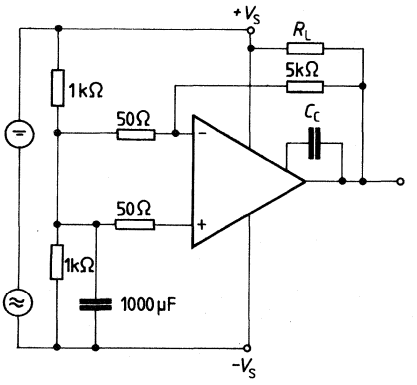
Common-mode rejection



$$G_{VC} = \frac{\Delta V_Q}{\Delta V_{IC}}$$

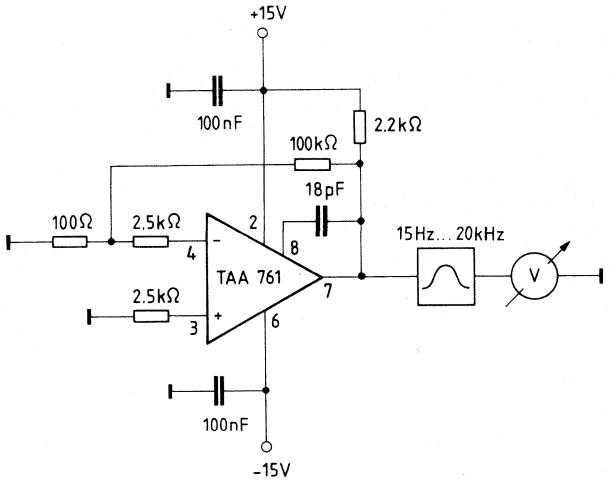
$$k_{CMR} = 20 \log \frac{G_{V0}}{G_{VC}} \text{ [dB]}$$

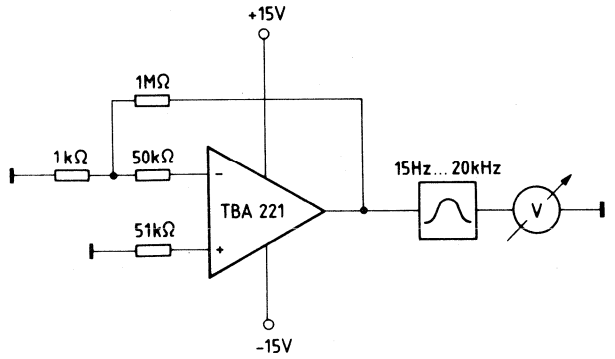
Supply voltage rejection



$$\frac{\Delta V_{IO}}{\Delta V_S} = \frac{\Delta V_Q}{100 \times \Delta V_S}$$

Noise voltage in accordance with DIN 45 405
Psophometer U 2033 (from Siemens)
Position: noise voltage; evaluation peak/zero





Relationship between slew rate *SR* and cutoff frequency for high-signal output voltage swing (power bandwidth f_p)

The slew rate of an operational amplifier is determined by the charge/discharge of capacitors. For a capacitor the charge is $Q = C \cdot V$ or $Q = \int I \cdot dt$. The voltage of capacitors changes as:

$$dv/dt \approx \Delta V/\Delta t = I/C$$

For the given current, faster charging or discharging of capacitors is not possible. This maximum speed of the voltage change is indicated for op amps by the factor *SR* (so-called slew rate) which is given in V/µs. Usual values are of the order of 0.3 to 20 V/µs.

The maximum frequency of a sinewave signal that is amplified without distortion is determined by the steepness of the sinewave signal at the zero crossover ($t = 0$).

The sinewave signal of amplitude V_{QS} and angular frequency ω ($= 2\pi f$) has a steepness that is described by the first derivative of this function:

signal: $V_q = V_{QS} \cdot \sin(\omega t)$
1st derivative: $dvq/dt_{max} = V_{QS} \cdot \omega \cdot \cos(\omega t)$

for $t = 0$: $\cos(\omega t) = 1$
thus: $dvq/dt_{max} = V_{QS} \cdot \omega \cdot 1 = V_{QS} \cdot 2\pi f$

This value must be less than or equal to the slew rate of the op amp for a distortion-free output signal.

$$SR \geq V_{QS} \cdot 2\pi f$$

Therefore:
$$f_p = \frac{SR}{2 \cdot \pi \cdot V_{QS}} = \frac{SR}{2 \cdot \pi \cdot \sqrt{2} \cdot V_{Qrms}}$$

$$V_{Qrms} = \frac{SR}{2 \cdot \pi \cdot \sqrt{2} \cdot f_p}$$

Example 1: $SR = 0.5\ V/\mu s$ (corresponding to 500,000 V/s)

$V_{Qrms} = 10\ V$

$$f_p = \frac{500\,000}{2 \cdot \pi \cdot \sqrt{2} \cdot 10} = 5.62\ kHz$$

If a signal of 10 kHz is to be transmitted, this is possible without distortion up to an rms voltage of 5.62 V.

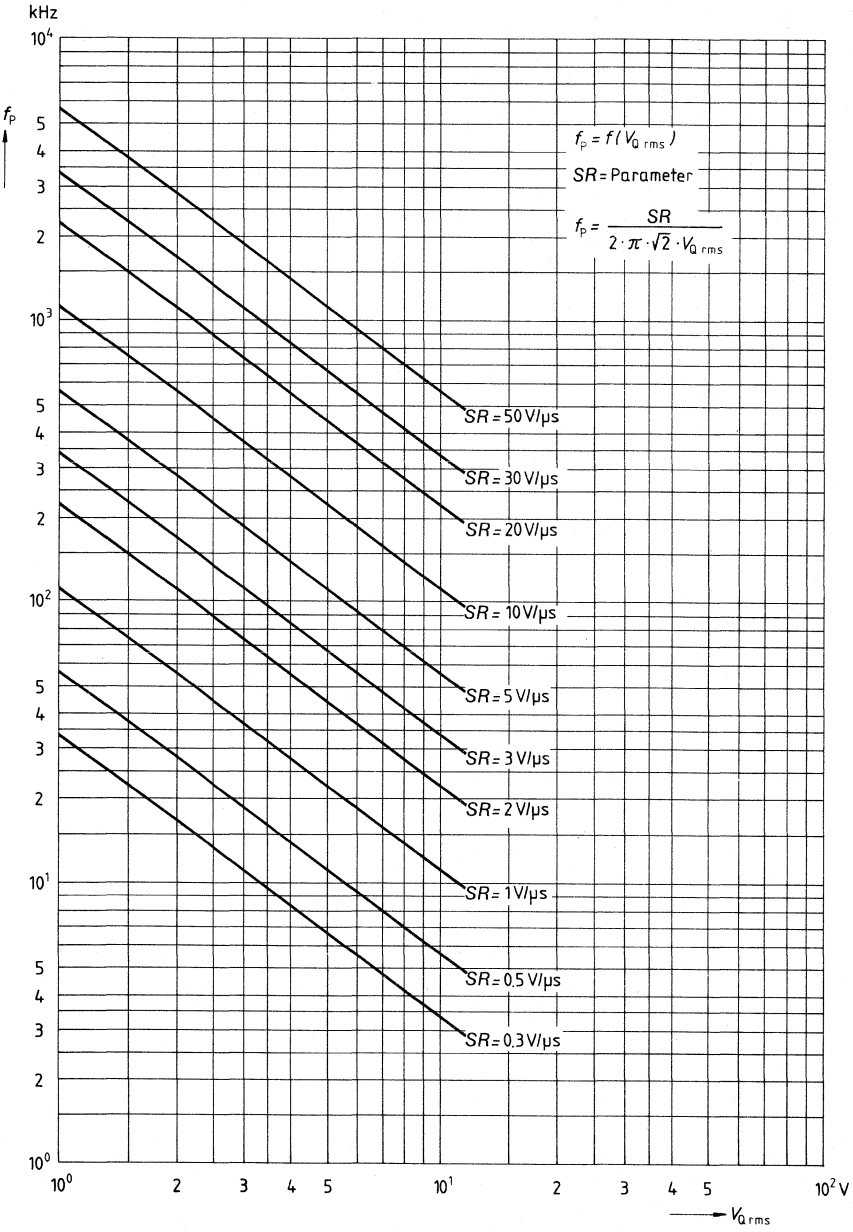
Example 2: $SR = 10\ V/\mu s$

$V_{Qrms} = 10\ V$

$f_p = 112\ kHz$

The bandwidth cannot of course be infinite (as is possible in the equation). Additionally there is a limitation in the small-signal cutoff frequency (f_T).

Slew rate and power bandwidth



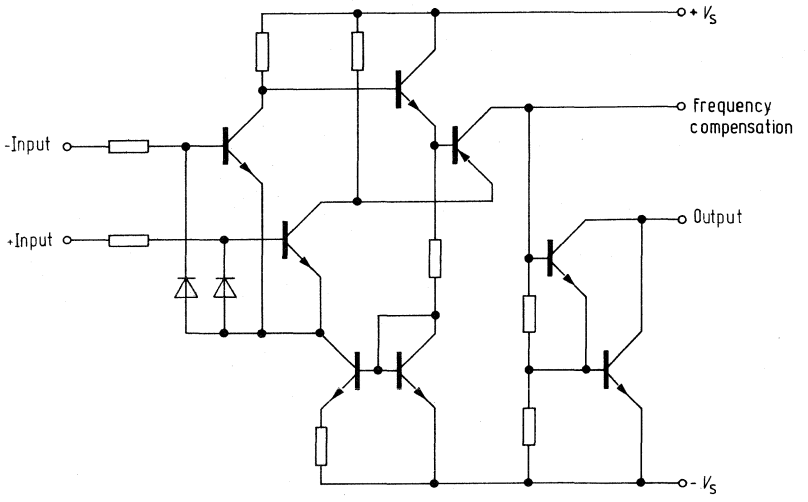
Type	Ordering code	Package	Color code	Fig. No.
TAA 762 A	Q67000-A2271	DIP 6	–	5
TAA 762 G	Q67000-A2273	similar to SO 6	white/yellow	25
TAA 765 A	Q67000-A524	DIP 6	–	5
TAA 765 G	Q67000-A599-G1	similar to SO 6	yellow/yellow	25

Particularly economic and versatile op amps. Owing to their excellent performance qualities they are well suited for a wide scope of applications, as in control engineering, automotive electronics, AF circuits, analog computers, etc.

In addition to high gain, high input resistance, low offset voltage, minor dependence on temperature and supply voltage, the amplifiers are outstanding for:

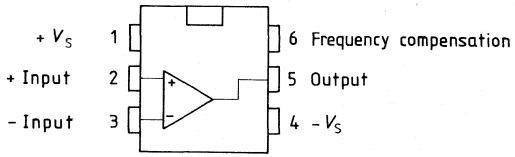
- Wide common-mode range
- Large supply voltage range
- Large control range
- Wide temperature range (TAA 762)
- High output current
- Simple frequency compensation

Circuit diagram

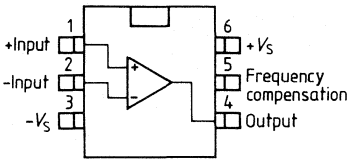


Pin configurations

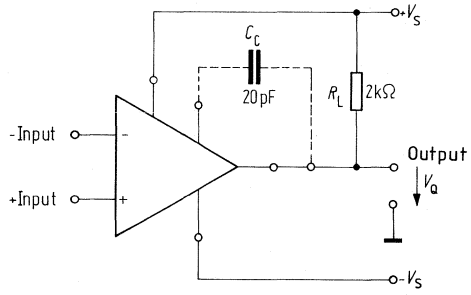
TAA 762 A
TAA 765 A



TAA 762 G
TAA 765 G



Connection diagram



C_C = output frequency compensation; R_L = load resistor

Maximum ratings

Supply voltage		V_S	± 18	V
Output current		I_Q	70	mA
Differential input voltage		V_{ID}	± V_S	V
Junction temperature		T_j	150	°C
Storage temperature range		T_{stg}	−55 to 125	°C
Thermal resistance (system-air)	TAA 762 A	$R_{th\ SA}$	115	K/W
	TAA 762 G	$R_{th\ SA}$	200	K/W

Operating range

Supply voltage range	V_S	± 1.5 to ± 18	V
Ambient temperature range	T_{amb}	−55 to 125	°C

Characteristics

V_S = ± 5 V to ± 15 V

		T_{amb} = 25 °C			T_{amb} = −55 to 125 °C		
		min	typ	max	min	max	
Open-loop supply current consumption	I_S		1.5	2.5		2.5	mA
Input offset voltage (R_G = 50 Ω)	V_{IO}	−4		4	−6	6	mV
Input offset current	I_{IO}	−100	± 50	100	−300	300	nA
Input current	I_I		0.3	0.7		1.0	µA
Output voltage (R_L = 2 kΩ, V_S = ± 15 V)	V_{Qpp}	14.9		−14	14.8	−14	V
Output voltage (R_L = 620 Ω, V_S = ± 15 V)	V_{Qpp}	14.9		−12.5	14.8	−12	V
Output voltage (R_L = 2 kΩ, V_S = ± 15 V, f = 100 kHz)	V_{Qpp}		± 10				V
Input impedance (f = 1 kHz)	Z_i		200				kΩ
Open-loop voltage gain (R_L = 2 kΩ, f = 1 kHz)	G_{V0}	85	87		80		dB
Open-loop voltage gain (R_L = 10 kΩ, f = 1 kHz)	G_{V0}		92				dB
Open-loop voltage gain (R_L = 2 kΩ, f = 1 MHz)	G_{V0}		43				dB
Output reverse current	I_{QR}			1		5	µA

Characteristics
$V_S = \pm 5$ V to ± 15 V

		$T_{amb} = 25$ °C			$T_{amb} = -55$ to 125 °C		
		min	typ	max	min	max	
Common-mode input voltage range ($R_L = 2$ kΩ, $V_S = \pm 15$ V)	V_{IC}	13	±14	−13	12	−12	V
Common-mode rejection ($R_L = 2$ kΩ)	k_{CMR}	80	85		75		dB
Supply voltage rejection ($G_V = 100$)	k_{SVR}		25	200		200	µV/V
Temperature coefficient of V_{IO} ($R_G = 50$ Ω)	α_{VIO}		6	25		25	µV/K
Temperature coefficient of I_{IO} ($R_G = 50$ Ω)	α_{IIO}		0.3	1,5		1.5	nA/K
Slew rate of V_q for non-inverting operation*) (test circuit 1)	SR		9				V/µs
Slew rate of V_q for inverting operation*) (test circuit 2)	SR		18				V/µs
Noise voltage (in acc. with DIN 45405; referred to input; $R_S = 2.5$ kΩ)	V_n		3				µV

Characteristics
$V_S = \pm 2$ V

Input offset voltage	V_{IO}	−4		4	−6	6	mV
Input offset current	I_{IO}	−70		70	−200	200	nA
Input current	I_I		0,2	0,5		0,8	µA
Open-loop voltage gain ($R_L = 2$ kΩ, $f = 1$ kHz)	G_{V0}	80			75		dB

*) For the relationship between power bandwidth and slew rate refer to "General information" page 40

Maximum ratings

Supply voltage		V_S	± 18	V
Output current		I_Q	70	mA
Differential input voltage		V_{ID}	± V_S	V
Junction temperature		T_j	150	°C
Storage temperature range		T_{stg}	−55 to 125	°C
Thermal resistance (system-air)	TAA 765 A	$R_{th\ SA}$	115	K/W
	TAA 765 G	$R_{th\ SA}$	200	K/W

Operating range

Supply voltage range	V_S	± 1.5 to ± 18	V
Ambient temperature range	T_{amb}	−25 to 85	°C

Characteristics

$V_S = \pm 5$ V to ± 15 V

		$T_{amb} = 25$ °C			$T_{amb} = -25$ to 85 °C		
		min	typ	max	min	max	
Open-loop supply current consumption	I_S		1.5	2.5		2.5	mA
Input offset voltage ($R_G = 50\ \Omega$)	V_{IO}	−5.5		5.5	−7	7	mV
Input offset current	I_{IO}	−200	±80	200	−300	300	nA
Input current	I_I		0.5	0.8		1.0	µA
Output voltage ($R_L = 2$ kΩ, $V_S = \pm 15$ V)	V_{Qpp}	14.9		−14	14.8	−14	V
Output voltage ($R_L = 620\ \Omega$, $V_S = \pm 15$ V)	V_{Qpp}	14.9		−12.5	14.8	−12	V
Output voltage ($R_L = 2$ kΩ, $V_S = \pm 15$ V, $f = 100$ kHz)	V_{Qpp}		± 10				V
Input impedance ($f = 1$ kHz)	Z_i		200				kΩ
Open-loop voltage gain ($R_L = 2$ kΩ, $f = 1$ kHz)	G_{V0}	80	85		80		dB
Open-loop voltage gain ($R_L = 10$ kΩ, $f = 1$ kHz)	G_{V0}		90				dB
Open-loop voltage gain ($R_L = 2$ kΩ, $f = 1$ MHz)	G_{V0}		43				dB
Output reverse current	I_{QR}			10		20	µA

Characteristics
$V_S = \pm 5$ V to ± 15 V

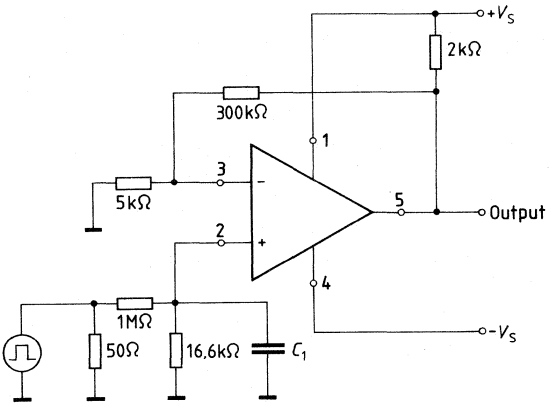
		$T_{amb} = 25$ °C			$T_{amb} = -25$ to 85 °C		
		min	typ	max	min	max	
Common-mode input voltage range ($R_L = 2$ kΩ, $V_S = \pm 15$ V)	V_{IC}	13	±14	−13	12	−12	V
Common-mode rejection ($R_L = 2$ kΩ)	k_{CMR}	75	83		75		dB
Supply voltage rejection ($G_V = 100$)	k_{SVR}		25	200		200	µV/V
Temperature coefficient of V_{IO} ($R_G = 50$ Ω)	α_{VIO}		6	25		25	µV/K
Temperature coefficient of I_{IO} ($R_G = 50$ Ω)	α_{IIO}		0.3	1.5		1.5	nA/K
Slew rate of V_q for non-inverting operation*) (test circuit 1)	SR		9				V/µs
Slew rate of V_q for inverting operation*) (test circuit 2)	SR		18				V/µs
Noise voltage (in acc. with DIN 45405; referred to input; $R_S = 2.5$ kΩ)	V_n		3				µV

Characteristics
$V_S = \pm 2$ V

Input offset voltage	V_{IO}	−6		6	−7.5	7.5	mV
Input offset current	I_{IO}	−150		150	−200	200	nA
Input current	I_I		0,2	0.6		0,8	µA
Open-loop voltage gain ($R_L = 2$ kΩ, $f = 1$ kHz)	G_{V0}	75			75		dB

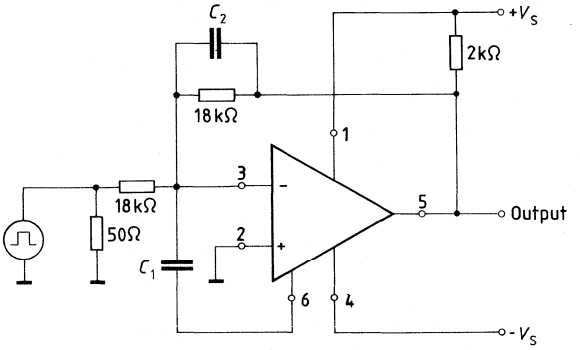
*) For the relationship between power bandwidth and slew rate refer to "General information" page 40

Test circuit 1 for slew rate (non-inverting operation)



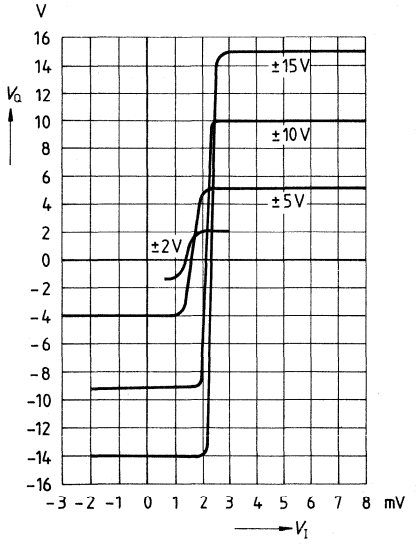
C_1 for min. overshoot (approx. 22 pF)

Test circuit 2 for slew rate (inverting operation)

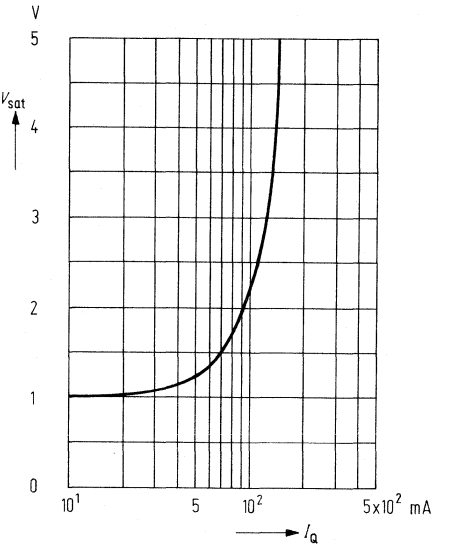


C_2 causes a frequency-dependent compensation to reduce rise times (approx. 390 pF)
C_1 for min. overshoot (approx. 3.9 pF)

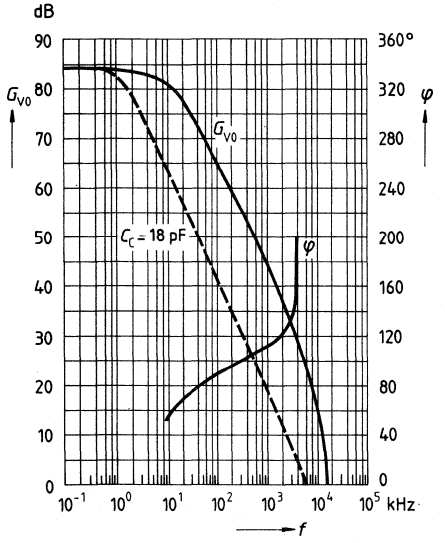
Transfer characteristic
Output voltage versus input voltage
V_S = parameter, $R_L = 2\ k\Omega$



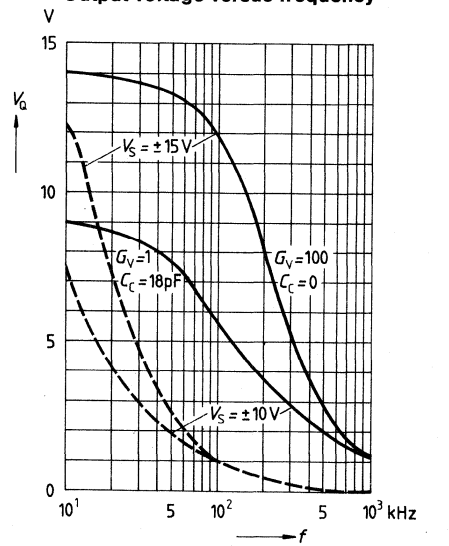
Saturation voltage versus output current
$T_{amb} = 25\ °C$



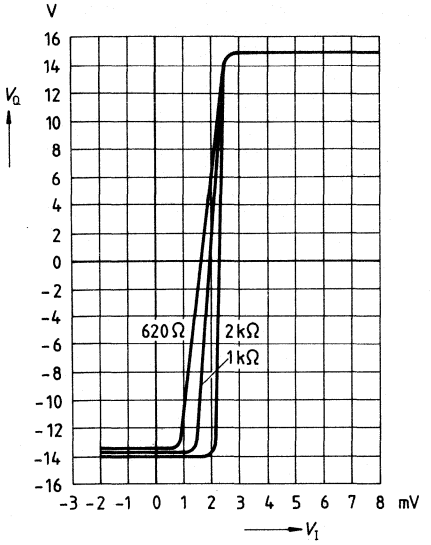
Open-loop voltage gain and phase versus frequency
$V_S = \pm 15\ V$; $R_L = 2\ k\Omega$



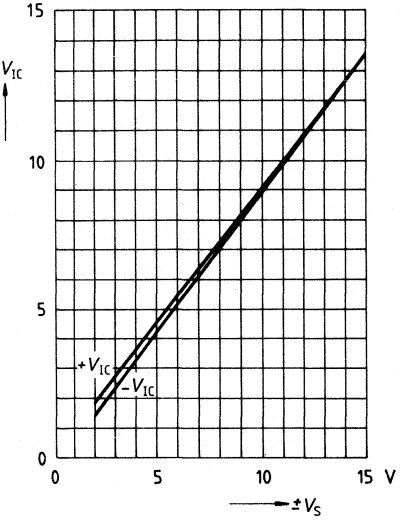
Frequency dependence of large signal modulation
Output voltage versus frequency



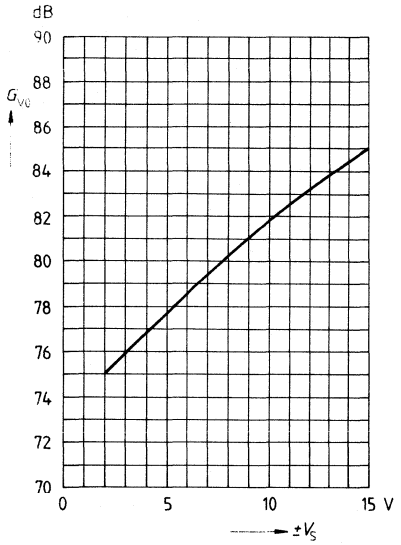
Transfer characteristic
Output voltage versus input voltage
$V_S = \pm 15$ V; R_L = parameter



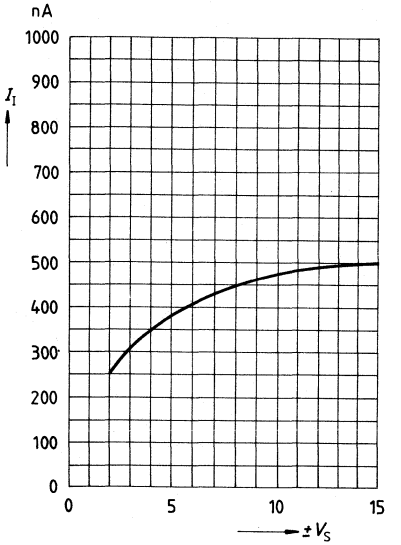
Common-mode voltage range
Common-mode input
voltage versus supply voltage



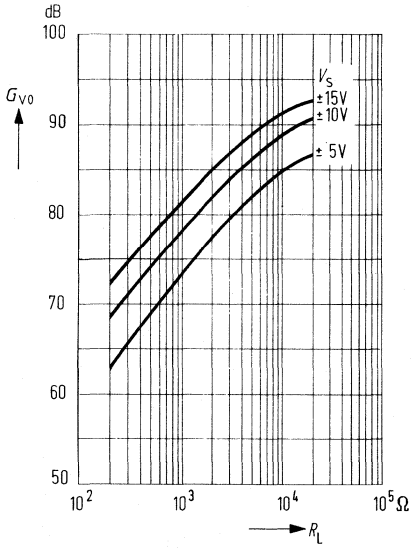
Open-loop voltage gain versus supply voltage
$T_{amb} = 25\,°C$, $R_L = 2\,k\Omega$



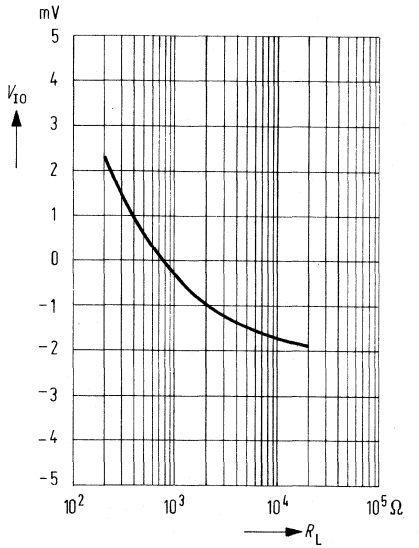
Input current versus supply voltage



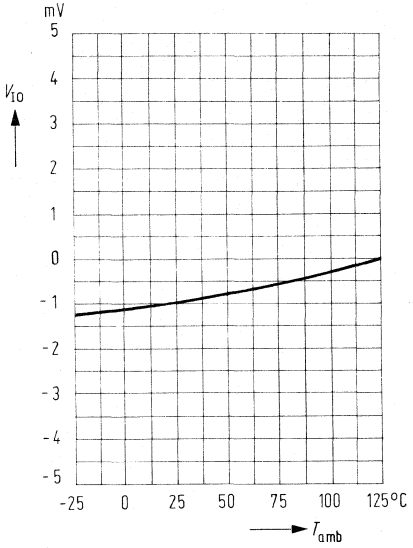
Open-loop voltage gain versus load resistance
$T_{amb} = 25\,°C$



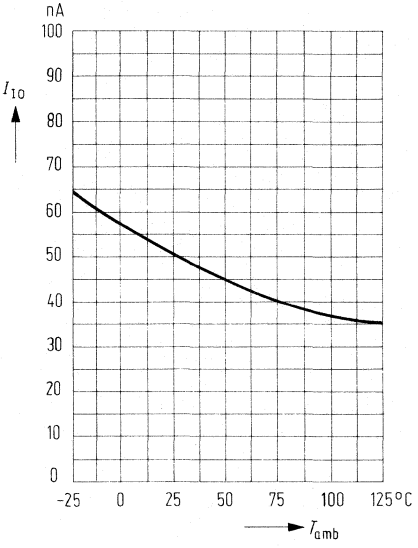
Input offset voltage versus load resistance
$V_S = \pm\,15\,V$



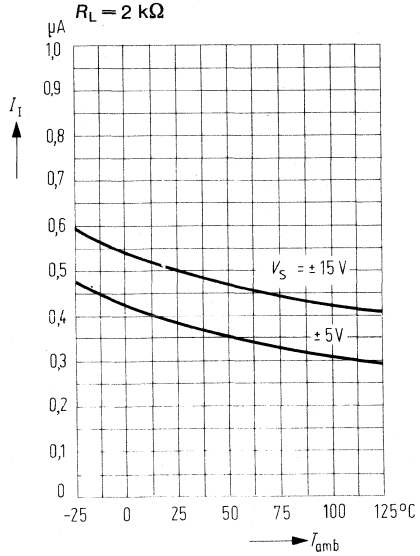
Input offset voltage versus ambient temperature
$R_L = 2\ k\Omega$, $V_S = \pm 15\ V$



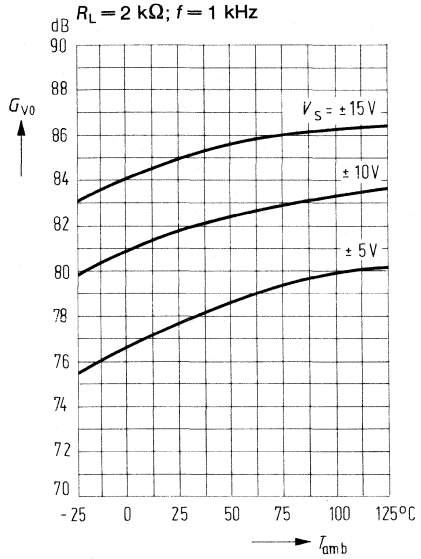
Input offset current versus ambient temperature
$R_L = 2\ k\Omega$, $V_S = \pm 15\ V$



Input current versus ambient temperature
$R_L = 2\ k\Omega$



Open-loop voltage gain versus ambient temperature
$R_L = 2\ k\Omega$; $f = 1\ kHz$



Type	Ordering code	Package	Color code	Fig. No.
TCA 332 A	Q67000-A2272	DIP 6	–	5
TCA 332 G	Q67000-A2270	similar to SO 6	orange/yellow	25
TCA 335 A	Q67000-A563	DIP 6	–	5
TCA 335 G	Q67000-A1018-G1	similar to SO 6	blue/yellow	25

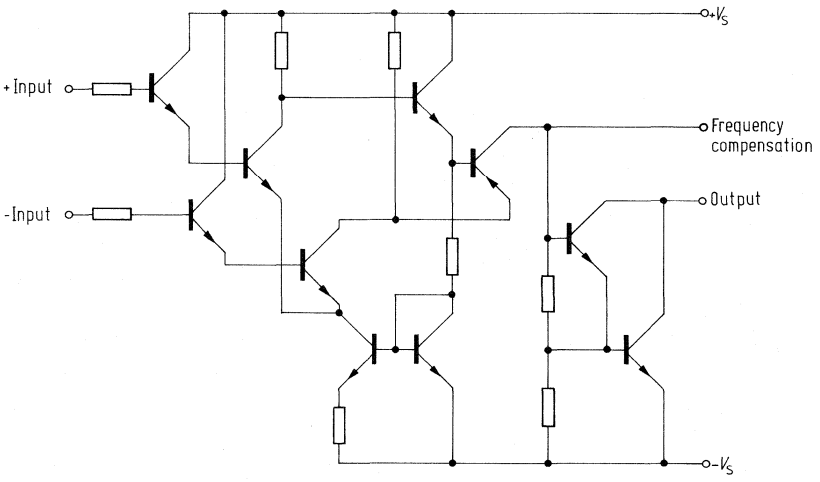
For TCA 315 A, G; TCA 325 A, G see chapter "Comparators".

Economic and versatile op amps. Owing to their excellent performance characteristics they are well suited for a wide scope of applications, such as measuring and control engineering, automotive electronics, AF circuits, analog computers, etc. The low input current of these amplifiers is particularly advantageous for application in measuring and control systems.

In addition to high gain, low offset voltage, minor dependence on temperature and supply voltage, the amplifiers are outstanding for:

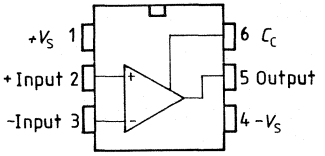
- High input resistance
- Wide common-mode range
- Large supply-voltage range
- Large control range
- High output current
- Simple frequency compensation
- Wide temperature range (TCA 332)

Circuit diagram

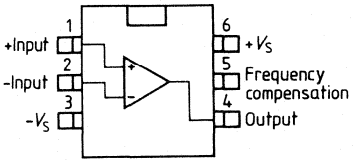


Pin configurations

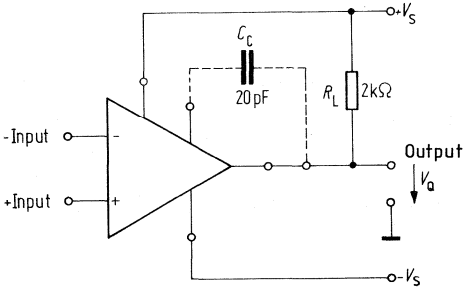
TCA 332 A
TCA 335 A



TCA 332 G
TCA 335 G



Connection diagram



C_C = output frequency compensation
R_L = load resistor

Maximum ratings

Supply voltage		V_S	± 15	V
Output current		I_Q	70	mA
Differential input voltage: V_S = 13 to 15 V		V_{ID}	± 13	V
Differential input voltage: V_S = 2 to 13 V		V_{ID}	± V_S	V
Junction temperature		T_j	150	°C
Storage temperature range		T_{stg}	−55 to 125	°C
Thermal resistance (system-air)	TCA 332 A	$R_{th\ SA}$	115	K/W
	TCA 332 G	$R_{th\ SA}$	200	K/W

Operating range

Supply voltage range	V_S	± 2 to ± 15	V
Ambient temperature range	T_{amb}	−55 to 125	°C

Characteristics

V_S = ± 5 V to ± 15 V

		T_{amb} = 25 °C			T_{amb} = −55 to 125 °C		
		min	typ	max	min	max	
Open-loop supply current consumption	I_S		1.5	2.5		2.5	mA
Input offset voltage (R_G = 50 Ω)	V_{IO}	−10		10	−15	15	mV
Input offset current	I_{IO}	−5		5	−10	10	nA
Input current	I_I		5	15		25	nA
Input current (V_{ID} = ± 13 V)	I_I			200			nA
Output voltage							
(R_L = 2 kΩ, V_S = ± 15 V)	$V_{Q\ pp}$	14.9		−14.0	14.8	−14.0	V
(R_L = 620 Ω, V_S = ± 15 V)	$V_{Q\ pp}$	14.9		−12.5	14.8	−12.0	V
(R_L = 2 kΩ, V_S = ± 15 V, f = 100 kHz)	$V_{Q\ pp}$		± 10				V

Characteristics $V_S = \pm 5$ V to ± 15 V		$T_{amb} = 25$ °C			$T_{amb} = -55$ to 125 °C		
		min	typ	max	min	max	
Input impedance ($f = 1$ kHz)	Z_i		3				MΩ
Open-loop voltage gain							
($R_L = 2$ kΩ, $f = 1$ kHz)	G_{V0}	80	83		75		dB
($R_L = 10$ kΩ, $f = 1$ kHz)	G_{V0}		88				dB
($R_L = 2$ kΩ, $f = 1$ MHz)	G_{V0}		43				dB
Common-mode input voltage range ($R_L = 2$ kΩ, $V_S = \pm 15$ V)	V_{IC}	13		−13	12	−12	V
Common-mode rejection ($R_L = 2$ kΩ)	k_{CMR}	75	80		70		dB
Supply voltage rejection ($G_V = 100$)	k_{SVR}		25	200		200	μV/V
Temperature coefficient of V_{IO} ($R_G = 50$ Ω)	α_{VIO}		12	50		50	μV/K
Temperature coefficient of I_{IO}	α_{IIO}		50				pA/K
Slew rate of V_q for non-inverting operation*) (see TAA 765, test circuit 1)	SR		9				V/μs
Slew rate of V_q for inverting operation*) (see TAA 765, test circuit 2)	SR		18				V/μs
Output saturation voltage ($I_Q = 10$ mA)	V_{Qsat}			1			V
Output reverse current	I_{QR}			1		5	μA

Characteristics $V_S = \pm 2$ V							
Input offset voltage ($R_G = 50$ Ω)	V_{IO}	−10		10	−15	15	mV
Input offset current	I_{IO}	−5		5	−10	10	nA
Input current	I_I		5	15		25	nA
Open-loop voltage gain ($R_L = 2$ kΩ, $f = 1$ kHz)	G_{V0}	75			70		dB

*) For the relationship between power bandwidth and slew rate refer to "General information" page 40

Maximum ratings

Supply voltage		V_S	± 15	V
Output current		I_Q	70	mA
Differential input voltage: V_S = 13 to 15 V		V_{ID}	± 13	V
Differential input voltage: V_S = 2 to 13 V		V_{ID}	± V_S	V
Junction temperature		T_j	150	°C
Storage temperature range		T_{stg}	−55 to 125	°C
Thermal resistance (system-air)	TCA 335 A	$R_{th\ SA}$	115	K/W
	TCA 335 G	$R_{th\ SA}$	200	K/W

Operating range

Supply voltage range	V_S	± 2 to ± 15	V
Ambient temperature range	T_{amb}	−25 to 85	°C

Characteristics

V_S = ± 5 V to ± 15 V

		T_{amb} = 25 °C			T_{amb} = −25 to 85 °C		
		min	typ	max	min	max	
Open-loop supply current consumption	I_S		1.5	2.5		2.5	mA
Input offset voltage (R_G = 50 Ω)	V_{IO}	−15		15	−18	18	mV
Input offset current	I_{IO}	−10		10	−20	20	nA
Input current	I_I		5	25		35	nA
Input current (V_{ID} = ± 13 V)	I_I			200			nA
Output voltage							
(R_L = 2 kΩ, V_S = ± 15 V)	$V_{Q\ pp}$	14.9		−14.0	14.8	−14.0	V
(R_L = 620 Ω, V_S = ± 15 V)	$V_{Q\ pp}$	14.9		−12.5	14.8	−12.0	V
(R_L = 2 kΩ, V_S = ± 15 V, f = 100 kHz)	$V_{Q\ pp}$		± 10				V

Characteristics
$V_S = \pm 5$ V to ± 15 V

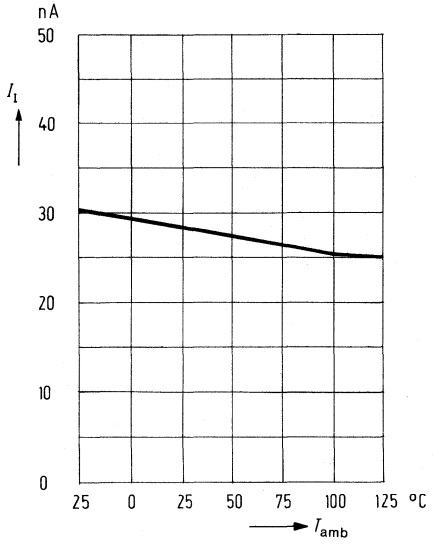
		$T_{amb} = 25$ °C			$T_{amb} = -25$ to 85 °C		
		min	typ	max	min	max	
Input impedance ($f = 1$ kHz)	Z_i		3				MΩ
Open-loop voltage gain							
($R_L = 2$ kΩ, $f = 1$ kHz)	G_{V0}	75	80		75		dB
($R_L = 10$ kΩ, $f = 1$ kHz)	G_{V0}		85				dB
($R_L = 2$ kΩ, $f = 1$ MHz)	G_{V0}		43				dB
Common-mode input voltage range ($R_L = 2$ kΩ, $V_S = \pm 15$ V)	V_{IC}	13		−13	12	−12	V
Common-mode rejection ($R_L = 2$ kΩ)	k_{CMR}	70	78		70		dB
Supply voltage rejection ($G_V = 100$)	k_{SVR}		25	200		200	μV/V
Temperature coefficient of V_{IO} ($R_G = 50$ Ω)	α_{VIO}		12	50		50	μV/K
Temperature coefficient of I_{IO}	α_{IIO}		50				pA/K
Slew rate of V_q for non-inverting operation*) (see TAA 765 test circuit 1)	SR		9				V/μs
Slew rate of V_q for inverting operation*) (see TAA 765, test circuit 2)	SR		18				V/μs
Output saturation voltage ($I_Q = 10$ mA)	V_{Qsat}			1			V
Output reverse current	I_{QR}			10		20	μA

Characteristics
$V_S = \pm 2$ V

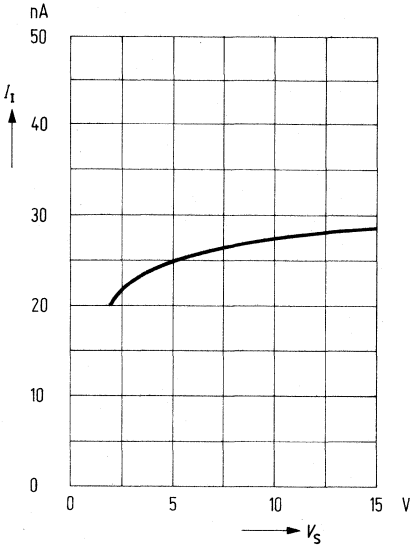
Input offset voltage ($R_G = 50$ Ω)	V_{IO}	−17		17	−20	20	mV
Input offset current	I_{IO}	−10		10	−20	20	nA
Input current	I_I		5	25		35	nA
Open-loop voltage gain ($R_L = 2$ kΩ, $f = 1$ kHz)	G_{V0}	70			70		dB

*) For the relationship between power bandwidth and slew rate refer to "General information" page 40

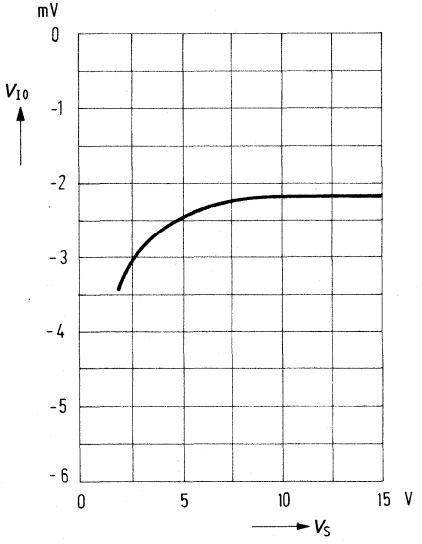
Input current versus ambient temperature
$R_L = 2\ k\Omega$



Input current versus supply voltage
$T_{amb} = 25\,°C$; $R_L = 2\ k\Omega$



Input offset voltage versus supply voltage



Type	Ordering code	Package	Color code	Fig. No.
TAE 1453 A	Q67000-A2017	DIP 6	–	5
TAE 1453 G	Q67000-A2106	similar to SO 6	blue/silver	25
TAF 1453 A	Q67000-A2269	DIP 6	–	5
TAF 1453 G	Q67000-A2209	similar to SO 6	red/red	25

The operational amplifiers are circuits for universal applications having a PNP input differential stage and an open collector output. Apart from one resistor, only active components are used. The integrated regulator provides for all parameters a large degree of independence from the supply voltage. The TAE/TAF 1453 is especially suited for applications with the following characteristics:

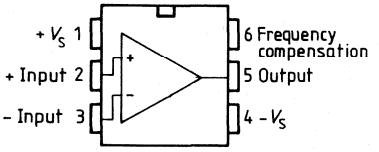
- Operation with very low supply voltages of 2 V (1.8 V)
- Direct driving of loads up to 70 mA
- Direct driving of TTL loads
- Level conversion to all logic families
- Large-signal control
- Zero detector $V_I = 0$ V or $-V_S$
- High immunity of the inputs to overvoltage surges (up to 40 V)
- Pin-compatible and functionally compatible with TAA 765

Outstanding electrical features

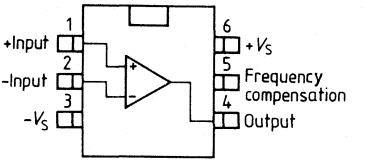
- Supply voltage range between 2 V (1.8 V) and 36 V
- Low current consumption, 0.25 mA typ.
- Extremely large control range
- Low output saturation voltage, almost independent of load current
- Very wide common-mode range, down to 0.3 V below the negative supply voltage
- Output current up to 70 mA (100 mA max.)
- Short-circuit proof output
- Very low input current
- Very low input offset voltage
- Operating temperature range of TAE 1453 A, TAE 1453 G: −25 to 85 °C
  TAF 1453 A, TAF 1453 G: −55 to 125 °C

Pin configurations

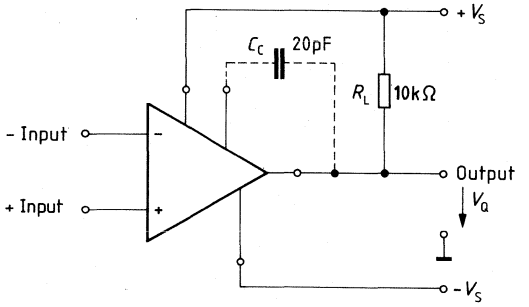
TAE 1453 A, TAF 1453 A



TAE 1453 G, TAF 1453 G

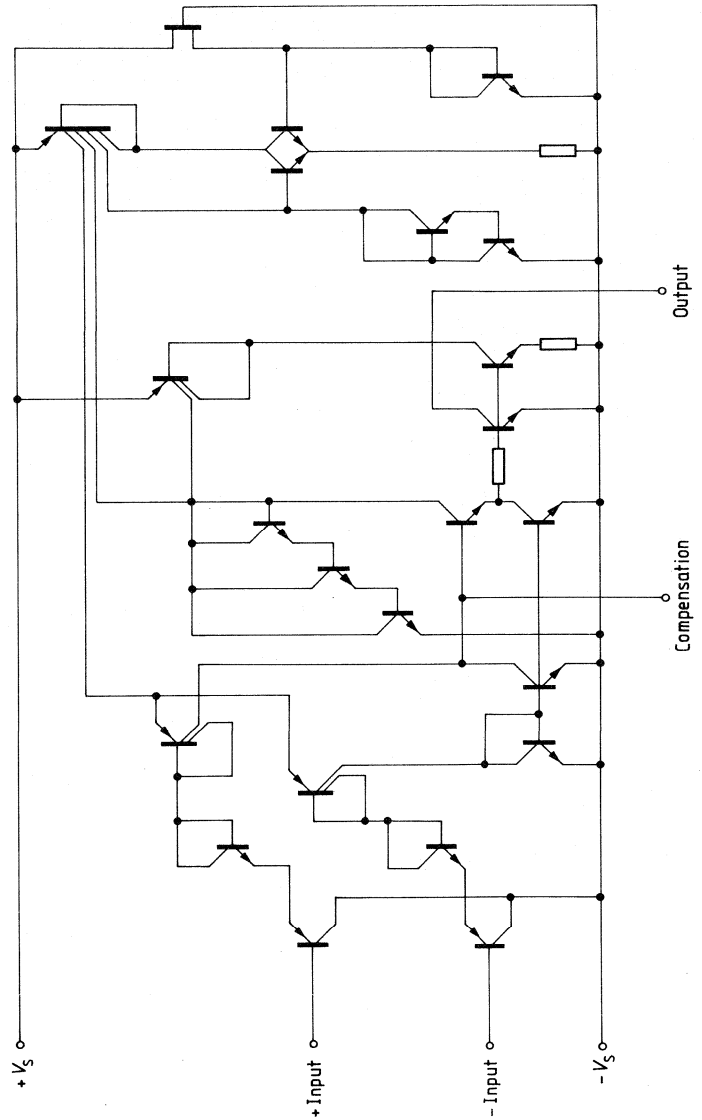


Connection diagram



C_C = output frequency compensation (if required);
R_L = load resistor

Circuit diagram



Maximum ratings

Supply voltage		V_S	± 18	V
Output current		I_Q	100	mA
Differential input voltage		V_{ID}	± V_S	V
Junction temperature		T_j	150	°C
Storage temperature range		T_{stg}	−55 to 150	°C
Thermal resistance (system-air)	TAE 1453 A	$R_{th\ SA}$	135	K/W
	TAE 1453 G	$R_{th\ SA}$	200	K/W

Operating range

Supply voltage range	V_S	± 1.0 to ± 18 (± 0.9 V with slightly increased offset voltage)	V
Ambient temperature range	T_{amb}	−25 to 85	°C

Characteristics

$V_S = \pm 5$ V to ± 15 V
$R_L = 10$ kΩ

		$T_{amb} = 25$ °C			$T_{amb} = -55$ to 85 °C		
		min	typ	max	min	max	
Open-loop current consumption (Output in H state)	I_S		0.25	0.4		0.45	mA
Input offset voltage ($R_G = 50\ \Omega$, $R_L = 2$ kΩ)	V_{IO}	−5.5		5.5	−7	7	mV
Input offset current	I_{IO}			75		100	nA
Input current	I_{IO}		40	150		200	nA
Output voltage ($R_L = 2$ kΩ, $V_S = \pm 15$ V)	V_{Qpp}	14.9		−14.7	14.8	−14.7	V
Output voltage ($R_L = 620\ \Omega$, $V_S = \pm 15$ V)	V_{Qpp}	14.9		−14.5	14.8	−14.4	V
Output voltage ($R_L = 2$ kΩ, $V_S = \pm 15$ V, $f = 100$ kHz)	V_{Qpp}	10		−10			V
Input impedance ($f = 1$ kHz)	Z_i		200				kΩ
Open-loop voltage gain	G_{V0}	78	85		78		dB
Output reverse current	I_{QR}			10		20	µA
Common-mode input voltage	V_{IC}	$-V_S$−0.2		$+V_S$−1.8	$-V_S$	$+V_S$−2.0	V
Common-mode rejection	k_{CMR}	75	80		75		dB
Supply voltage rejection ($G_V = 100$)	k_{SVR}		25	100		120	µV/V
Temperature coefficient of I_{IO}	α_{IIO}		0.1				nA/K
Temperature coefficient of V_{IO} ($R_G = 50\ \Omega$)	α_{VIO}		6				µV/K
Slew rate for non-inverting operation*)	SR		20				V/µs
Slew rate for inverting operation*)	SR		30				V/µs

Characteristics

$V_S = \pm 2$ V

Input offset voltage ($R_G = 50\ \Omega$)	V_{IO}	−6		6	−7.5	7.5	mV
Input offset current	I_{IO}			75		100	nA
Input current	I_I		40	150		200	nA
Open-loop voltage gain	G_{V0}	70			70		dB

*) For the relationship between power bandwidth and slew rate refer to "General information" page 40

Maximum ratings

Supply voltage		V_S	± 18	V
Output current		I_Q	100	mA
Differential input voltage		V_{ID}	± V_S	V
Junction temperature		T_j	150	°C
Storage temperature range		T_{stg}	−55 to 150	°C
Thermal resistance (system-air)	TAF 1453 A	$R_{th\ SA}$	135	K/W
	TAF 1453 G	$R_{th\ SA}$	200	K/W

Operating range

Supply voltage range	V_S	± 1.0 to ± 18 (± 0.9 V with slightly increased offset voltage)	V
Ambient temperature range	T_{amb}	−55 to 125	°C

Characteristics

V_S = ± 5 V to ± 15 V
R_L = 10 kΩ

		T_{amb} = 25 °C			T_{amb} = −55 to 125 °C		
		min	typ	max	min	max	
Open-loop current consumption (Output in H state)	I_S		0.25	0.35		0.45	mA
Input offset voltage (R_G = 50 Ω, R_L = 2 kΩ)	V_{IO}	−4		4	−6	6	mV
Input offset current	I_{IO}			50		75	nA
Input current	I_I		40	100		150	nA
Output voltage (R_L = 2 kΩ, V_S = ± 15 V)	V_{Qpp}	14.9		−14.7	14.8	−14.7	V
Output voltage (R_L = 620 Ω, V_S = ± 15 V)	V_{Qpp}	14.9		−14.5	14.8	−14.4	V
Output voltage (R_L = 2 kΩ, V_S = ± 15 V, f = 100 kHz)	V_{Qpp}	10		−10			V
Input impedance (f = 1 kHz)	Z_i		200				kΩ
Open-loop voltage gain	G_{V0}	80	85		80		dB
Output reverse current	I_{QR}			1		5	μA
Common-mode input voltage	V_{IC}	$-V_S$−0.3		$+V_S$−1.5	$-V_S$	$+V_S$−1.8	V
Common-mode rejection	k_{CMR}		85		75		dB
Supply voltage rejection (G_V = 100)	k_{SVR}		25	100		100	μV/V
Temperature coefficient of I_{IO}	α_{IIO}		0.1	0.8			nA/K
Temperature coefficient of V_{IO} (R_G = 50 Ω)	α_{VIO}		6	25			μV/K
Slew rate for non-inverting operation*)	SR		20				V/μs
Slew rate for inverting operation*)	SR		30				V/μs

Characteristics

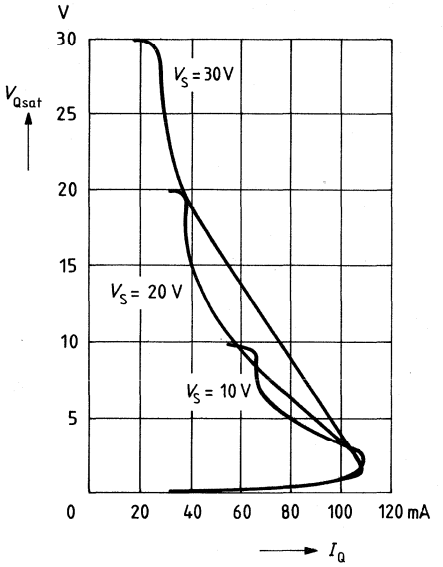
V_S = ± 2 V

Input offset voltage (R_G=50 Ω, R_L=2kΩ)	V_{IO}	−4		4	−6	6	mV
Input offset current	I_{IO}			50		75	nA
Input current	I_I		40	100		150	nA
Open-loop voltage gain (R_L = 10 kΩ)	G_{V0}	75			70		dB

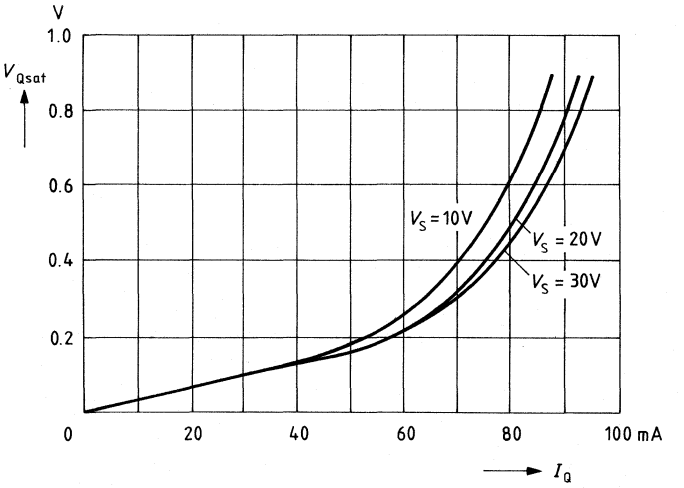
*) For the relationship between power bandwidth and slew rate refer to "General information" page 40

Typical characteristics of electrical parameters

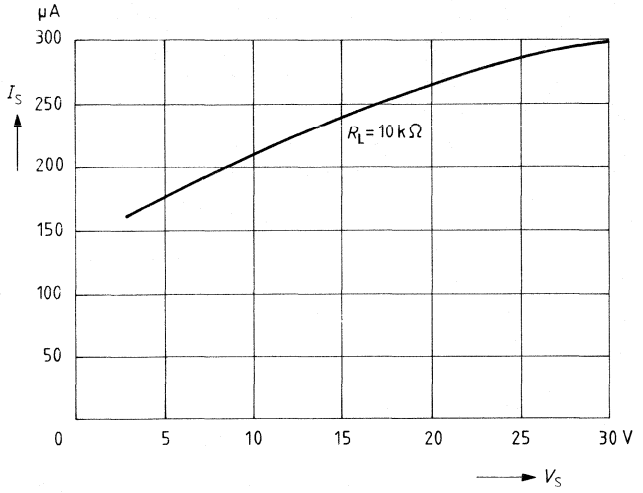
Load characteristics
Output saturation voltage versus output current



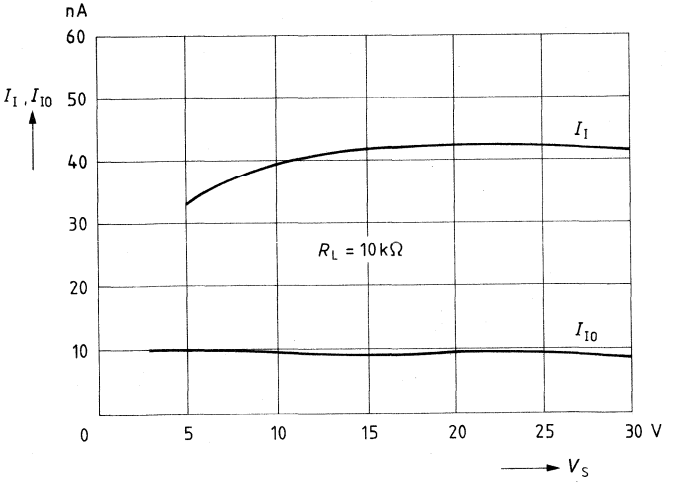
Output saturation voltage versus output current



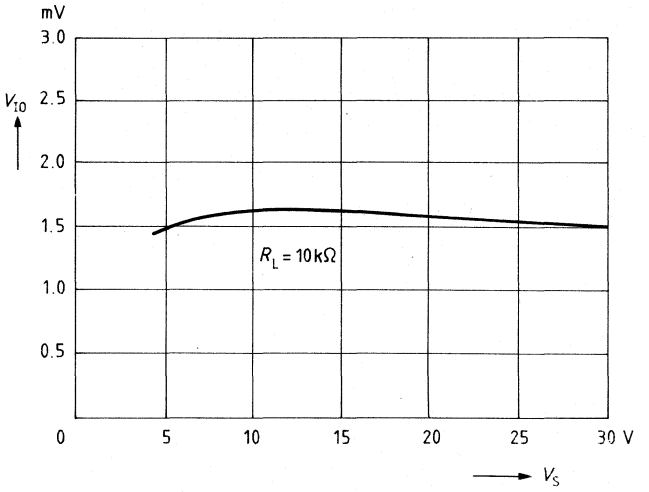
Supply current versus supply voltage



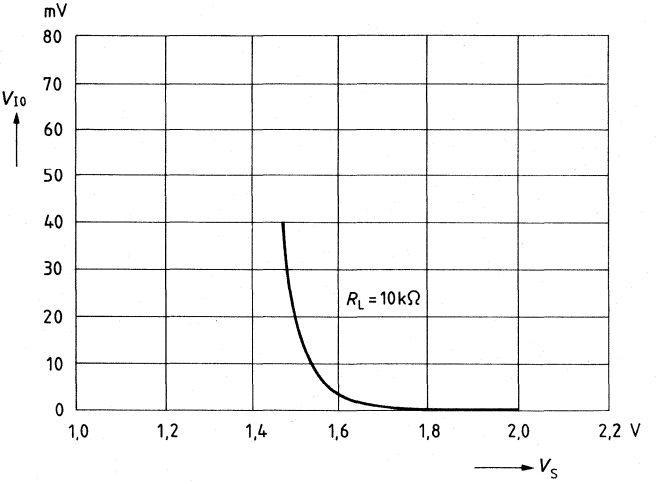
Input current and input offset current versus supply voltage



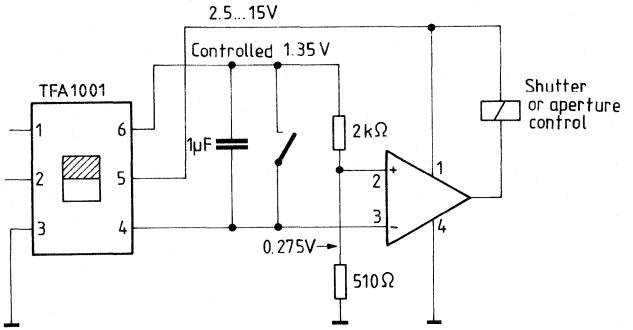
Input offset voltage versus supply voltage



V_{IO} behavior at low operating voltages
Input offset voltage versus supply voltage



Camera exposure control with TAE 1453/TAF 1453



Application example

The circuit diagram shows the TAE 1453 together with the TFA 1001 photosensor IC in an application as exposure control system. The TFA 1001 supplies an impressed output current which is directly proportional to the incident light. A constant voltage of 1.35 V is available at pin 6. In order to determine the exposure time, a capacitor is charged to the controlled 1.35 V; i.e. its potential of 1.35 V runs time-proportionally to ground. By means of the 510 Ω and 2 kΩ resistors, a reference voltage of approximately 0.275 V is set at the TAE 1453 op amp which operates as comparator in this case. Thus, a voltage which is substantially lower than with NPN op amps, is obtained. Should the voltage at the capacitor fall below 0.275 V, the shutter (or aperture) relay receives no current and drops; exposure is finished.

In this application, three features are of particular interest: the low supply voltage (< 2 V), the common-mode range down to almost 0 V (ground), as well as the low saturation voltage of the output (< 0.3 V).

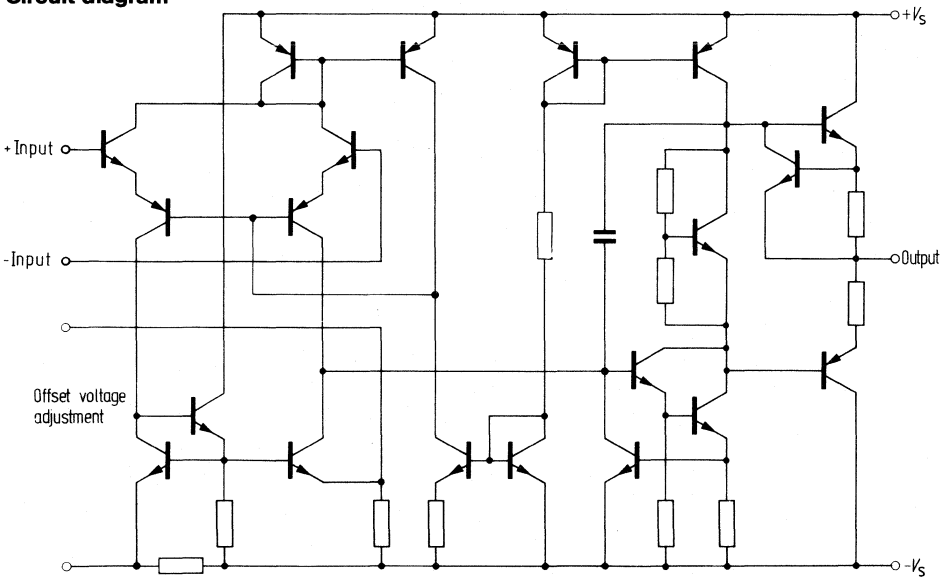
Type	Ordering code	Package	Color code	Fig. No.
TBA 221 B	Q67000-A281	DIP 8	–	6
TBA 221 G	Q67000-A923-G1	similar to SO 8	brown/brown	26
TBA 222 B	Q67000-A2280	DIP 8	–	6
TBA 222 G	Q67000-A97-G1	similar to SO 8	brown/white	26
TBB 741 G	Q67000-A1498-G1	similar to SO 8	blue/brown	26

These op amps are short-circuit proof to $+V_S$, $-V_S$, and ground. The input offset voltage can be very easily compensated. Very few external components are required due to the internal frequency compensation. The gain reduction by 6 dB/octave yields a very good stability.

Features

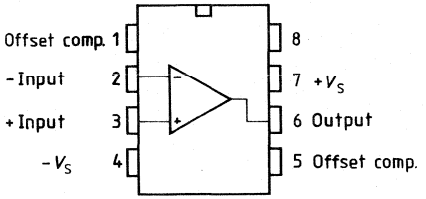
- Simple handling
- High differential input voltage
- Short-circuit proof
- High voltage gain
- High supply voltage
- Wide temperature range (TBA 222)

Circuit diagram

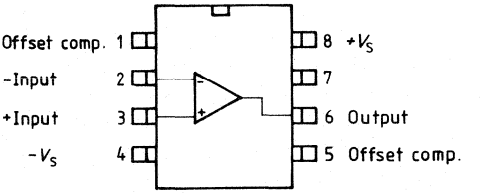


Pin configurations

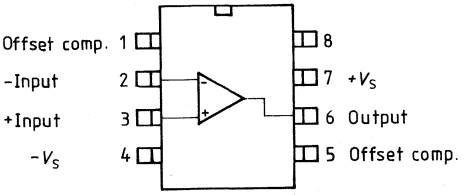
TBA 221 B; TBA 222 B



TBA 221 G, TBA 222 G



TBB 741 G



Maximum ratings

		TBA 221 TBB 741	TBA 222	
Supply voltage	V_S	± 18	± 22	V
Input voltage: V_S = ± 4 to ± 15 V	V_I	± V_S	± V_S	V
$V_S \geq$ 15 V	V_I	± 15	± 15	V
Differential input voltage	V_{ID}	± 30	± 30	V
Output short-circuit duration[1]	t_{QSC}	∞	∞	
Junction temperature	T_j	150	150	°C
Storage temperature range	T_{stg}	−55 to 125	−65 to 150	°C
Thermal resistance (system-air)				
TBA 221 B/222 B	$R_{th\ SA}$	100		K/W
TBA 221 G/222 G	$R_{th\ SA}$	200		K/W
TBB 741 G	$R_{th\ SA}$	200		K/W

Operating range

Supply voltage range	V_S	± 4 to ± 18	± 4 to ± 22	V
Ambient temperature range	T_{amb}	0 to 70	−55 to 125	°C

1) Short circuit may be to $+V_S$, $-V_S$, or 0, whereby maximum ratings like T_j must not be exceeded.

Characteristics

$V_S = \pm 15$ V

		$T_{amb} = 25$ °C			$T_{amb} = 0$ °C to 70 °C		
		min	typ	max	min	max	
Input offset voltage ($R_G \leq 10$ kΩ)	V_{IO}	−6		6	−7,5	7,5	mV
Setting range of V_{IO}	V_{IO}	6	± 15	−6			mV
Input offset current	I_{IO}	−200	± 20	200	−300	300	nA
Input current	I_I		80	500		800	nA
Supply current	I_S		1,7	2,8		2,8	mA
Pos. output short-circuit current	I_{QSC+}	15	20	25			mA
Neg. output short-circuit current	I_{QSC-}	−25	−20	−15			mA
Input resistance	R_I	300	2000				kΩ
Input capacitance	C_I		1,4				pF
Output resistance	R_Q		75				Ω
Output voltage ($R_L \geq 10$ kΩ)	V_{Qpp}	13	±14	−12,5			V
($R_L \geq 2$ kΩ)	V_{Qpp}	11	±13	−11			V
Common-mode input voltage range	V_{IC}	12	±13	−12			V
Open-loop voltage gain ($V_{Qpp} = \pm 10$ V, $R_L \geq 2$ kΩ)	G_{V0}	86	100		84		dB
Common-mode rejection ($R_G \leq 10$ kΩ)	k_{CMR}	70	90				dB
Supply voltage rejection	k_{SVR}		30	150			µV/V
Transient response of output voltage at $G_V = 1$:							
Rise time ($V_I = 20$ mV, $R_L = 2$ kΩ, $C_L \leq 100$ pF)	t_r		0,3				µs
Overshoot			5				%
Slew rate*) ($R_L \leq 2$ kΩ)	SR		0,5				V/µs
Temperature coefficient of V_{IO}	α_{VIO}		3				µV/K
Temperature coefficient of I_{IO}	α_{IIO}		0,4				nA/K

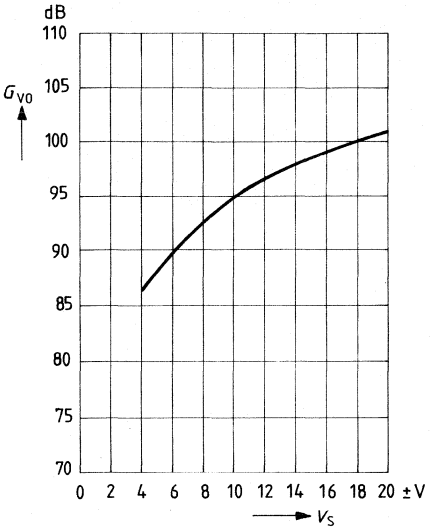
*) For the relationship between power bandwidth and slew rate refer to "General information" page 40

Characteristics
$V_S = \pm 15$ V

		$T_{amb} = 25$ °C			$T_{amb} = -55$ to 125 °C		
		min	typ	max	min	max	
Input offset voltage ($R_G \leq 10$ kΩ)	V_{IO}	−4		4	−5,5	5,5	mV
Setting range of V_{IO}	V_{IO}	6	± 15	−6			mV
Input offset current	I_{IO}	−100	± 20	100	−400	400	nA
Input current	I_I		80	350		1200	nA
Supply current	I_S		1,7	2,8		2,8	mA
Pos. output short-circuit current	I_{QSC+}	15	20	25			mA
Neg. output short-circuit current	I_{QSC-}	−25	−20	−15			mA
Input resistance	R_I	300	2000				kΩ
Input capacitance	C_I		1,4				pF
Output resistance	R_Q		75				Ω
Output voltage ($R_L \geq 10$ kΩ)	V_{Qpp}	13	±14	−12,5			V
($R_L \geq 2$ kΩ)	V_{Qpp}	11	±13	−11			V
Common-mode input voltage range	V_{IC}	12	±13	−12			V
Open-loop voltage gain ($V_{Qpp} = \pm 10$ V, $R_L \geq 2$ kΩ)	G_{V0}	94	106		88		dB
Common-mode rejection ($R_G \leq 10$ kΩ)	k_{CMR}	80	90				dB
Supply voltage rejection	k_{SVR}		30	100			µV/V
Transient response of output voltage at $G_V = 1$:							
Rise time ($V_I = 20$ mV, $R_L = 2$ kΩ, $C_L \leq 100$ pF)	t_r		0,3				µs
Overshoot			5				%
Slew rate*) ($R_L \leq 2$ kΩ)	SR		0,5				V/µs
Temperature coefficient of V_{IO}	α_{VIO}		3				µV/K
Temperature coefficient of I_{IO}	α_{IIO}		0,4				nA/K

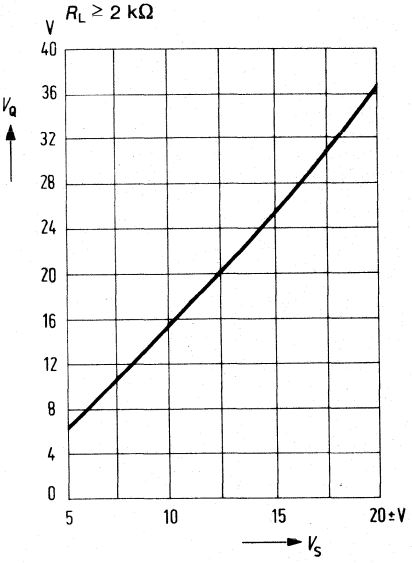
*) For the relationship between power bandwidth and slew rate refer to "General information" page 40

Open-loop voltage gain versus supply voltage



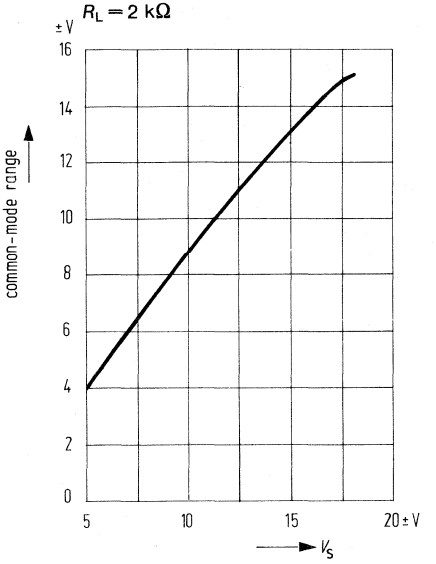
Output voltage versus supply voltage

$R_L \geq 2$ kΩ

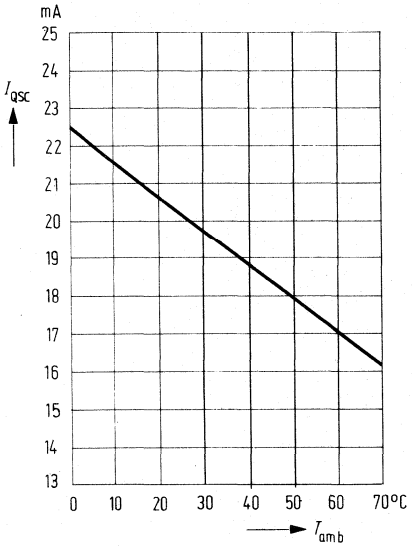


Common-mode range versus supply voltage

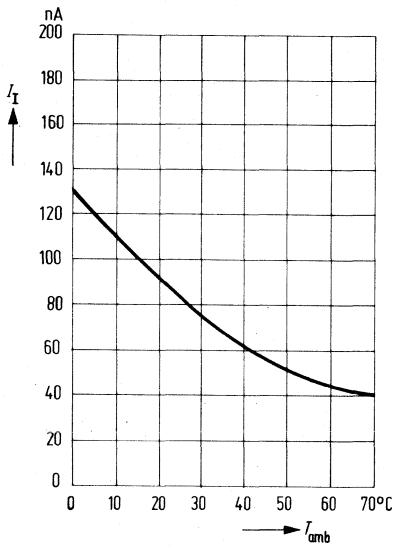
$R_L = 2$ kΩ



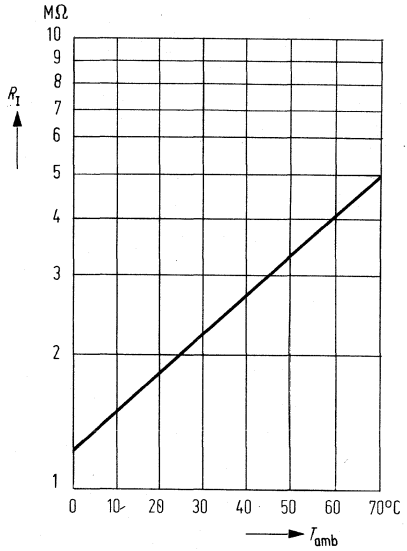
Output short-circuit current versus ambient temperature



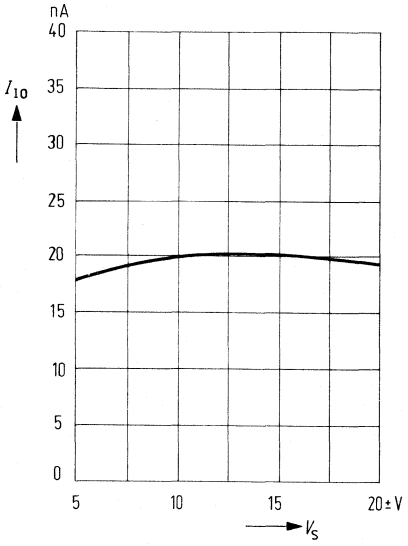
Input current versus ambient temperature
$V_S = \pm 15$ V



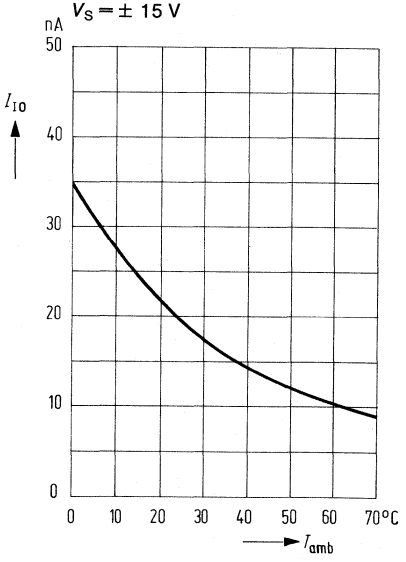
Input resistance versus ambient temperature
$V_S = \pm 15$ V



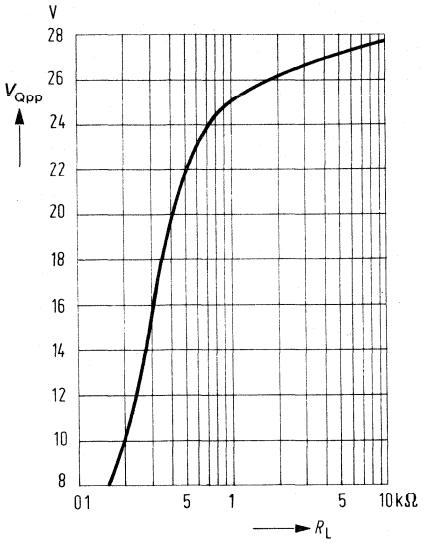
Input offset current versus supply voltage



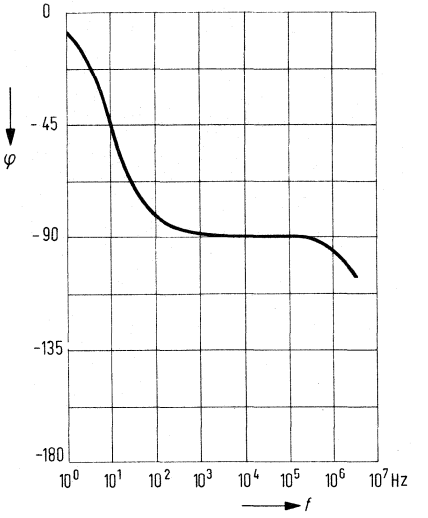
Input offset current versus ambient temperature
$V_S = \pm 15$ V



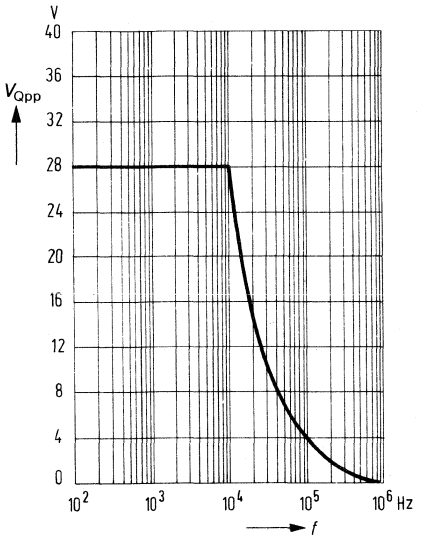
Output voltage versus load resistance
$V_S = \pm 15$ V



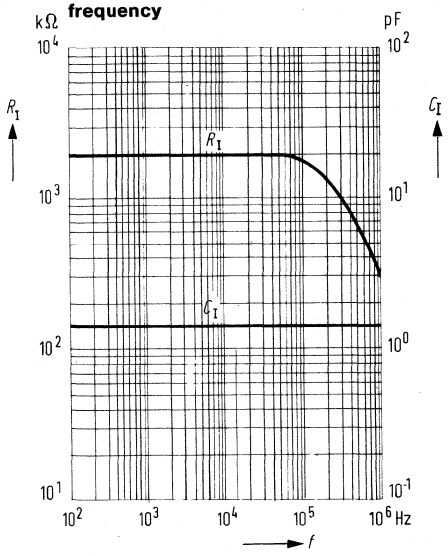
Phase response of open-loop voltage gain
Phase versus frequency
$V_S = \pm 15$ V



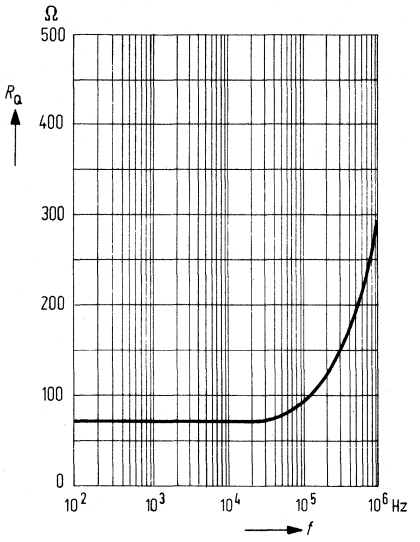
Output voltage versus frequency
$V_S = \pm 15$ V; $R_L = 10$ kΩ



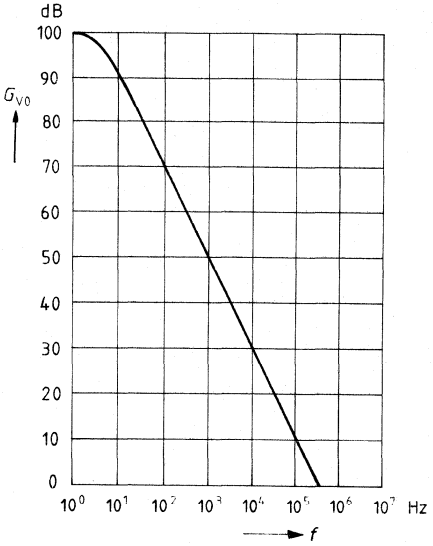
Input resistance and input capacitance versus frequency



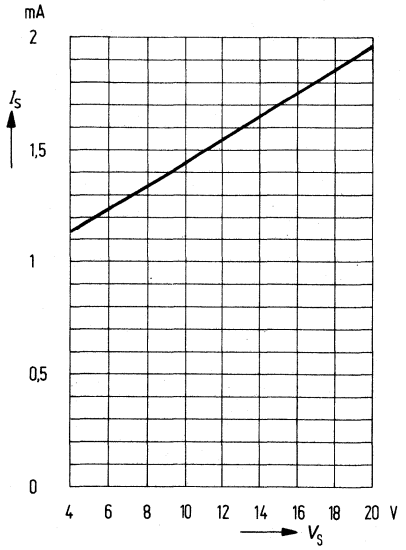
Output resistance versus frequency



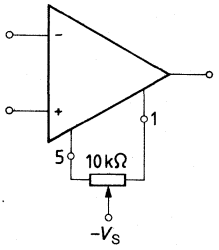
Open-loop voltage gain versus frequency



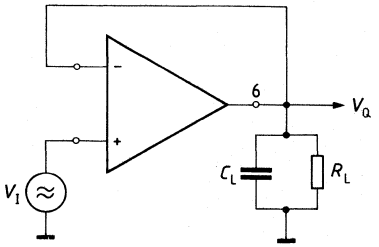
Supply current versus supply voltage



Offset voltage adjustment circuit



Transient response



Dual Operational Amplifiers

Type	Ordering code	Package	Fig. No.
TAA 2762 A	Q67000-A2499	DIP 8	6
TAA 2765 A	Q67000-A1031	DIP 8	6

Particularly economic and versatile op amps. Owing to their excellent performance qualities they are well suited for a wide scope of applications, as in control engineering, automotive electronics, AF circuits, analog computers, etc.

In addition to high gain, high input resistance, low offset voltage, minor dependence on temperature and supply voltage, the amplifiers, are outstanding for:

- Wide common-mode range
- Large supply voltage range
- Wide temperature range (TAA 2762 A)
- High output current
- Large control range
- No frequency compensation

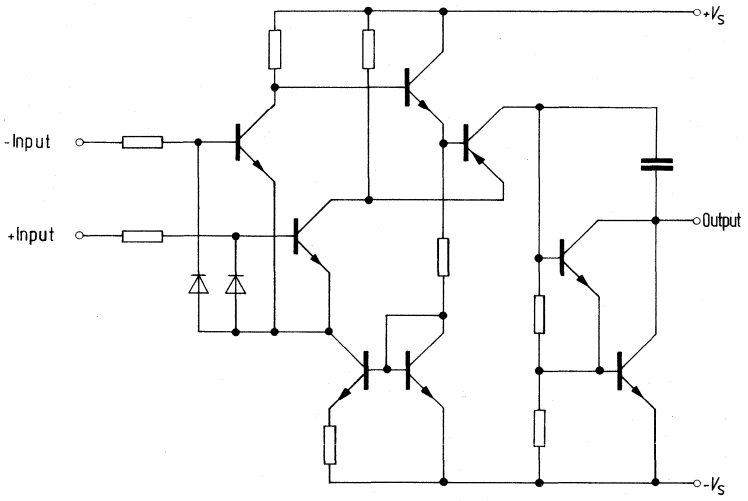
Maximum ratings

Supply voltage	V_S	± 15	V
Output current	I_Q	70	mA
Differential input voltage	V_{ID}	± V_S	
Junction temperature	T_j	150	°C
Storage temperature range	T_{stg}	−55 to 125	°C
Thermal resistance (system-air)	$R_{th\ SA}$	100	K/W

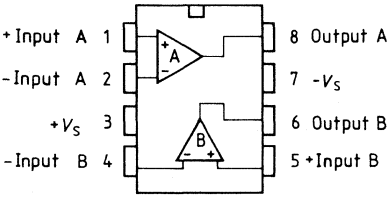
Operating range

Supply voltage range	V_S	± 2 to ± 15	V
Ambient temperature range			
TAA 2762 A	T_{amb}	−55 to 125	°C
TAA 2765 A	T_{amb}	−25 to 85	°C

Circuit diagram of a single op amp



Pin configuration



Characteristics
$V_S = \pm 5$ V to ± 15 V

		$T_{amb} = 25$ °C			$T_{amb} = -55$ to 125 °C		
		min	typ	max	min	max	
Open-loop supply current consumption, total	I_S		0,5	1.5		1.5	mA
Input offset voltage ($R_G = 50\ \Omega$)	V_{IO}	−4		4	−6	6	mV
Input offset current	I_{IO}	−100	±50	100	−300	300	nA
Input current	I_I		0.3	0.7		1.0	µA
Output voltage							
($R_L = 2$ kΩ, $V_S = \pm 15$ V)	V_{Qpp}	14.9		−14	14,8	−14	V
($R_L = 620\ \Omega$, $V_S = \pm 15$ V)	V_{Qpp}	14.9		−12.5	14,8	−12	V
Input impedance ($f = 1$ kHz)	Z_i		200				kΩ
Open-loop voltage gain							
($R_L = 2$ kΩ, $f = 100$ Hz)	G_{V0}	85	87		80		dB
($R_L = 10$ kΩ, $f = 100$ Hz)	G_{V0}		92				dB
Output reverse current	I_{QR}			1		5	µA
Common-mode input voltage range ($R_L = 2$ kΩ, $V_S = \pm 15$ V)	V_{IC}	13	±13.5	−13	12	−12	V
Common-mode rejection ($R_L = 2$ kΩ)	k_{CMR}	80	85			75	dB
Supply voltage rejection ($G_V = 100$)	k_{SVR}		25	100		100	µV/V
Temperature coefficient of V_{IO} ($R_G = 50\ \Omega$)	α_{VIO}		6	25		25	µV/K
Temperature coefficient of I_{IO} ($R_G = 50\ \Omega$)	α_{IIO}		0,3	1.5		1.5	nA/K
Noise voltage (in acc. with DIN 45405; referred to input; $R_S = 2.5$ kΩ)	V_n		3				µV
Output saturation voltage ($I_Q = 10$ mA)	V_{Qsat}			1			V
Slew rate for non-inverting operation*)	SR		0,5				V/µs
Slew rate for inverting operation*)	SR		0,5				V/µs

Characteristics
$V_S = \pm 2$ V

Input offset voltage	V_{IO}	−4		4	−6	6	mV
Input offset current	I_{IO}	−70		70	−200	200	nA
Input current	I_I		0,2	0.5		0.8	µA
Open-loop voltage gain ($R_L = 2$ kΩ, $f = 100$ Hz)	G_{V0}	80			75		dB

*) For the relationship between power bandwidth and slew rate refer to "General information" page 40

Characteristics
$V_S = \pm 5$ V to ± 15 V

		$T_{amb} = 25$ °C			$T_{amb} = -25$ to 85 °C		
		min	typ	max	min	max	
Open-loop supply current consumption, total	I_S		0,5	1.5		1.5	mA
Input offset voltage ($R_G = 50\ \Omega$)	V_{IO}	−5.5		5.5	−7	7	mV
Input offset current	I_{IO}	−200	±80	200	−300	300	nA
Input current	I_I		0.5	0.8		1.0	µA
Output voltage ($R_L = 2$ kΩ, $V_S = \pm 15$ V)	V_{Qpp}	14.9		−14	14.8	−14	V
($R_L = 620\ \Omega$, $V_S = \pm 15$ V)	V_{Qpp}	14.9		−12.5	14.8	−12	V
Input impedance ($f = 1$ kHz)	Z_i		200				kΩ
Open-loop voltage gain ($R_L = 2$ kΩ, $f = 100$ Hz)	G_{V0}	80	85		80		dB
($R_L = 10$ kΩ, $f = 100$ Hz)	G_{V0}		90				dB
Output reverse current	I_{QR}			10		20	µA
Common-mode input voltage range ($R_L = 2$ kΩ, $V_S = \pm 15$ V)	V_{IC}	13	±13.5	−13	12	−12	V
Common-mode rejection ($R_L = 2$ kΩ)	k_{CMR}	75	83		75		dB
Supply voltage rejection ($G_V = 100$)	k_{SVR}		25	100		100	µV/V
Temperature coefficient of V_{IO} ($R_G = 50\ \Omega$)	α_{VIO}		6			25	µV/K
Temperature coefficient of I_{IO} ($R_G = 50\ \Omega$)	α_{IIO}		0,3			1.5	nA/K
Noise voltage (in acc. with DIN 45405; referred to input; $R_S = 2.5$ kΩ)	V_n		3				µV
Output saturation voltage ($I_Q = 10$ mA)	V_{Qsat}			1			V
Slew rate for non-inverting operation*)	SR		0,5				V/µs
Slew rate for inverting operation*)	SR		0,5				V/µs

Characteristics
$V_S = \pm 2$ V

Input offset voltage	V_{IO}	−6		6	−7,5	7,5	mV
Input offset current	I_{IO}	−150		150	−200	200	nA
Input current	I_I		0,2	0,6		0,8	µA
Open-loop voltage gain ($R_L = 2$ kΩ, $f = 100$ Hz)	G_{V0}	75			75		dB

*) For the relationship between power bandwidth and slew rate refer to "General information" page 40

Dual Operational Amplifiers with Darlington Input

TBC 2332 B
TBE 2335 B

Bipolar IC

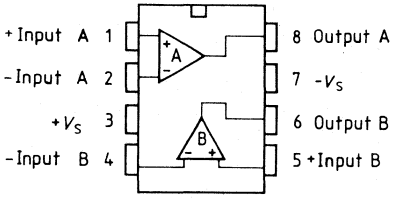
Type	Ordering code	Package	Fig. No.
TBC 2332 B	Q67000-A2500	DIP 8	6
TBE 2335 B	Q67000-A1165	DIP 8	6

Economic and versatile op amps. Owing to their excellent performance qualities, they are well suited for a wide scope of applications, as in measurement and control engineering, automotive electronics, AF circuits, analog computers, etc. The low input current of these amplifiers is particularly advantageous for measurement and control systems.

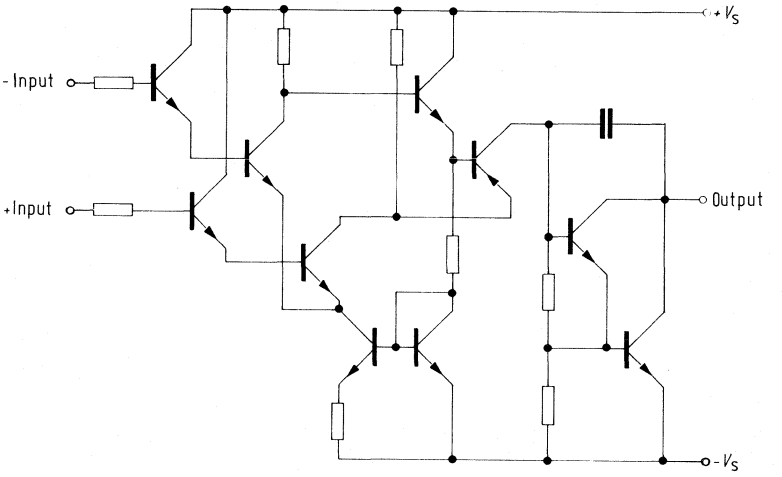
In addition to high gain, low offset voltage, minor dependence on temperature and supply voltage, the amplifiers are outstanding for:

- High input resistance
- Wide common-mode range
- Large supply voltage range
- Large control range
- High output current
- Wide temperature range (TBC 2332 B)

Pin configuration



Circuit diagram of a single op amp



Maximum ratings

Supply voltage	V_S	± 15	V
Output current	I_Q	70	mA
Differential input voltage			
(V_S = ± 13 to ± 15 V)	V_{ID}	± 13	V
(V_S = ± 2 to ± 13 V)	V_{ID}	± V_S	
Junction temperature	T_j	150	°C
Storage temperature range	T_{stg}	−55 to 125	°C
Thermal resistance (system-air)	$R_{th\ SA}$	100	K/W

Operating range

Supply voltage range	V_S	± 2 to ± 15	V
Ambient temperature range	T_{amb}	−55 to 125	°C

Characteristics

V_S = ± 5 V to ± 15 V

		T_{amb} = 25 °C			T_{amb} = −55 to 125 °C		
		min	typ	max	min	max	
Open-loop supply current consumption, total	I_S		0.5	1.5		1.5	mA
Input offset voltage (R_G = 50 Ω)	V_{IO}	−10		10	−15	15	mV
Input offset current	I_{IO}	−5		5	−10	10	nA
Input current	I_I		5	15		25	nA
Output voltage							
(R_L = 2 kΩ, V_S = ± 15 V)	$V_{Q\ pp}$	14.9		−14	14.8	−14	V
(R_L = 620 Ω, V_S = ± 15 V)	$V_{Q\ pp}$	14.9		−12.5	14.8	−12	V

Characteristics
$V_S = \pm 5$ V to ± 15 V

		$T_{amb} = 25$ °C			$T_{amb} = -55$ to 125 °C		
		min	typ	max	min	max	
Input impedance ($f = 1$ kHz)	Z_i		3				MΩ
Open-loop voltage gain							
($R_L = 2$ kΩ, $f = 100$ Hz)	G_{V0}	85	87		80		dB
($R_L = 10$ kΩ, $f = 100$ Hz)	G_{V0}		92				dB
Output reverse current	I_{QR}			1		5	µA
Common-mode input voltage range ($R_L = 2$ kΩ, comparator operation)	V_{IC}	$+V_S$		$-V_S+2.0$	$+V_S$	$-V_S+3$	V
Common-mode rejection ($R_L = 2$ kΩ)	k_{CMR}	80	85		75		dB
Supply voltage rejection ($G_V = 100$)	k_{SVR}		25	100		100	µV/V
Temperature coefficient of V_{IO} ($R_G = 50$ Ω)	α_{VIO}		12	50		50	µV/K
Temperature coefficient of I_{IO} ($R_G = 50$ Ω)	α_{IIO}		50				pA/K
Output saturation voltage ($I_Q = 10$ mA)	$V_{Q\,sat}$			1			V
Slew rate for non-inverting operation*)	SR		0.5				V/µs
Slew rate for inverting operation*)	SR		0.5				V/µs

Characteristics
$V_S = \pm 2$ V

Input offset voltage	V_{IO}	−10		10	−15	15	mV
Input offset current	I_{IO}	−5		5	−10	10	nA
Input current	I_I		5	15		25	nA
Open-loop voltage gain ($R_L = 2$ kΩ, $f = 100$ Hz)	G_{V0}	80			75		dB

*) For the relationship between power bandwidth and slew rate refer to "General information" page 40

Maximum ratings

Supply voltage	V_S	± 15	V
Output current	I_Q	70	mA
Differential input voltage			
(V_S = ± 13 to ± 15 V)	V_{ID}	± 13	V
(V_S = ± 2 to ± 13 V)	V_{ID}	± V_S	
Junction temperature	T_j	150	°C
Storage temperature range	T_{stg}	−55 to 125	°C
Thermal resistance (system-air)	$R_{th\ SA}$	100	K/W

Operating range

Supply voltage range	V_S	± 2 to ± 15	V
Ambient temperature range	T_{amb}	−25 to 85	°C

Characteristics

V_S = ± 5 V to ± 15 V

		T_{amb} = 25 °C			T_{amb} = −25 to 85 °C		
		min	typ	max	min	max	
Open-loop supply current consumption, total	I_S		0.5	1.5		1.5	mA
Input offset voltage (R_G = 50 Ω)	V_{IO}	−15		15	−18	18	mV
Input offset current	I_{IO}	−10		10	−20	20	nA
Input current	I_I		5	25		35	nA
Output voltage							
(R_L = 2 kΩ, V_S = ± 15 V)	$V_{Q\ pp}$	14.9		−14	14.8	−14	V
(R_L = 620 Ω, V_S = ± 15 V)	$V_{Q\ pp}$	14.9		−12.5	14.8	−12	V

Characteristics
$V_S = \pm 5$ V to ± 15 V

		$T_{amb} = 25$ °C			$T_{amb} = -25$ to 85 °C		
		min	typ	max	min	max	
Input impedance ($f = 1$ kHz)	Z_i		3				MΩ
Open-loop voltage gain							
($R_L = 2$ kΩ, $f = 100$ Hz)	G_{V0}	80	85		80		dB
($R_L = 10$ kΩ, $f = 100$ Hz)	G_{V0}		90				dB
Output reverse current	I_{QR}			10		20	µA
Common-mode input voltage range ($R_L = 2$ kΩ, comparator operation)	V_{IC}	$+V_S$-0.5		$-V_S$+2.0	$+V_S$-0.8	$-V_S$+3	V
Common-mode rejection ($R_L = 2$ kΩ)	k_{CMR}	75	83		75		dB
Supply voltage rejection ($G_V = 100$)	k_{SVR}		25	100		100	µV/V
Temperature coefficient of V_{IO} ($R_G = 50$ Ω)	α_{VIO}		12			50	µV/K
Temperature coefficient of I_{IO} ($R_G = 50$ Ω)	α_{IIO}		50				pA/K
Output saturation voltage ($I_Q = 10$ mA)	$V_{Q\,sat}$			1			V
Slew rate for non-inverting operation*)	SR		0.5				V/µs
Slew rate for inverting operation*)	SR		0.5				V/µs

Characteristics
$V_S = \pm 2$ V

Input offset voltage	V_{IO}	−17		17	−20	20	mV
Input offset current	I_{IO}	−10		10	−20	20	nA
Input current	I_I		5	25		35	nA
Open-loop voltage gain ($R_L = 2$ kΩ, $f = 100$ Hz)	G_{V0}	75			75		dB

*) For the relationship between power bandwidth and slew rate refer to "General information" page 40

Type	Ordering code	Package	Color code	Fig. No.
TAE 2453 A	Q67000-A2107	DIP 8	–	6
TAE 2453 G	Q67000-A2108	similar to SO-8	white	26
TAF 2453 A	Q67000-A2210	DIP 8	–	6
TAF 2453 G	Q67000-A2209	similar to SO-8	green	26

The TAF 2453/TAE 2453 consists of two independent, frequency-compensated op amps, each having a PNP input differential stage and an open collector output. The integrated regulator provides for all parameters a large degree of independence of the supply voltage. The component is especially suited for applications with the following characteristics:

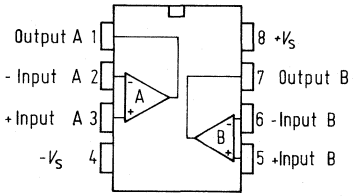
- Operation with very low supply voltages of 2 V (1.8 V)
- Direct driving of loads up to 70 mA
- Direct driving of TTL loads
- Level conversion to all logic families
- Large-signal control
- Zero detector $V_I = 0$ V or $-V_S$
- High immunity of the inputs to overvoltage surges (up to 40 V)

Outstanding electrical features

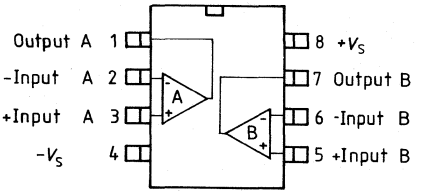
- Supply voltage range between 2 V (1.8 V) and 36 V
- Low current consumption, 0.8 mA typ.
- Extremely large control range
- Low output saturation voltage, virtually independent of load current
- Very wide common-mode range, down to 0.3 V below the negative supply voltage
- Output current up to 70 mA (100 mA max.)
- Short-circuit proof output
- Very low input current
- Very low input offset voltages
- Operating temperature range of TAE 2453 A; G: −25 °C to + 85 °C
  TAF 2453 A; G −55 °C to + 125 °C

Pin configurations

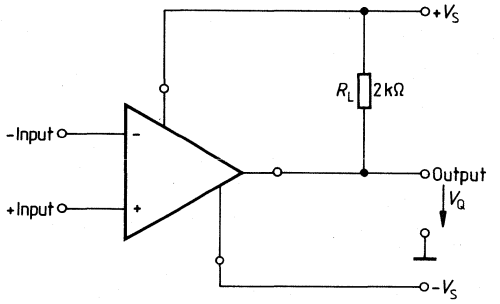
TAE 2453 A; TAF 2453 A



TAE 2453 G; TAF 2453 G

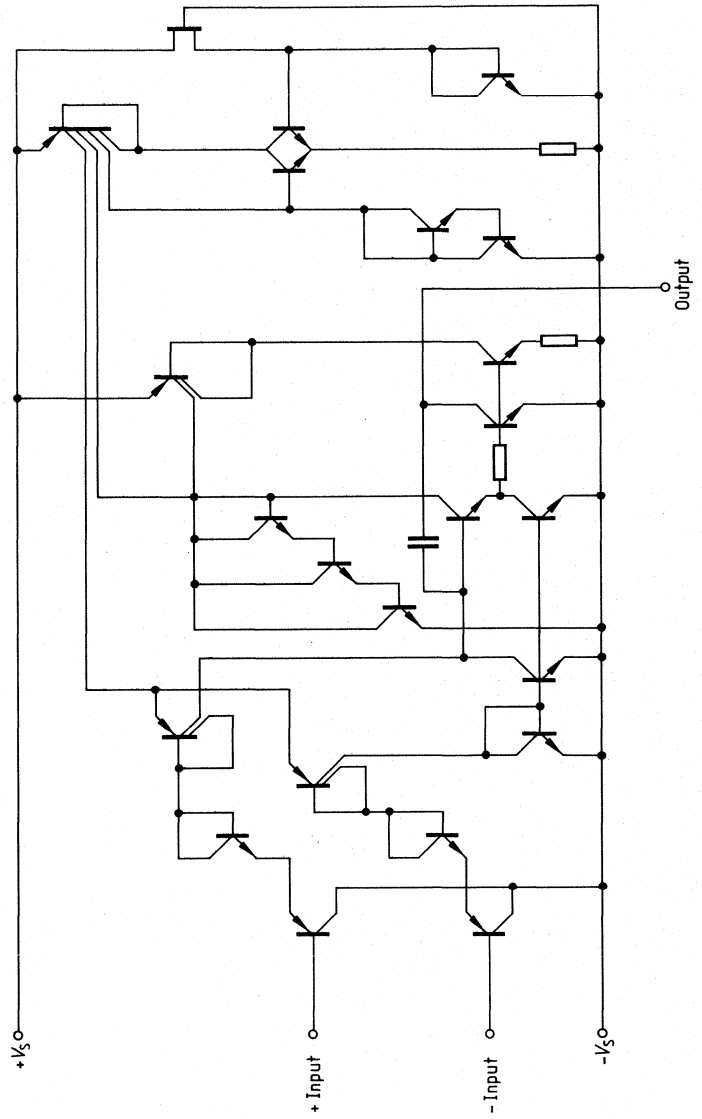


Connection diagram



R_L = load resistor

Circuit diagram



Maximum ratings

Supply voltage	V_S	± 18	V
Output current	I_Q	100	mA
Differential input voltage	V_{ID}	± V_S	V
Junction temperature	T_j	150	°C
Storage temperature range	T_{stg}	−55 to 150	°C
Thermal resistance (system-air) TAE 2453 A	$R_{th\ SA}$	100	K/W
TAE 2453 G	$R_{th\ SA}$	170	K/W

Operating range

Supply voltage range	V_S	± 1.0 to ± 18 (± 0.9 V with slightly increased offset voltage)	V
Ambient temperature range	T_{amb}	−25 to 85	°C

Characteristics

$V_S = \pm 5$ V to ± 15 V

		$T_{amb} = 25$ °C			$T_{amb} = -25$ to 85 °C		
		min	typ	max	min	max	
Open-loop supply current consumption (Outputs in H state)	I_S		0.8	1.5		1.8	mA
Input offset voltage ($R_G = 50\ \Omega$)	V_{IO}	−5.5		5.5	−7	7	mV
Input offset current	I_{IO}			75		100	nA
Input current	I_I		40	150		200	nA
Output voltage ($R_L = 2$ kΩ, $V_S = \pm 15$ V)	$V_{Q\ pp}$	14.9		−14.7	14.8	−14.7	V
Output voltage ($R_L = 620\ \Omega$, $V_S = \pm 15$ V)	$V_{Q\ pp}$	14.9		−14.5	14.8	−14.4	V
Input impedance ($f = 1$ kHz)	Z_i		200				kΩ
Open-loop voltage gain ($R_L = 2$ kΩ)	G_{V0}	80	85		80		dB
Output reverse current	I_{QR}			10		20	µA
Common-mode input voltage range ($R_L = 2$ kΩ)	V_{IC}	$-V_S$−0.2		$+V_S$−1.8	$-V_S$	$+V_S$−2.0	V
Common-mode rejection ($R_L = 2$ kΩ)	k_{CMR}	75	80		75		dB
Supply voltage rejection ($G_V = 100$)	k_{SVR}		25	100		100	µV/V
Temperature coefficient of I_{IO}	α_{IIO}		0.1				nA/K
Temperature coefficient of V_{IO} ($R_G = 50\ \Omega$)	α_{VIO}		6				µV/K
Slew rate for non-inverting operation*)	SR		1				V/µs
Slew rate for inverting operation*)	SR		1				V/µs

Characteristics

$V_S = \pm 2$ V

Input offset voltage ($R_G = 50\ \Omega$)	V_{IO}	−6		6	−7.5	7.5	mV
Input offset current	I_{IO}			75		100	nA
Input current	I_I		40	150		200	nA
Open-loop voltage gain ($R_L = 2$ kΩ)	G_{V0}	70			70		dB

*) For the relationship between power bandwidth and slew rate refer to "General information" page 40

Maximum ratings

Supply voltage	V_S	± 18	V
Output current	I_Q	100	mA
Differential input voltage	V_{ID}	± V_S	V
Junction temperature	T_j	150	°C
Storage temperature range	T_{stg}	−55 to 150	°C
Thermal resistance (system-air) TAF 2453 A	$R_{th\ SA}$	100	K/W
TAF 2453 G	$R_{th\ SA}$	170	K/W

Operating range

Supply voltage range	V_S	± 1.0 to ± 18 (± 0.9 V with slightly increased offset voltage)	V
Ambient temperature range	T_{amb}	− 55 to 125	°C

Characteristics

$V_S = \pm 5$ V to ± 15 V

		T_{amb} = 25 °C			T_{amb} = −55 to 125 °C		
		min	typ	max	min	max	
Open-loop supply current consumption (Outputs in H state)	I_S		0.8	1.5		1.8	mA
Input offset voltage (R_G = 50 Ω)	V_{IO}	−4		4	−6	6	mV
Input offset current	I_{IO}				50	75	nA
Input current	I_I		40	100		150	nA
Output voltage (R_L = 2 kΩ, V_S = ± 15 V)	$V_{Q\ pp}$	14.9		−14.7	14.8	−14.7	V
Output voltage (R_L = 620 Ω, V_S = ± 15 V)	$V_{Q\ pp}$	14.9		−14.5	14.8	−14.4	V
Input impedance (f = 1 kHz)	Z_i		200				kΩ
Open-loop voltage gain (R_L = 2 kΩ)	G_{V0}	85	87		80		dB
Output reverse current	I_{QR}			1		5	µA
Common-mode input voltage range (R_L = 2 kΩ)	V_{IC}	$-V_S$-0.3		$+V_S$-1.5	$-V_S$	$+V_S$-1.8	V
Common-mode rejection (R_L = 2 kΩ)	k_{CMR}	80	85		75		dB
Supply voltage rejection (G_V = 100)	k_{SVR}		25	100		100	µV/V
Temperature coefficient of I_{IO}	α_{IIO}		0.1	0.8		0.8	nA/K
Temperature coefficient of V_{IO} (R_G = 50 Ω)	α_{VIO}		6	25		25	µV/K
Slew rate for non-inverting operation*)	SR		1				V/µs
Slew rate for inverting operation*)	SR		1				V/µs

Characteristics

$V_S = \pm 2$ V

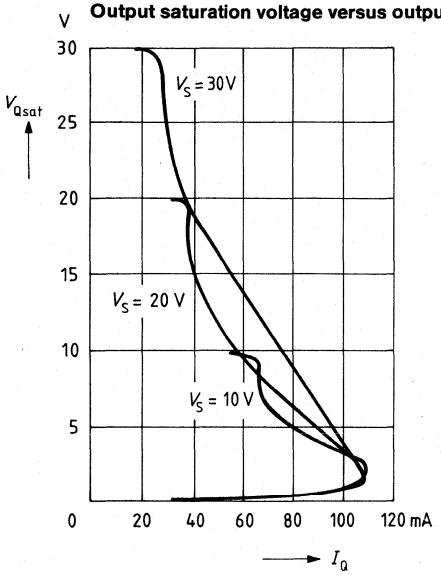
Input offset voltage (R_G = 50 Ω)	V_{IO}	−4		4	−6	6	mV
Input offset current	I_{IO}			50		75	nA
Input current	I_I		40	100		150	nA
Open-loop voltage gainΩ (R_L = 2 kΩ)	G_{V0}	75			70		dB

*) For the relationship between power bandwidth and slew rate refer to "General information" page 40

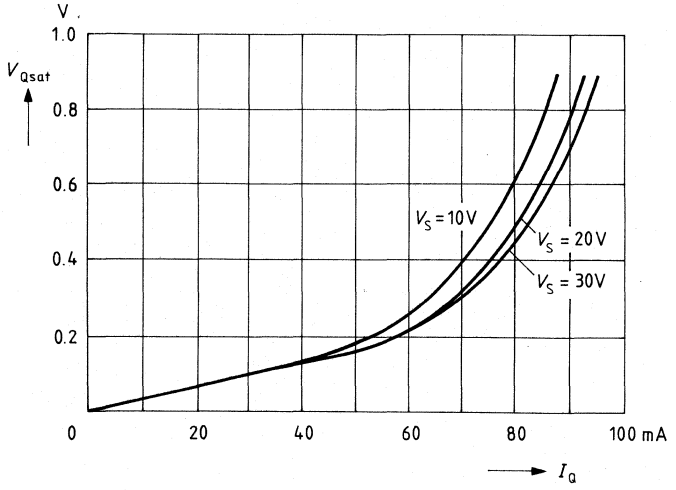
Typical characteristics of electrical parameters

Load characteristic

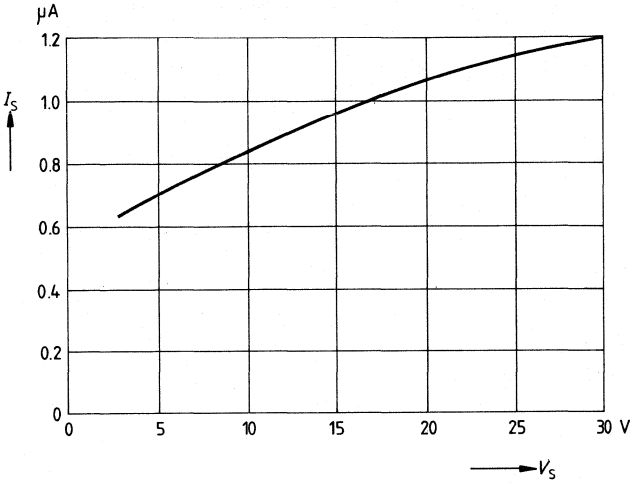
Output saturation voltage versus output current



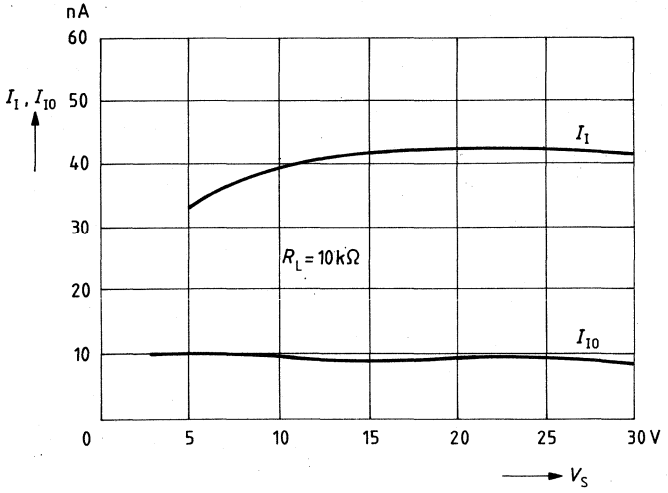
Output saturation voltage versus output current



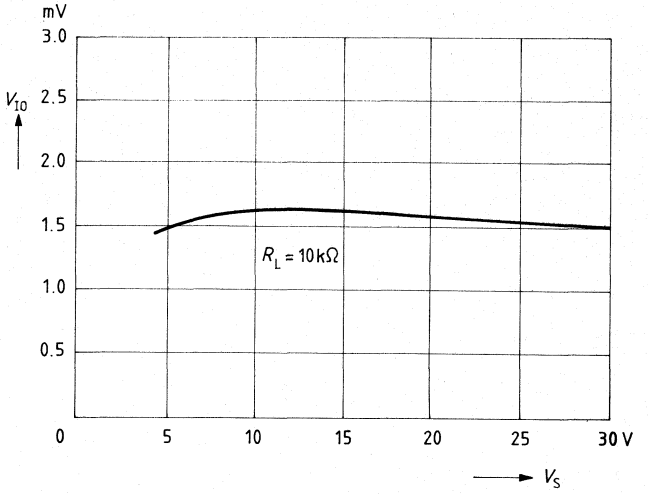
Supply current versus supply voltage



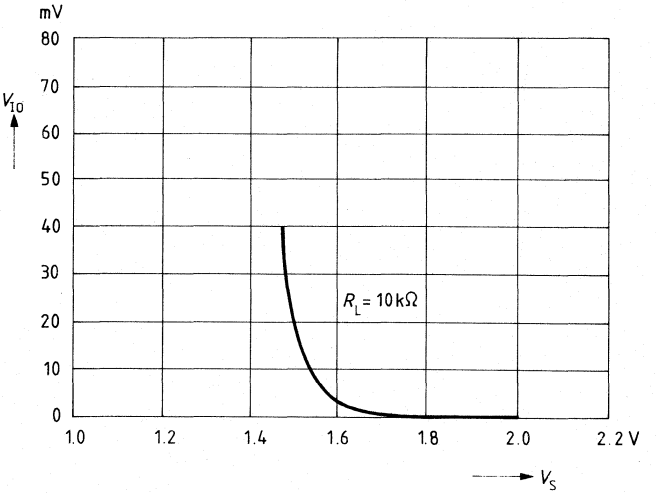
Input current and input offset current versus supply voltage



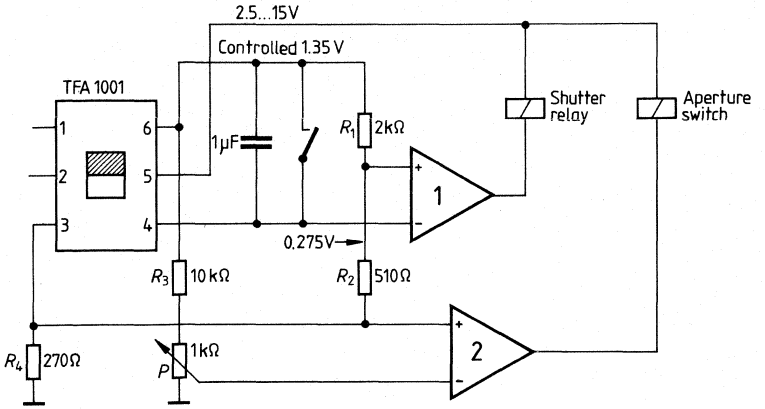
Input offset voltage versus supply voltage



V_{IO} behavior at low operating voltages
Input offset voltage versus supply voltage



Camera exposure control with TAE 2453/TAF 2453



Application example

The circuit diagram shows the TAE 2453 together with the TFA 1001 photosensor IC in an application as exposure control system. The TFA 1001 supplies an impressed output current which is directly proportional to the incident light. A constant voltage of 1.35 V is available at pin 6. In order to determine the exposure time, a capacitor is charged to the controlled 1.35 V; i.e. its potential of 1.35 V runs time-proportionally to ground. By means of the 510 Ω and 2 kΩ resistances, a reference voltage of approximately 0.275 V is set at the op amp 1 which operates as comparator in this case. Thus, a voltage which is substantially lower than with NPN op amps, is obtained. Should the voltage at the capacitor fall below 0.275 V, the shutter (or aperture) relay receives no current and drops; exposure is finished.

Comparator 2 compares the voltage drop at R_4, caused by the light-dependent current consumption, with a reference voltage set by potentiometer P, and actuates the aperture switch.

In this application, three features are of particular interest: the low supply voltage (< 2 V), the common-mode range down to almost 0 V (ground), as well as the low saturation voltage of the output (< 0.3 V).

Bipolar IC

Type	Ordering code	Package	Color code	Fig. No.
TBB 1458 B	Q67000-A1036	DIP 8	–	6
TBB 1458 G	Q67000-A1485-G1	similar to SO 8	orange/orange	26

The op amp TBB 1458 is outstanding for its large common-mode and differential input voltage range, as well as its short-circuit strength. No external components are required for frequency compensation.

For single amplifier performance refer to the TBA 221 data sheet.

Maximum ratings

Supply voltage	V_S	± 18	V
Input voltage[1]	V_I	± 15	V
Differential input voltage[2]	V_{ID}	± 30	V
Output short-circuit duration[3]	t_{QSC}	∞	
Junction temperature	T_j	150	°C
Storage temperature range	T_{stg}	−55 to 125	°C
Thermal resistance (system-air)			
TBB 1458 B	$R_{th\ SA}$	100	K/W
TBB 1458 G	$R_{th\ SA}$	170	K/W

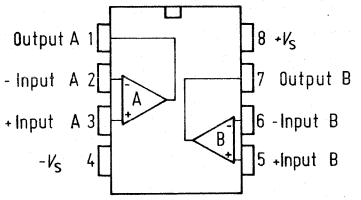
Operating range

Supply voltage range	V_S	± 4 to ± 18	V
Ambient temperature range	T_{amb}	0 to 70	°C

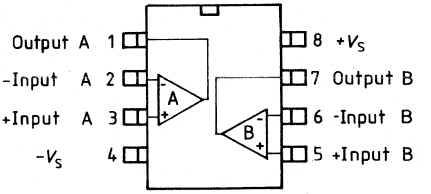
1) For supply voltages less than ± 15 V, the maximum input voltage is equal to the supply voltage.
2) For supply voltages less than ± 15 V, the maximum differential input voltage is equal to ± (V_{S+} + | V_{S-} |).
3) Short circuit may be to ground or to the supply voltage ± V_S, whereby the maximum ratings must not be exceeded.

Pin configurations

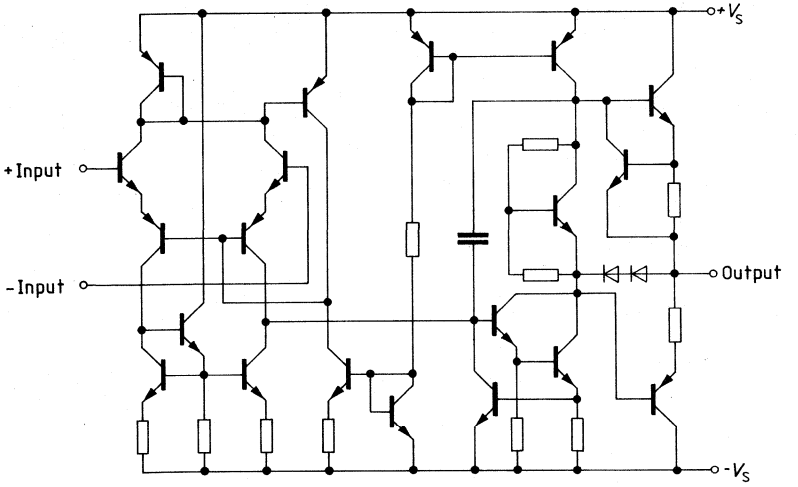
TBB 1458 B



TBB 1458 G



Circuit diagram of a single op amp

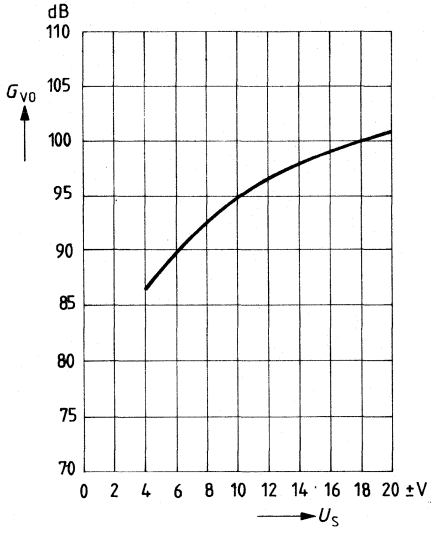


Characteristics
$V_S = \pm 15$ V

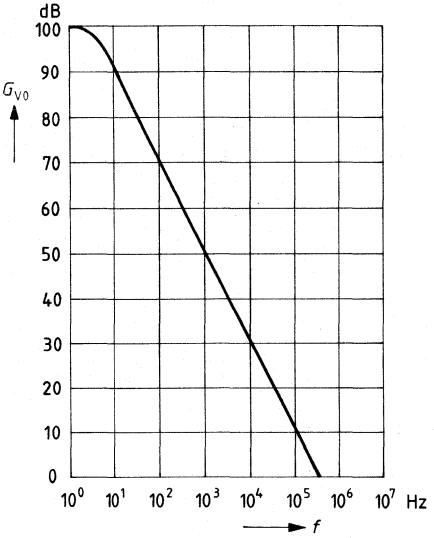
		$T_{amb} = 25$ °C			$T_{amb} = 0$ °C to 70 °C		
		min	typ	max	min	max	
Input offset voltage ($R_G \leq 10$ kΩ)	V_{IO}	−6		6	−7.5	7.5	mV
Input offset current	I_{IO}	−200	± 20	200	−300	300	nA
Input current	I_I		80	500		800	nA
Open-loop supply current consumption, total	I_S		2	3		3	mA
Output short-circuit current	I_{QSC}		± 18				mA
Common-mode input voltage range	V_{IC}	12	± 13	−12			V
Input resistance	R_I	0.3	1				MΩ
Input capacitance	C_I		6				pF
Output resistance	R_Q		75	−13			Ω
Output voltage ($R_L \geq 10$ kΩ)	$V_{Q\,pp}$	13	± 14	−13			V
($R_L \geq 2$ kΩ)	$V_{Q\,pp}$	11	± 13	−11			V
Voltage gain ($V_{Q\,pp} = \pm 10$ V, $R_L = 2$ kΩ)	G_V	86	100		84		dB
Common-mode rejection ($R_G \leq 10$ kΩ)	k_{CMR}	70	90				dB
Supply voltage rejection	k_{SCR}		30	150		150	μV/V
Temperature coefficient of V_{IO}	α_{VIO}		3				μV/K
Temperature coefficient of I_{IO}	α_{IIO}		0.4				nA/K
Slew rate*) ($G_V = 1$, $R_L \geq 2$ kΩ)	SR		0.5				V/μs

*) For the relationship between power bandwidth and slew rate refer to "General information" page 40

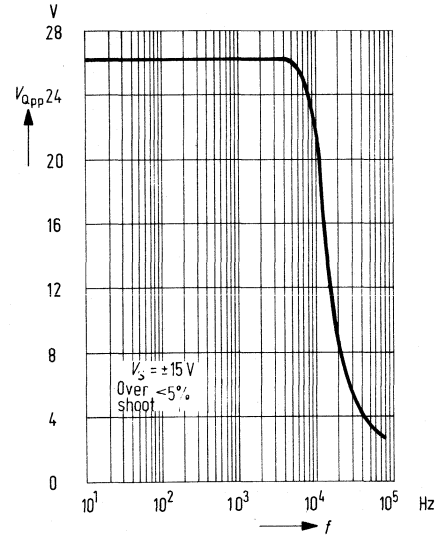
Open-loop voltage gain versus supply voltage



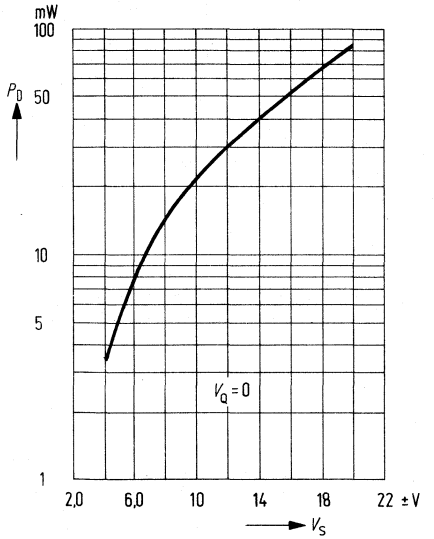
Open-loop voltage gain versus frequency



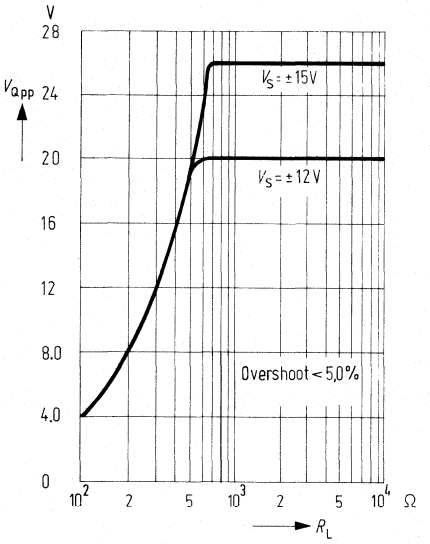
Power bandwidth
Output voltage versus frequency

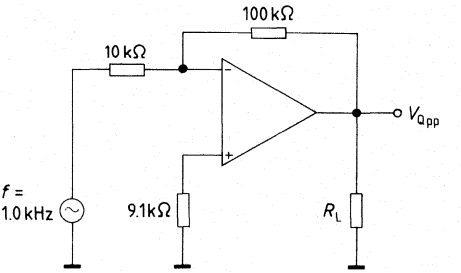


Power dissipation versus supply voltage

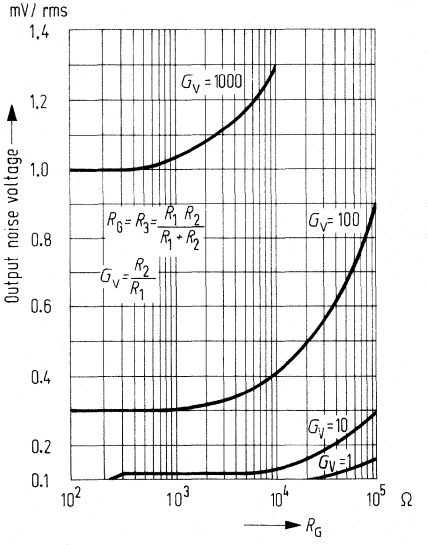


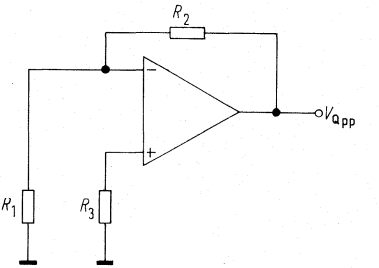
Output voltage versus load resistance





Output noise voltage versus generator resistance





For further characteristic curves refer to TBA 221.

Quad Operational Amplifiers

Type	Ordering code	Package	Fig. No.
TAA 4762 A	Q67000-A2502	DIP 14	7
TAA 4765 A	Q67000-A1033		

Particularly economic and versatile op amps. Owing to their excellent performance qualities, they are well suited for a wide scope of applications, as in control engineering, automotive electronics, AF circuits, analog computers, etc.

In addition to high gain, input resistance, low offset voltage, minor dependence on temperature and supply voltage, the amplifiers are outstanding for:

- Wide common-mode range
- Large supply voltage range
- Comprehensive protection against destruction
- High output current
- Large control range
- No frequency compensation
- Wide temperature range (TAA 4762 A)

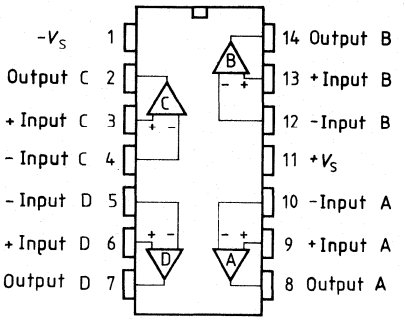
Maximum ratings

Supply voltage	V_S	± 15	V
Output current	I_Q	70	mA
Differential input voltage	V_{ID}	± V_S	V
Junction temperature	T_j	150	°C
Storage temperature range	T_{stg}	−55 to 125	°C
Thermal resistance (system-air)	$R_{th\ SA}$	80	K/W

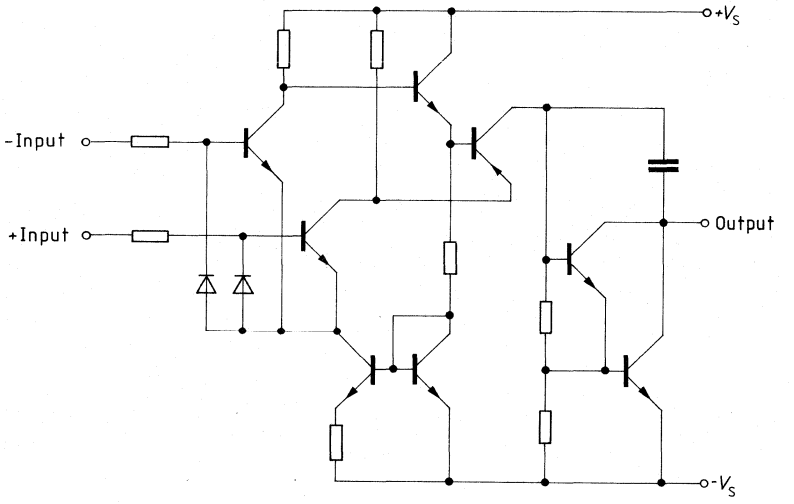
Operating range

Supply voltage range	V_S	± 2 to ± 15	V
Ambient temperature range TAA 4762 A	T_{amb}	−55 to 125	°C
TAA 4765 A	T_{amb}	−25 to 85	°C

Pin configuration



Circuit diagram of a single op amp



Characteristics
$V_S = \pm 5$ V to ± 15 V

		$T_{amb} = 25$ °C			$T_{amb} = -55$ to 125 °C		
		min	typ	max	min	max	
Open-loop supply current consumption, total	I_S		1	3		3	mA
Input offset voltage ($R_G = 50\ \Omega$)	V_{IO}	−4		4	−6	6	mV
Input offset current	I_{IO}	−100	± 50	100	−300	300	nA
Input current	I_I		0.3	0.7		1.0	µA
Output voltage ($R_L = 2$ kΩ, $V_S = \pm 15$ V)	V_{Qpp}	14.9		−14	14.8	−14	V
($R_L = 620\ \Omega$, $V_S = \pm 15$ V)	V_{Qpp}	14.9		−12.5	14.8	−12	V
Input impedance ($f = 1$ kHz)	Z_i		200				kΩ
Open-loop voltage gain ($R_L = 2$ kΩ, $f = 100$ Hz)	G_{V0}	85	87		80		dB
($R_L = 10$ kΩ, $f = 100$ Hz)	G_{V0}		92				dB
Output reverse current	I_{QR}			1		5	µA
Common-mode input voltage range ($R_L = 2$ kΩ, $V_S = \pm 15$ V)	V_{IC}	13	± 13.5	−13	12	−12	V
Common-mode rejection ($R_L = 2$ kΩ)	k_{CMR}	80	85		75		dB
Supply voltage rejection ($G_V = 100$)	k_{SVR}		25	100		100	µV/V
Temperature coefficient of V_{IO} ($R_G = 50\ \Omega$)	α_{VIO}		6	25		25	µV/K
Temperature coefficient of I_{IO} ($R_G = 50\ \Omega$)	α_{IIO}		0.3	1.5		1.5	nA/K
Noise voltage (in acc. with DIN 45405), referred to input $R_S = 2.5\ \Omega$)	V_n		3				µV
Output saturation voltage ($I_Q = 10$ mA)	V_{Qsat}			1			V
Slew rate for non-inverting operation*)	SR		0.5				V/µs
Slew rate for inverting operation*)	SR		0.5				V/µs

Characteristics
$V_S = \pm 2$ V

Input offset voltage	V_{IO}	−4		4	−6	6	mV
Input offset current	I_{IO}	−70		70	−200	200	nA
Input current	I_I		0.2	0.5		0.8	µA
Open-loop voltage gain ($R_L = 2$ kΩ, $f = 100$ Hz)	G_{V0}	80			75		dB

*) For the relationship between power bandwidth and slew rate refer to "General information" page 40

Characteristics
$V_S = \pm 5$ V to ± 15 V

		$T_{amb} = 25$ °C			$T_{amb} = -25$ to 85 °C		
		min	typ	max	min	max	
Open-loop supply current consumption, total	I_S		1	3		3	mA
Input offset voltage ($R_G = 50\ \Omega$)	V_{IO}	−5,5		5,5	−7	7	mV
Input offset current	I_{IO}	−200	± 80	200	−300	300	nA
Input current	I_I		0.5	0.8		1.0	µA
Output voltage ($R_L = 2$ kΩ, $V_S = \pm 15$ V)	V_{Qpp}	14.9		−14	14.8	−14	V
($R_L = 620\ \Omega$, $V_S = \pm 15$ V)	V_{Qpp}	14.9		−12.5	14.8	−12	V
Input impedance ($f = 1$ kHz)	Z_i		200				kΩ
Open-loop voltage gain ($R_L = 2$ kΩ, $f = 100$ Hz)	G_{V0}	80	85		80		dB
($R_L = 10$ kΩ, $f = 100$ Hz)	G_{V0}		90				dB
Output reverse current	I_{QR}			10		20	µA
Common-mode input voltage range ($R_L = 2$ kΩ, $V_S = \pm 15$ V)	V_{IC}	13	± 13.5	−13	12	−12	V
Common-mode rejection ($R_L = 2$ kΩ)	k_{CMR}	75	83		75		dB
Supply voltage rejection ($G_V = 100$)	k_{SVR}		25	100		100	µV/V
Temperature coefficient of V_{IO} ($R_G = 50\ \Omega$)	α_{VIO}		6				µV/K
Temperature coefficient of I_{IO} ($R_G = 50\ \Omega$)	α_{IIO}		0.3				nA/K
Noise voltage (in acc. with DIN 45405, referred to input $R_S = 2.5\ \Omega$)	V_n		3				µV
Output saturation voltage ($I_Q = 10$ mA)	V_{Qsat}			1			V
Slew rate for non-inverting operation*)	SR		0.5				V/µs
Slew rate for inverting operation*)	SR		0.5				V/µs

Characteristics
$V_S = \pm 2$ V

Input offset voltage	V_{IO}	−6		6	−7.5	7.5	mV
Input offset current	I_{IO}	−150		150	−200	200	nA
Input current	I_I		0.2	0.6		0.8	µA
Open-loop voltage gain ($R_L = 2$ kΩ, $f = 100$ Hz)	G_{V0}	75			75		dB

*) For the relationship between power bandwidth and slew rate refer to "General information" page 40

Quad Operational Amplifiers with Darlington Input

TBC 4332 A
TBE 4335 A

Bipolar IC

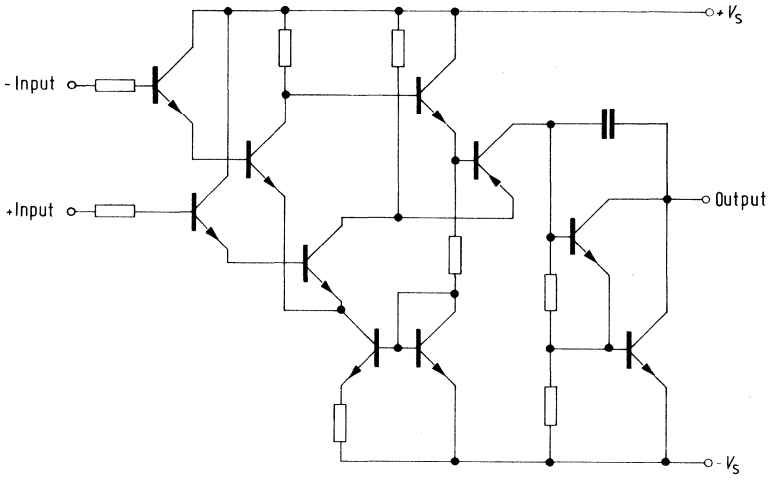
Type	Ordering code	Package	Fig. No.
TBC 4332 A	Q67000-A2503	DIP 14	7
TBE 4335 A	Q67000-A1167	DIP 14	7

Economic and versatile op amps. Owing to their excellent performance qualities, they are well suited for a wide scope of applications, as in control engineering, automotive electronics, AF circuits, analog computers, etc. The low input current of these amplifiers is particularly advantageous for application in control systems.

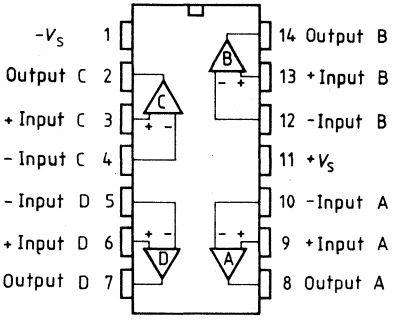
In addition to high gain, low offset voltage, minor dependence on temperature and supply voltage, the amplifiers are outstanding for:

- High input resistance
- Wide common-mode range
- Large supply voltage range
- Large control range
- High output current
- Wide temperature range (TBC 4332 A)

Circuit diagram of a single op amp



Pin configuration



Maximum ratings

Supply voltage	V_S	± 15	V
Output current	I_Q	70	mA
Differential input voltage, V_S = ± 13 to ± 15 V	V_{ID}	± 13	V
Differential input voltage, V_S = ± 2 to ± 13 V	V_{ID}	± V_S	V
Junction temperature	T_j	150	°C
Storage temperature range	T_{stg}	−55 to 125	°C
Thermal resistance (system-air)	$R_{th\ SA}$	80	K/W

Operating range

Supply voltage range	V_S	± 2 to ± 15	V
Ambient temperature range	T_{amb}	−55 to 125	°C

Characteristics

V_S = ± 5 V to ± 15 V

		T_{amb} = 25 °C			T_{amb} = −55 to 125 °C		
		min	typ	max	min	max	
Open-loop supply current consumption, total	I_S		1	3		3	mA
Input offset voltage (R_G = 50 Ω)	V_{IO}	−10		10	−15	15	mV
Input offset current	I_{IO}	−5		5	−10	10	nA
Input current	I_I		5	15		25	nA
Output voltage (R_L = 2 kΩ, V_S = ± 15 V)	V_{Qpp}	14.9		−14	14.8	−14	V
(R_L = 620 Ω, V_S = ± 15 V)	V_{Qpp}	14.9		−12.5	14.8	−12	V
Input impedance (f = 1 kHz)	Z_i		3				MΩ
Open-loop voltage gain (R_L = 2 kΩ, f = 100 Hz)	G_{V0}	85	87		80		dB
(R_L = 10 kΩ, f = 100 Hz)	G_{V0}		92				dB
Output reverse current	I_{QR}			1		5	µA
Common-mode input voltage range (R_L = 2 kΩ) (comparator operation)	V_{IC}	$+V_S$		$-V_S$+2.0	$+V_S$	$-V_S$+3	V
Common-mode rejection (R_L = 2 kΩ)	k_{CMR}	80	85		75		dB
Supply voltage rejection (G_V = 100)	k_{SVR}		25	100		100	µV/V
Temperature coefficient of V_{IO} (R_G = 50 Ω)	α_{VIO}		12	50		50	µV/K
Temperature coefficient of I_{IO} (R_G = 50 Ω)	α_{IIO}		50				pA/K
Output saturation voltage (I_Q = 10 mA)	V_{Qsat}			1			V
Slew rate for non-inverting operation*)	SR		0.5				V/µs
Slew rate for inverting operation*)	SR		0.5				V/µs

Characteristics

V_S = ± 2 V

Input offset voltage	V_{IO}	−10		10	−15	15	mV
Input offset current	I_{IO}	−5		5	−10	10	nA
Input current	I_I		5	15		25	nA
Open-loop voltage gain (R_L = 2 kΩ, f = 100 Hz)	G_{V0}	80			75		dB

*) For the relationship between power bandwidth and slew rate refer to "General information" page 40

Maximum ratings

Supply voltage	V_S	± 15	V
Output current	I_Q	70	mA
Differential input voltage, $V_S = \pm$ 13 to ± 15 V	V_{ID}	± 13	V
Differential input voltage, $V_S = \pm$ 2 to ± 13 V	V_{ID}	± V_S	V
Junction temperature	T_j	150	°C
Storage temperature range	T_{stg}	−55 to 125	°C
Thermal resistance (system-air)	$R_{th\ SA}$	80	K/W

Operating range

Supply voltage range	V_S	± 2 to ± 15	V
Ambient temperature range	T_{amb}	−25 to 85	°C

Characteristics

$V_S = \pm$ 5 V to ± 15 V

		T_{amb} = 25 °C			T_{amb} = −25 to 85 °C		
		min	typ	max	min	max	
Open-loop supply current consumption, total	I_S		1	3		3	mA
Input offset voltage (R_G = 50 Ω)	V_{IO}	−15		15	−18	18	mV
Input offset current	I_{IO}	−10		10	−20	20	nA
Input current	I_I		5	25		35	nA
Output voltage (R_L = 2 kΩ, $V_S = \pm$ 15 V)	V_{Qpp}	14.9		−14	14.8	−14	V
(R_L = 620 Ω, $V_S = \pm$ 15 V)	V_{Qpp}	14.9		−12.5	14.8	−12	V
Input impedance (f = 1 kHz)	Z_i		3				MΩ
Open-loop voltage gain (R_L = 2 kΩ, f = 100 Hz)	G_{V0}	80	85		80		dB
(R_L = 10 kΩ, f = 100 Hz)	G_{V0}		90				dB
Output reverse current	I_{QR}			10		20	µA
Common-mode input voltage range (R_L = 2 kΩ) (comparator operation)	V_{IC}	$+V_S$-0.5		$-V_S$+2.0	$+V_S$-.08	$-V_S$+3	V
Common-mode rejection (R_L = 2 kΩ)	k_{CMR}	75	83		75		dB
Supply voltage rejection (G_V = 100)	k_{SVR}		25	100		100	µV/V
Temperature coefficient of V_{IO} (R_G = 50 Ω)	α_{VIO}		12				µV/K
Temperature coefficient of I_{IO} (R_G = 50 Ω)	α_{IIO}		50				pA/K
Output saturation voltage (I_Q = 10 mA)	V_{Qsat}			1			V
Slew rate for non-inverting operation*)	SR		0.5				V/µs
Slew rate for inverting operation*)	SR		0.5				V/µs

Characteristics

$V_S = \pm$ 2 V

Input offset voltage	V_{IO}	−17		17	−20	20	mV
Input offset current	I_{IO}	−10		10	−20	20	nA
Input current	I_I		5	25		35	nA
Open-loop voltage gain (R_L = 2 kΩ, f = 100 Hz)	G_{V0}	75			75		dB

*) For the relationship between power bandwidth and slew rate refer to "General information" page 40

Type	Ordering code	Package	Fig. No.
TAE 4453 A	Q67000-A2109	DIP 14	7
TAE 4453 G	Q67000-A2152	SO 14	27
TAF 4453 A	Q67000-A2212	DIP 14	7
TAF 4453 G	Q67000-A2213	SO 14	27

The TAE 4453/TAF 4453 consists of four independent, frequency-compensated op amps, each having a PNP input differential stage and an open collector output. The integrated regulator provides for all parameters a large degree of independence of the supply voltage. The component is especially suited for applications with the following characteristics:

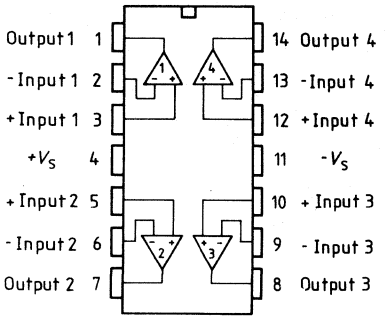
- Operation with very low supply voltages of 2 V (1.8 V)
- Direct driving of loads up to 70 mA
- Direct driving of TTL loads
- Level conversion to all logic families
- Large-signal control
- Zero detector $V_I = 0$ V or $-V_S$
- High immunity of the inputs to overvoltage surges (up to 40 V)

Outstanding electrical features

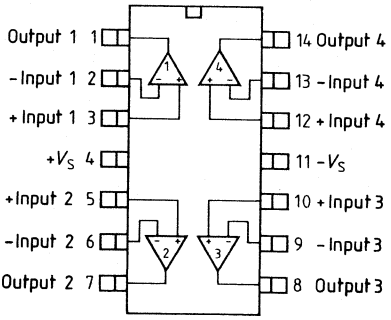
- Supply voltage range between 2 V (1.8 V) and 36 V
- Low current consumption, 1.6 mA typ.
- Extremely large control range
- Low output saturation voltage, almost independent of load current
- Very wide common-mode range, down to 0.3 V below the negative supply voltage
- Output current up to 70 mA (100 mA max.)
- Short-circuit proof output
- Very low input current
- Very low input offset voltages
- Operating temperature range of TAE 4453 A -25 to $+85$ °C
  TAF 4453 A -55 to $+125$ °C

Pin configuration

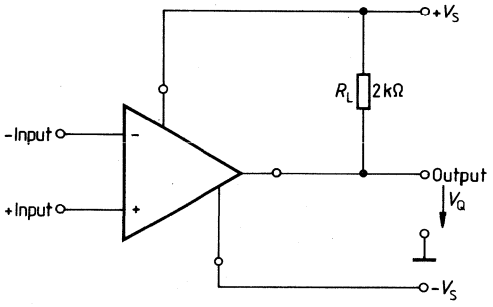
TAE 4453 A, TAF 4453 A



TAE 4453 G, TAF 4453 G

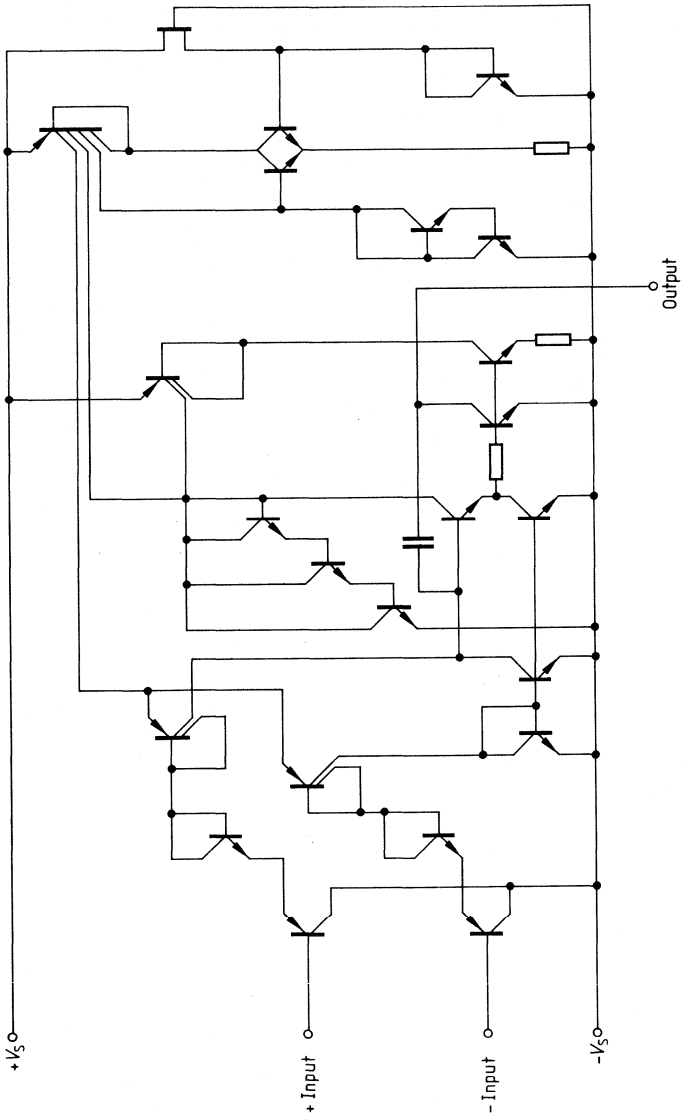


Connection diagram



R_L = load resistor

Circuit diagram



Maximum ratings

Supply voltage	V_S	± 18	V
Output current	I_Q	100	mA
Differential input voltage	V_{ID}	± V_S	V
Junction temperature	T_j	150	°C
Storage temperature range	T_{stg}	−55 to 150	°C
Thermal resistance (system-air)	$R_{th\ SA}$	80	K/W

Operating range

Supply voltage range	V_S	± 1.0 to ± 18 (± 0.9 V with slightly increased offset voltage)	V
Ambient temperature range	T_{amb}	−25 to 85	°C

Characteristics

V_S = ± 5 V to ± 15 V

		T_{amb} = 25 °C			T_{amb} = −25 to 85 °C		
		min	typ	max	min	max	
Open-loop supply current consumption (outputs in H state)	I_S		1.6	3.0		3.6	mA
Input offset voltage (R_G = 50 Ω)	V_{IO}	−5.5		5.5	−7	7	mV
Input offset current	I_{IO}			75		100	nA
Input current	I_I		40	150		200	nA
Output voltage (R_L = 2 kΩ, V_S = ± 15 V)	V_{Qpp}	14.9		−14.7	14.8	−14.7	V
Output voltage (R_L = 620 Ω, V_S = ± 15 V)	V_{Qpp}	14.9		−14.5	14.8	−14.4	V
Input impedance (f = 1 kHz)	Z_i		200				kΩ
Open-loop voltage gain (R_L = 2 kΩ)	G_{V0}	80	85		80		dB
Output reverse current	I_{QR}			10		20	µA
Common-mode input voltage range (R_L = 2 kΩ)	V_{IC}	$-V_S$-0.2		$+V_S$-1.8	$-V_S$	$+V_S$-2.0	V
Common-mode rejection (R_L = 2 kΩ)	k_{CMR}	75	80		75		dB
Supply voltage rejection (G_V = 100)	k_{SVR}		25	100		100	µV/V
Temperature coefficient of I_{IO}	α_{IIO}		0.1				nA/K
Temperature coefficient of V_{IO} (R_G = 50 Ω)	α_{VIO}		6				µV/K
Slew rate for non-inverting operation*)	SR		1				V/µs
Slew rate for inverting operation*)	SR		1				V/µs

Characteristics

V_S = ± 2 V

Input offset voltage (R_G = 50 Ω)	V_{IO}	−6		6	−7.5	7.5	mV
Input offset current	I_{IO}			75		100	nA
Input current	I_I		40	150		200	nA
Open-loop voltage gain (R_L = 2 kΩ)	G_{V0}	70			70		dB

*) For the relationship between power bandwidth and slew rate refer to "General information" page 40

Maximum ratings

Supply voltage	V_S	± 18	V
Output current	I_Q	100	mA
Differential input voltage	V_{ID}	± V_S	V
Junction temperature	T_j	150	°C
Storage temperature range	T_{stg}	−55 to 150	°C
Thermal resistance (system-air)	$R_{th\ SA}$	80	K/W

Operating range

Supply voltage range	V_S	± 1.0 to ± 18 (± 0.9 V with slightly increased offset voltage)	V
Ambient temperature range	T_{amb}	−55 to 125	°C

Characteristics

V_S = ± 5 V to ± 15 V

		T_{amb} = 25 °C			T_{amb} = −55 to 125 °C		
		min	typ	max	min	max	
Open-loop supply current consumption (outputs in H state)	I_S		1.6	3.0		3.6	mA
Input offset voltage (R_G = 50 Ω)	V_{IO}	−4		4	−6	6	mV
Input offset current	I_{IO}			50		75	nA
Input current	I_I		40	100		150	nA
Output voltage (R_L = 2 kΩ, V_S = ± 15 V)	V_{Qpp}	14.9		−14.7	14.8	−14.7	V
Output voltage (R_L = 620 Ω, V_S = ± 15 V)	V_{Qpp}	14.9		−14.5	14.8	−14.4	V
Input impedance (f = 1 kHz)	Z_i		200				kΩ
Open-loop voltage gain (R_L = 2 kΩ)	G_{V0}	85	87		80		dB
Output reverse current	I_{QR}			1		5	µA
Common-mode input voltage range (R_L = 2 kΩ)	V_{IC}	$-V_S$−0.3		$+V_S$−1.5	$-V_S$	$+V_S$−1.8	V
Common-mode rejection (R_L = 2 kΩ)	k_{CMR}	80	85		75		dB
Supply voltage rejection (G_V = 100)	k_{SVR}		25	100		100	µV/V
Temperature coefficient of I_{IO}	α_{IIO}		0.1	0.8		0.8	nA/K
Temperature coefficient of V_{IO} (R_G = 50 Ω)	α_{VIO}		6	25		25	µV/K
Slew rate for non-inverting operation*)	SR		1				V/µs
Slew rate for inverting operation*)	SR		1				V/µs

Characteristics

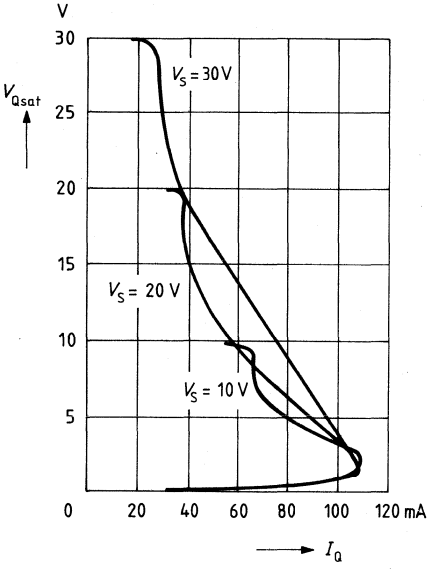
V_S = ± 2 V

Input offset voltage (R_G = 50 Ω)	V_{IO}	−4		4	−6	6	mV
Input offset current	I_{IO}			50		75	nA
Input current	I_I		40	100		150	nA
Open-loop voltage gain (R_L = 2 kΩ)	G_{V0}	75			70		dB

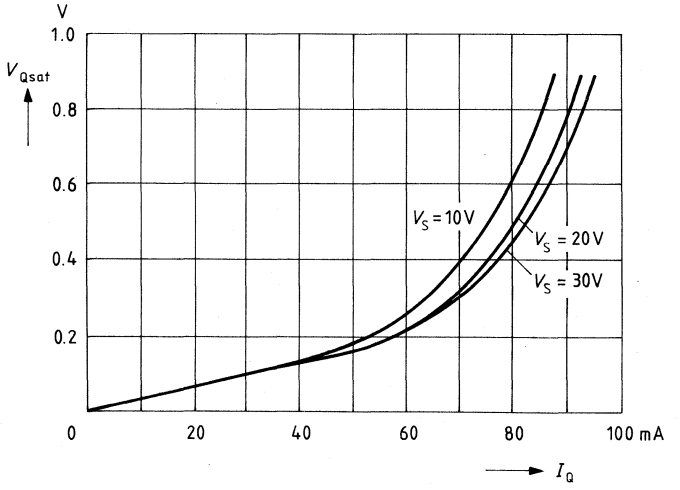
*) For the relationship between power bandwidth and slew rate refer to "General information" page 40

Typical characteristics of electrical parameters

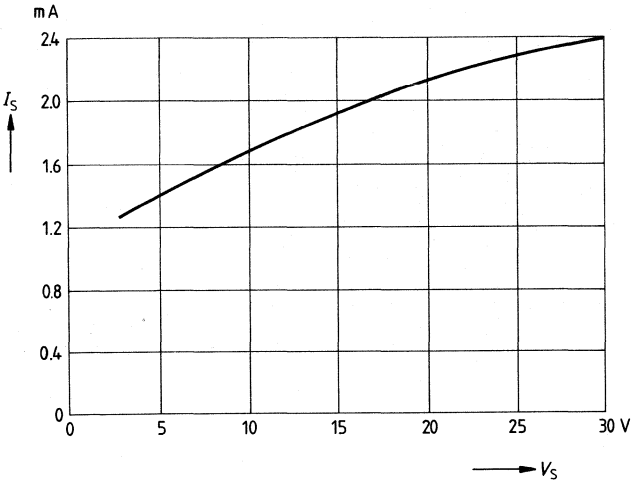
Load characteristics
Saturation voltage versus output current



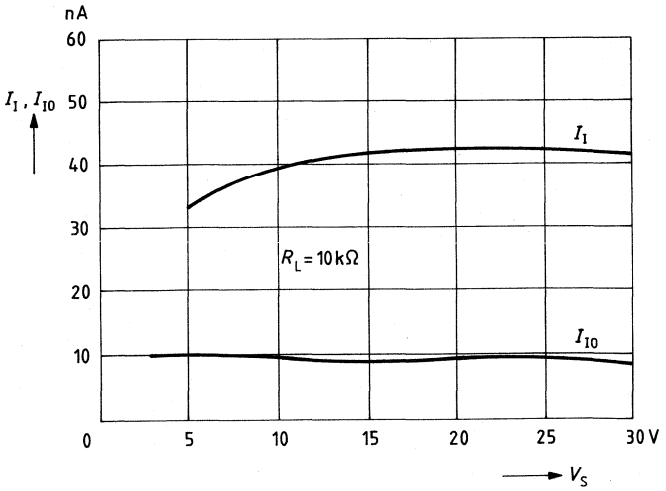
Saturation voltage versus output current



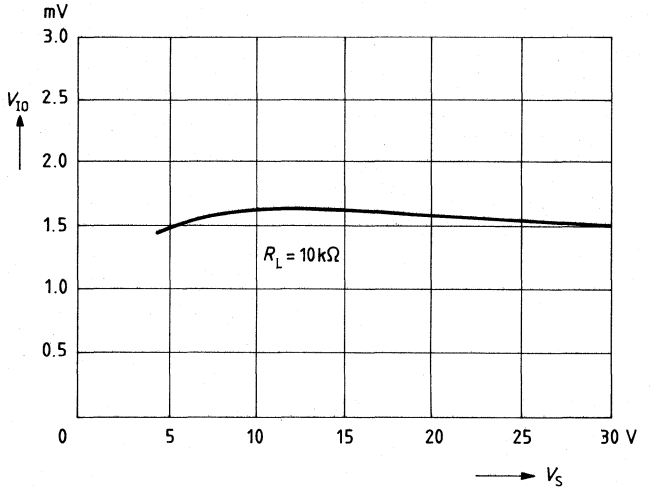
Supply current versus supply voltage



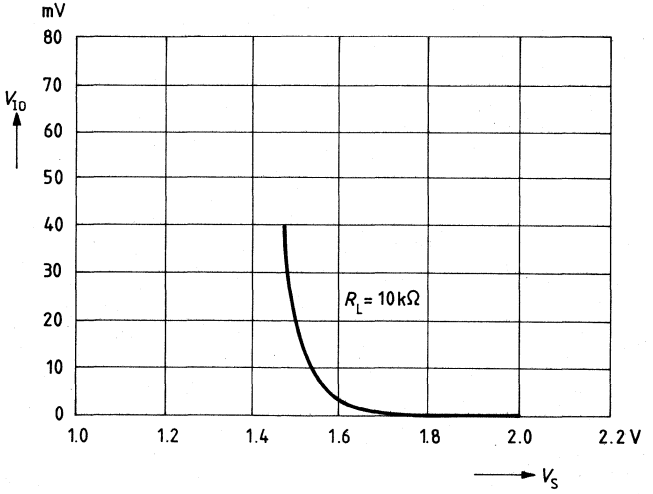
Input current and input offset current versus supply voltage



Input offset voltage versus supply voltage



V_{IO} behavior at low operating voltages
Input offset voltage versus supply voltage



Power Operational Amplifiers

Bipolar IC

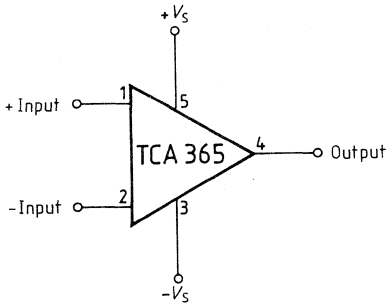
Type	Ordering code	Package	Fig. No.
TCA 365	Q67000-A1875	Plastic power package similar to TO 220	2
TCA 365 H	Q67000-A2145	Plastic power package similar to TO 220	1

The TCA 365 is a power op amp in a package which is similar to TO-220. At a maximum supply voltage of ± 18 V, the IC delivers the high output current of 3.0 A. The op amp is protected against thermal overload.

Features

- High peak output current, up to 3.0 A
- High supply voltage, up to 36 V
- Fast slew rate of 5 V/µs
- Thermal overload protection
- Internal power limitation

Pin configuration



Pin 3 is electrically connected to cooling fin.

Maximum ratings

Supply voltage	V_S	± 18	V
Differential input voltage	V_{ID}	± V_S	V
Peak output current	I_Q	3.0	A
Junction temperature	T_j	150	°C
Storage temperature range	T_{stg}	−55 to 125	°C
Total power dissipation (at T_{case} = 90 °C)	P_{tot}	15	W
Thermal resistance (system-case)	$R_{th\,SC}$	5	K/W

Operating range

Supply voltage range	V_S	± 4 to ± 18	V
Ambient temperature range	T_{amb}	−25 to 85	°C
Voltage gain	G_{Vmin}	20	dB

Characteristics $V_S = \pm 15$ V; $T_{case} = 25$ °C		Test circuit	min	typ	max	
Open-loop supply current consumption	I_S	1		20	40	mA
Input offset voltage	V_{IO}	2	−10		10	mV
Input offset current	I_{IO}	3	−100		100	nA
Input current	I_I	3		0.2	1	µA
Output voltage ($R_L = 13\ \Omega$)	$V_{Q\,pp}$	4	± 12.5	± 13		V
($R_L = 4.7\ \Omega$)			± 11.7	± 12		V
Output voltage ($R_L = 470\ \Omega$, $f = 100$ kHz, $G_V = 30$ dB)	$V_{Q\,pp}$	4		± 10		V
Input resistance ($f = 1$ kHz)	R_I	4	1	5		MΩ
Open-loop voltage gain ($R_L = 8.2\ \Omega$, $f = 100$ Hz)	G_{V0}	5	80	90		dB
Common-mode input voltage range	V_{IC}	6	+13.4/−15	+13.5/−15.1		V
Common-mode rejection	k_{CMR}	6	75	83		dB
Supply voltage rejection	k_{SVR}	7	70	80		dB
Temperature coefficient of V_{IO} $-25 \leq T_{case} \leq 85$ °C	α_{VIO}	2		50		µV/K
Temperature coefficient of I_{IO} $-25 \leq T_{case} \leq 85$ °C	α_{IIO}	3		0.4		nA/K
Slew rate of V_q for non-inverting operation*)	SR	8		5		V/µs
Slew rate of V_q for inverting operation*)	SR	9		5.5		V/µs
Equivalent input noise voltage	V_n	1		3		µV

*) For the relationship between power bandwidth and slew rate refer to "General information" page 40

Test circuits

Figure 1 Open-loop supply current consumption, equivalent input noise voltage

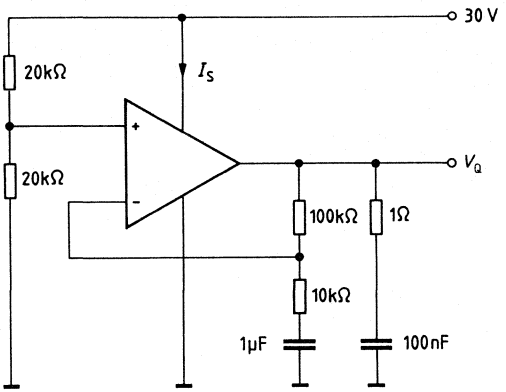


Figure 2 Input offset voltage, *TC* of V_{IO}

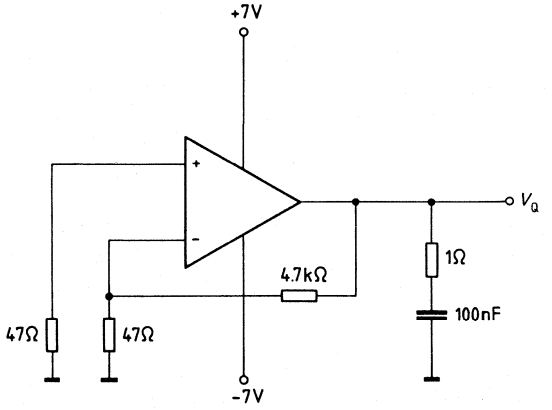
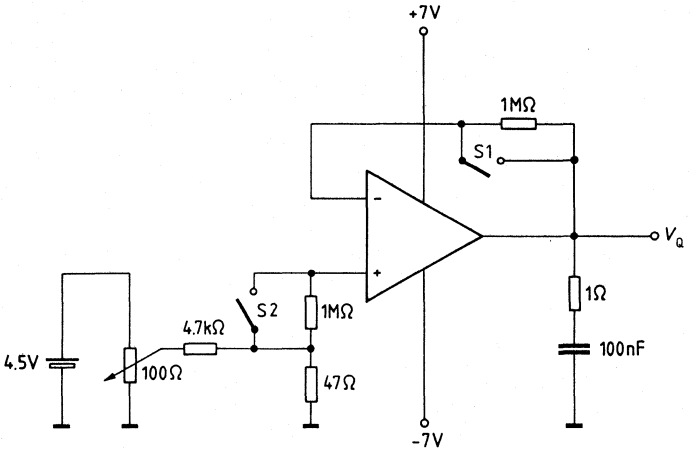


Figure 3 **Input offset current; input current,** *TC* of I_{IO}



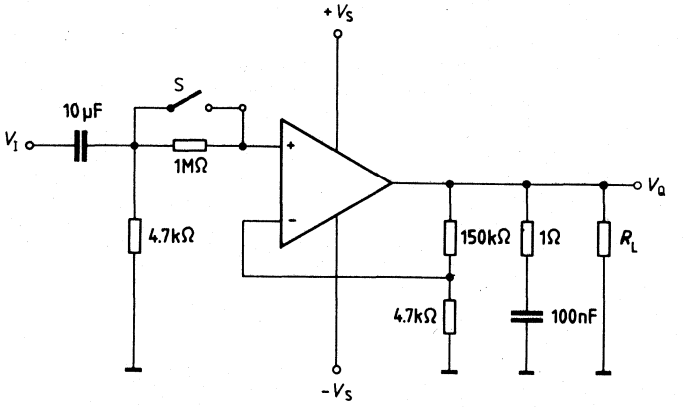
S1 open – S2 closed: $I_{I-} = \frac{V_Q}{1\,M\Omega}$

S2 open – S1 closed: $I_{I+} = \frac{V_Q}{1\,M\Omega}$

S1 open – S2 open: $I_{IO} = \frac{V_Q}{1\,M\Omega}$

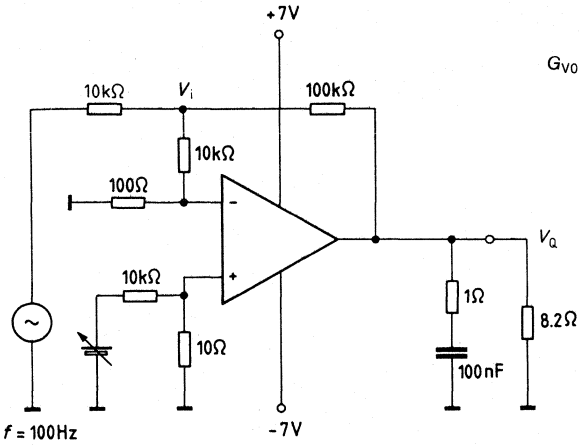
S1 closed – S2 closed: offset adjustment

Figure 4 **Output voltage, input resistance**



S closed: to measure V_{Qpp}
S open/closed: to measure R_I

Figure 5 Open-loop voltage gain



$$G_{VO} = \left| 20 \log 101 \times \frac{V_Q}{V_i} \right|$$

Figure 6 Common-mode voltage gain G_{VC}
Common-mode rejection k_{CMR} (dB) = G_{VO} (dB) − G_{VC} (dB)

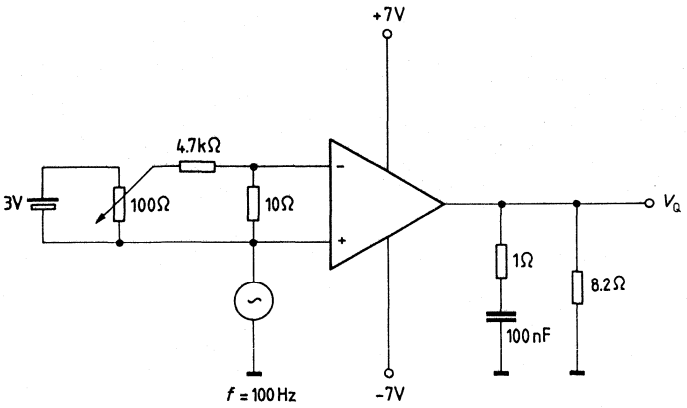
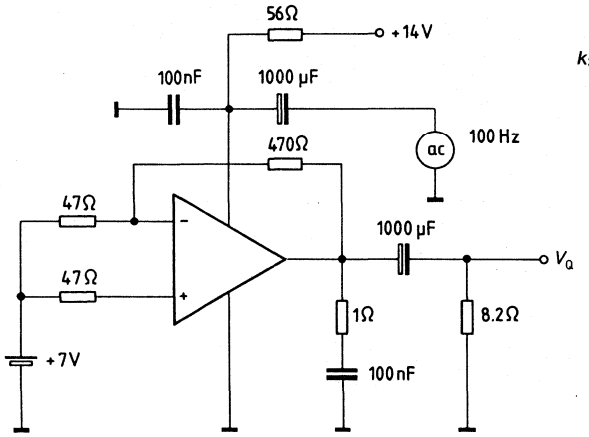


Figure 7 Supply voltage rejection



$$k_{SVR} = 20 \log \frac{\Delta V_Q}{G_V \times \Delta V_S} \text{ [dB]}$$

Figure 8 Slew rate for non-inverting operation

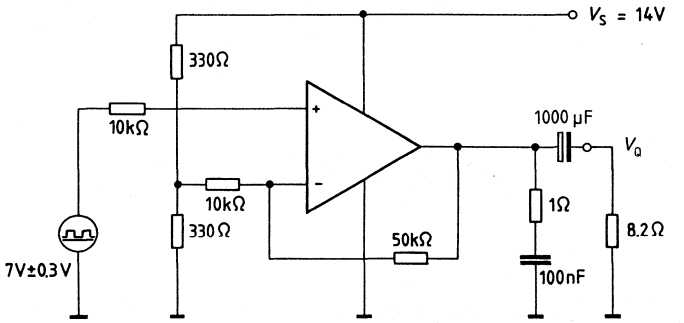
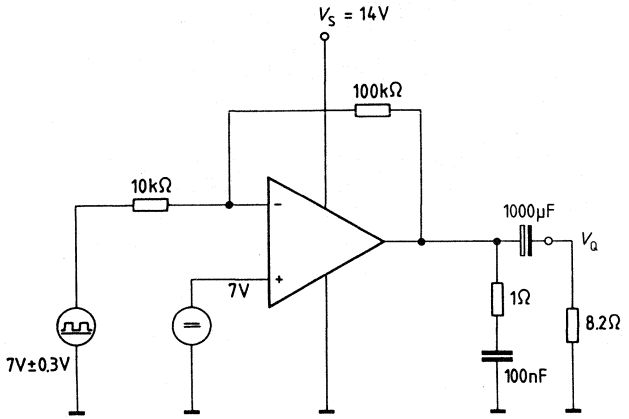
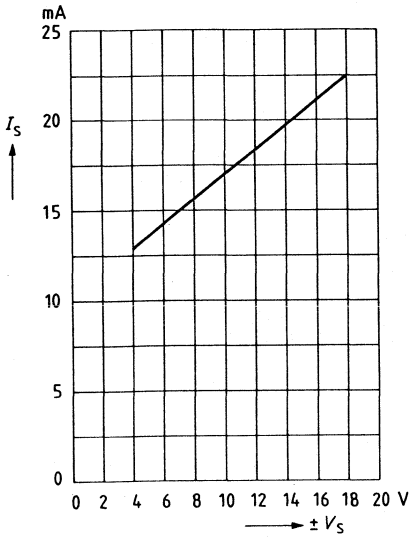


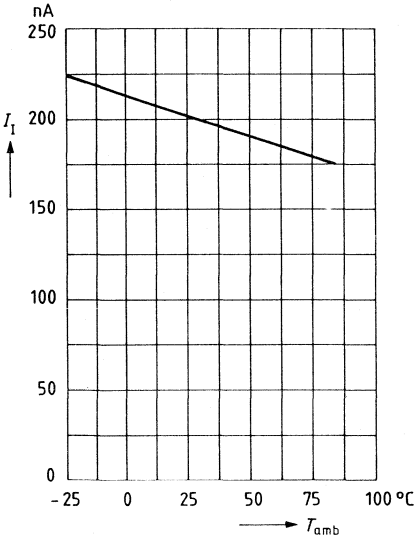
Figure 9 Slew rate for inverting operation



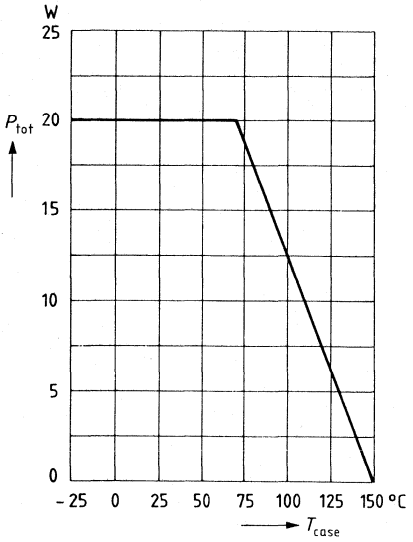
Supply current versus supply voltage



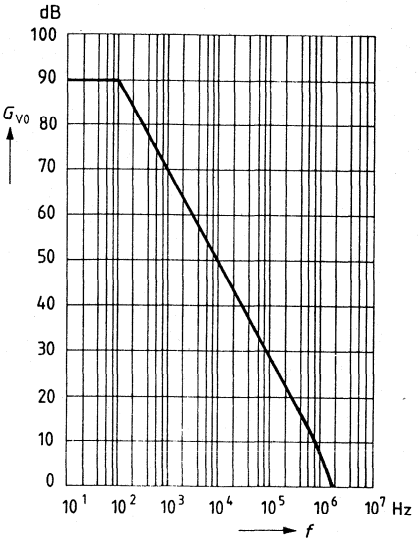
Input current versus ambient temperature



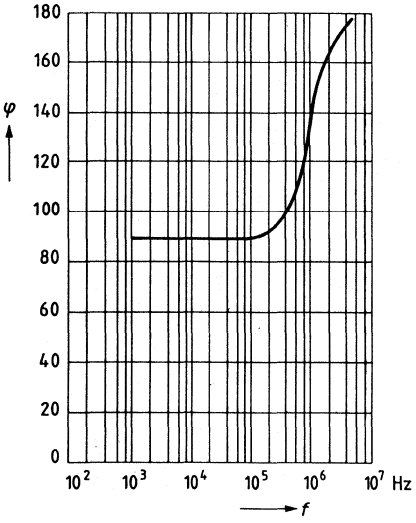
Total power dissipation versus case temperature



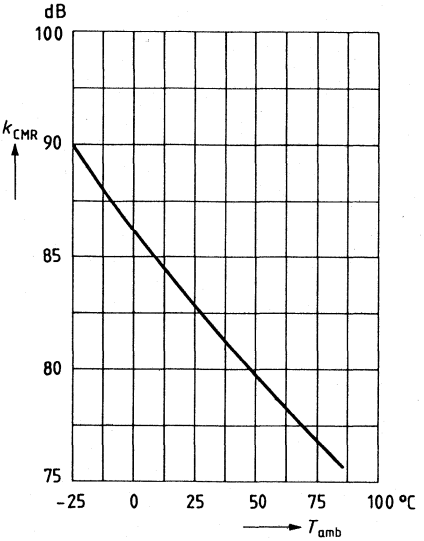
Open-loop voltage gain versus frequency



Phase response versus frequency



Common-mode rejection versus ambient temperature



Preliminary data **Bipolar IC**

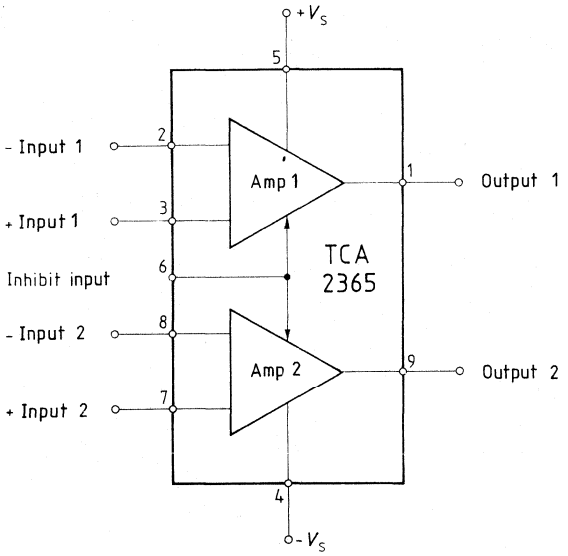
Type	Ordering code	Package	Fig. No.
TCA 2365	Q67000-A1876	SIP 9	21

The TCA 2365 is a dual power op amp in a SIP 9 package. The IC contains two identical op amps, each supplying a high output current of 2.5 A at supply voltages between ± 4 V and ± 13 V. Both amplifiers can be disconnected simultaneously (tristate; $Z_Q \approx 4$ kΩ) via an inhibit input. Integrated protective circuits protect the outputs against short circuit to $+V_S$ and $-V_S$ and prevent a thermal overloading of the IC.

Features

- High output current of two times 2.5 A
- Large operating voltage range, 8 V to 26 V
- High slew rate 4 V/µs
- Outputs entirely protected (dc short-circuit proof)
- Thermal overload protection
- Inhibit input enables "tristate" outputs

Pin configuration



Pin 4 is electrically connected to cooling fin.

Maximum ratings

Supply voltage	V_S	± 15	V
Differential input voltage	V_{ID}	± V_S	V
Output voltage range	V_Q	$-V_S-1$ to $+V_S+1$	V
Peak output current	I_Q	± 2.5	A
Supply current	I_S	5.5	A
Junction temperature	T_j	150	°C
Storage temperature range	T_{stg}	−55 to 125	°C
Total power dissipation			
$T_{case} = 90$ °C	P_{tot}	10.0	W
Thermal resistance (system-air)	$R_{th\ SA}$	65	K/W
Thermal resistance (system-case)	$R_{th\ SC}$	6	K/W

Operating range

Supply voltage range	V_S	± 4 to ± 13	V
Case temperature range			
($P_{tot} = 10.0$ W)	T_{case}	−25 to 85	°C
Voltage gain	G_{Vmin}	10	dB

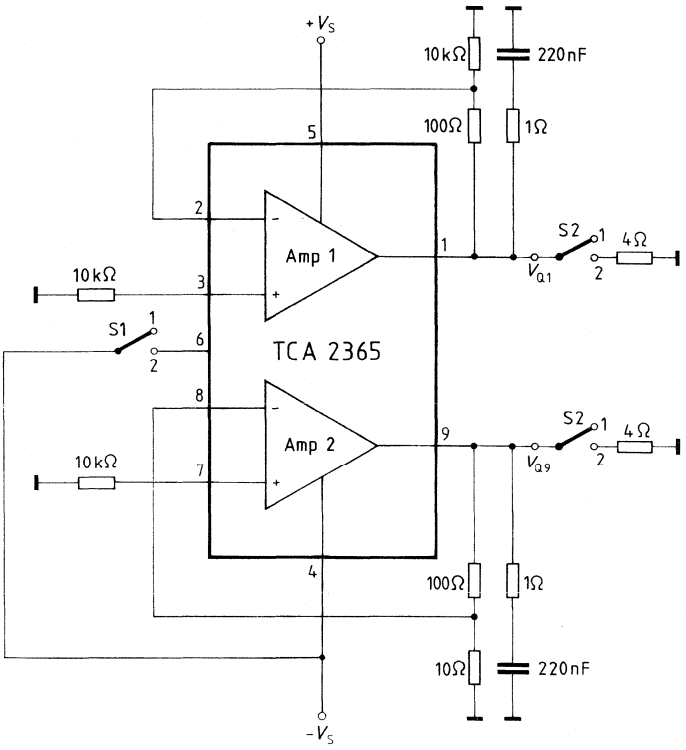
Characteristics
($V_S = \pm 10$ V; $T_{case} = 25$ °C)

		Test circuit	min	typ	max	
Open-loop supply current consumption						
S1 in position 1	I_S	1		30	50	mA
S1 in position 2	I_{SM}	1		5	8	mA
Input offset voltage	V_{IO}	2	−10		10	mV
Input offset current	I_{IO}	3	−100		100	nA
Input current	I_I	3		0.25	1	µA
Output voltage						
($R_L = 12\ \Omega$; $f = 1$ kHz)	$V_{Q\,pp}$	4	± 8.5	± 9.0		V
($R_L = 4\ \Omega$; $f = 1$ kHz)	$V_{Q\,pp}$	4	± 8.0	± 8.5		V
($R_L = 470\ \Omega$; $f = 50$ kHz)	$V_{Q\,pp}$	4		± 6.0		V
Input resistance ($f = 1$ kHz)	R_I	4	1	5		MΩ
Open-loop voltage gain ($f = 100$ Hz)	G_{V0}	5	70	80		dB
Voltage gain	G_V	8	10			dB
Common-mode input voltage range	V_{IC}	6	+7/−10	+7.5/−10.5		V
Common-mode rejection	k_{CMR}	6	70	80		dB
Supply voltage rejection	k_{SVR}	7	70	80		dB
Temperature coefficient of V_{IO} $-25\,°C \leq T_{case} \leq +85\,°C$	α_{VIO}	2		50		µV/K
Temperature coefficient of I_{IO} $-25\,°C \leq T_{case} \leq +85\,°C$	α_{IIO}	3		0.4		nA/K
Slew rate of V_q for non-inverting operation	SR	8		4		V/µs
Slew rate of V_q for inverting operation	SR	9		4		V/µs
Equivalent input noise voltage	V_n	1		3		µV
Inhibit input (referred to $-V_S$)						
V_6 for IC turned off	$V_{6\,off}$	1	0		1.0	V
V_6 for IC turned on	$V_{6\,on}$	1	3.0		$+V_S$	V
Turn-on time $\lvert I_{1;9} \rvert > 1$ A (referred to $V_{6\,off/on}$, S2 and S3 in position 2)	t_{don}	1		2	5	µs
Turn-off time $\lvert I_{1;9} \rvert < 1$ A (referred to $V_{6\,off/on}$, S2 and S3 in position 2)	t_{doff}	1		15	30	µs

*) For the relationship between power bandwidth and slew rate refer to "General information" page 40

Test circuits

Figure 1 Open-loop supply current consumption, equivalent input noise voltage, turn-off voltage



Switch as drawn if not specified otherwise.

Test circuits

Figure 2 Input offset voltage, temperature coefficient of V_{IO}

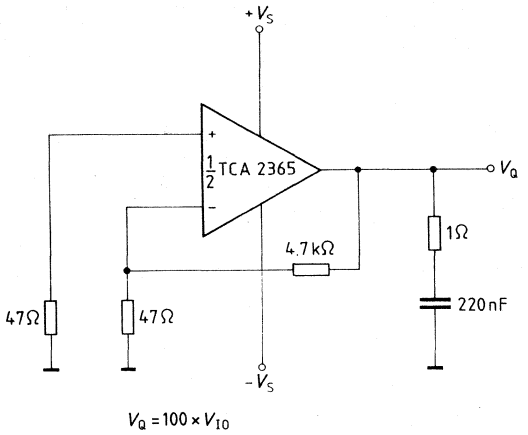
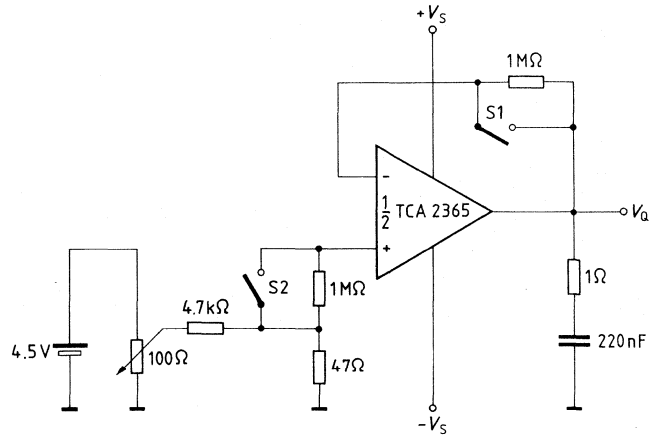


Figure 3 Input offset current, input current, temperature coefficient of I_{IO}



S1 open – S2 closed: $I_{I-} = \frac{V_Q}{1\,M\Omega}$

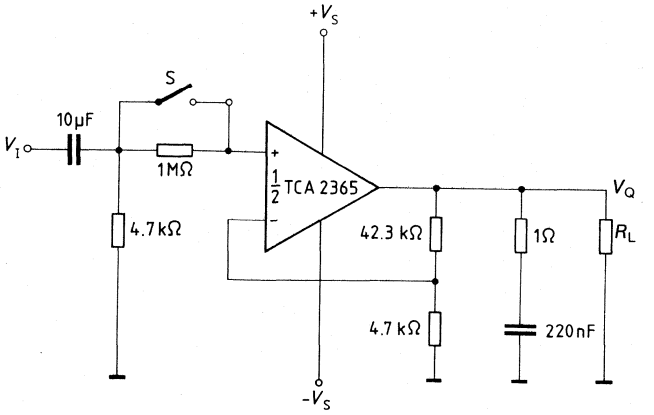
S2 open – S1 closed: $I_{I+} = \frac{V_Q}{1\,M\Omega}$

S1 open – S2 open: $I_{IO} = \frac{V_Q}{1\,M\Omega}$

S1 closed – S2 closed: offset adjustment

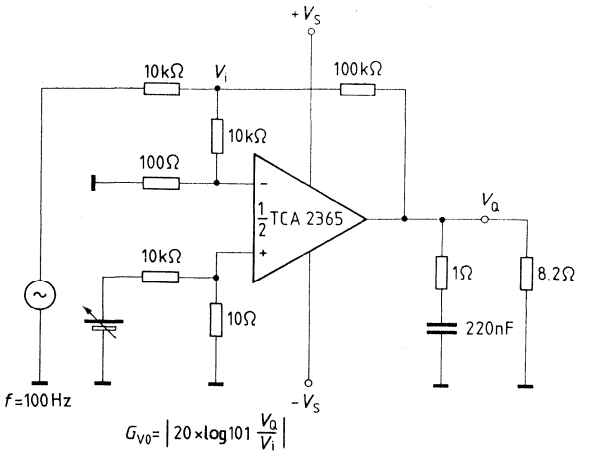
Test circuits

Figure 4 Output voltage, input resistance



S closed: to measure V_{Qpp}
S open/closed: to measure R_I

Figure 5 Open-loop voltage gain



Test circuits

Figure 6 **Open-loop voltage gain G_{VC}**
common-mode rejection k_{CMR} (dB) = G_{V0} (dB) – G_{VC} (dB)

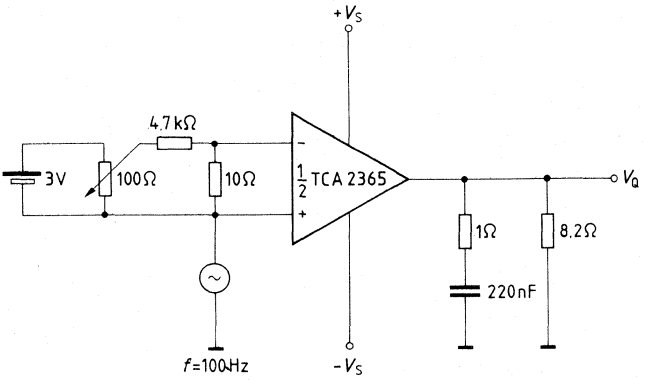
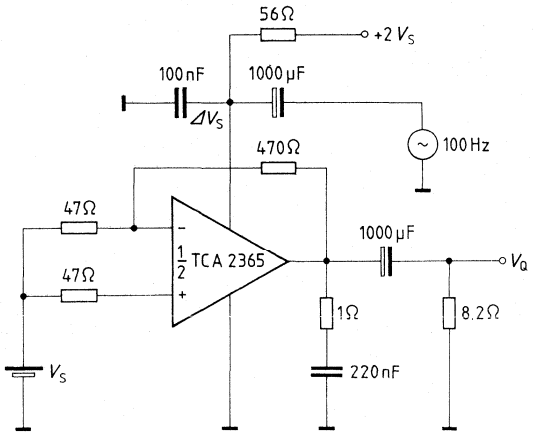


Figure 7 **Supply voltage rejection**



$$k_{SVR} = 20\log \frac{\Delta V_Q}{G_V \cdot \Delta V_S} \text{ [dB]}$$

Test circuits

Figure 8 Slew rate for non-inverting operation

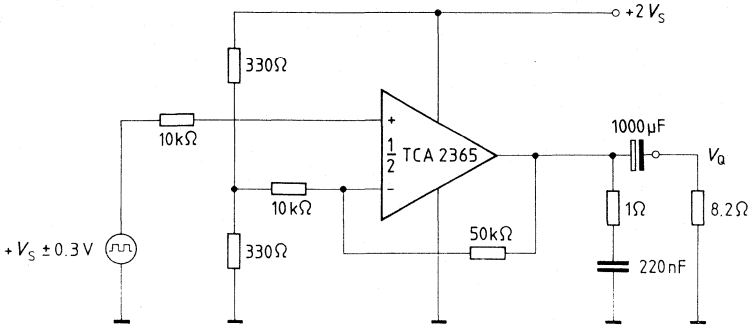
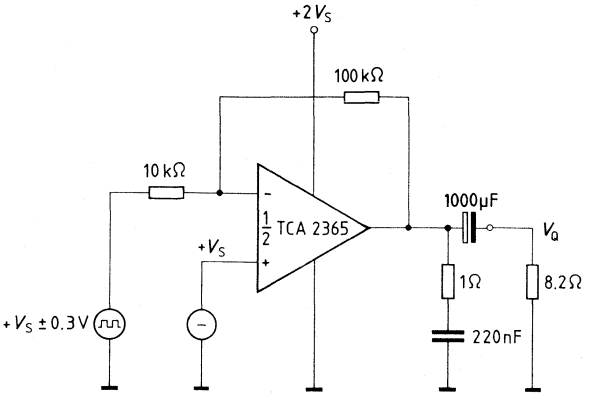
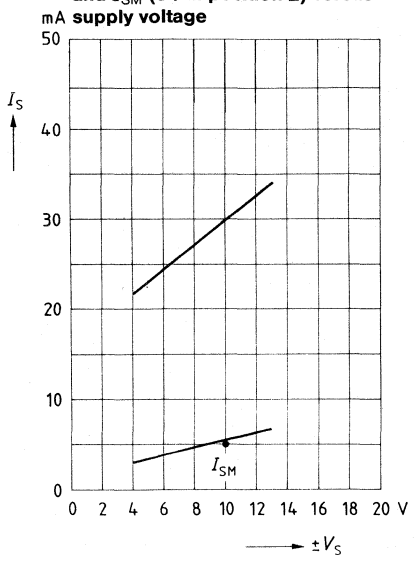


Figure 9 Slew rate for inverting operation

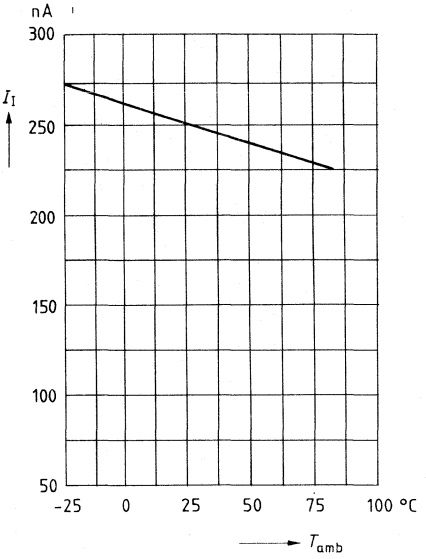


Characteristic curves

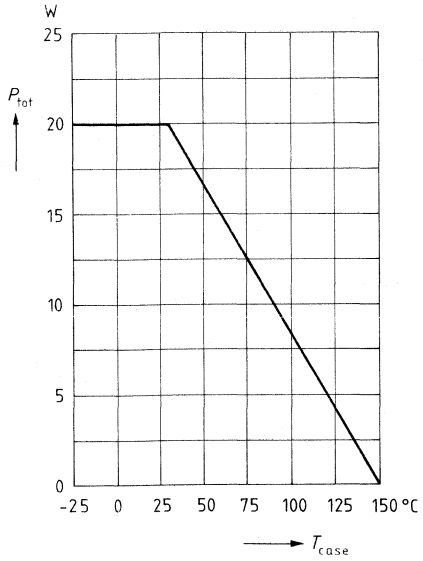
Supply current I_S (S1 in position 1) and I_{SM} (S1 in position 2) versus supply voltage



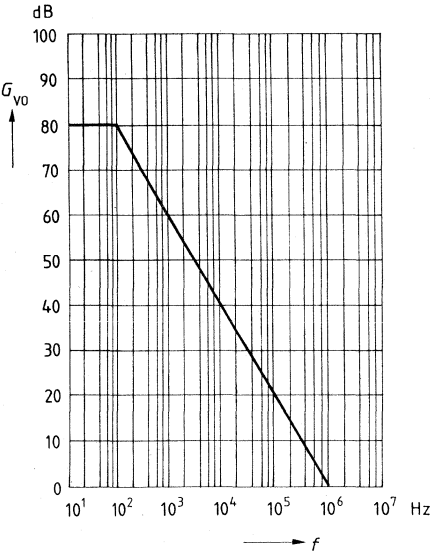
Input current versus ambient temperature



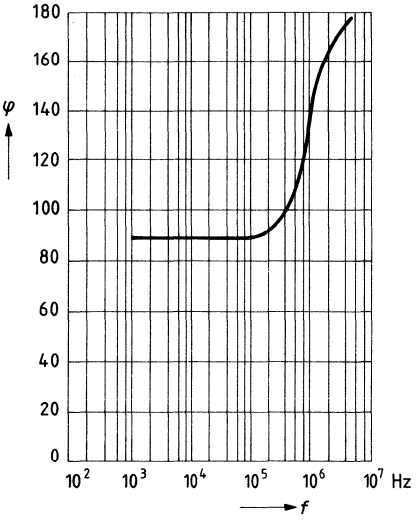
Max. permissible power dissipation versus case temperature



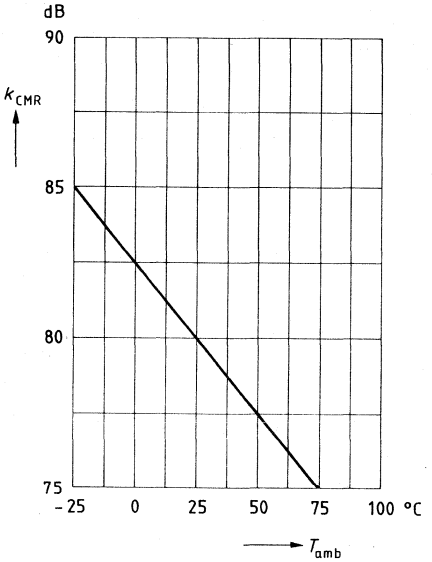
Open-loop voltage gain versus frequency



Phase response versus frequency



Common-mode rejection versus ambient temperature



Comparators
Threshold Switches

Bipolar IC

Type	Ordering code	Package	Color code	Fig. No.
TCA 105	Q67000-A527	DIP 6		5
TCA 105 B	Q67000-A587			
TCA 105 G[1])	Q67000-A988-G1	similar to SO 6	orange/white	25

TCA 105 contains an oscillator stage, a threshold switch, and two anti-valent output stages. These circuits are especially suitable for application in proximity switches, light barriers, and other contactless switching applications.

Features

- Wide range of supply voltage, 4.5 to 30 V
- High output current, 50 mA
- TTL-compatible
- Triggerable with dc signal

Maximum ratings		**TCA 105; G**	**TCA 105 B**	
Supply voltage	V_S	30	20	V
Output voltage (pin 4, pin 5)	V_Q	30	20	V
Output current	I_Q	50	50	mA
Switching frequency	f_S	40	40	kHz
Input voltage	V_I	≥ 0[2])	≥ 0[2])	V
Junction temperature	T_j	125	125	°C
Storage temperature range	T_{stg}	−55 to 125	−55 to 125	°C
Thermal resistance (system-air)				
TCA 105, TCA 105 B	$R_{th\ SA}$	115	115	K/W
TCA 105 G	$R_{th\ SA}$	200	200	K/W
Operating range				
Supply voltage range	V_S	4.75 to 30	4.75 to 20	V
Ambient temperature range	T_{amb}	−25 to 85	−25 to 85	°C
Oscillating frequency range	f_{OSC}	1 to 4.5	1 to 4.5	MHz

1) also available upon request in miniature plastic package (TCA 105 W)

2) negative input voltages are not permitted

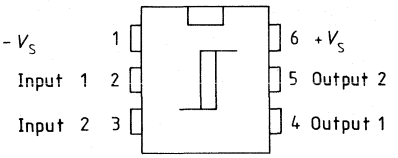
Characteristics

Static measurement, pins 3 and 1 interconnected
$V_S = 12$ V; $T_{amb} = 25$ °C; $R_C = 5.6$ kΩ

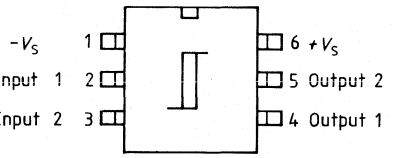
		min	typ	max	
Supply current	I_S		3.4	5	mA
Input threshold voltage with compensation resistor R_C	V_I	300	400	480	mV
Input threshold current	I_I		−60		µA
Hysteresis	V_{hy}	20	35	50	mV
L output voltage ($I_Q = 16$ mA)	V_{QL}		0.25	0.35	V
H output voltage	V_{QH}		corresponds to V_S		
Reverse current, $V_S = 30$ V and/or 20 V	I_{QH}			60	µA
L output voltage ($I_Q = 50$ mA)	V_{QL}		0.7	1.15	V
Switching time in TTL operation ($I_Q = 16$ mA)	t		3		µs

Pin configurations

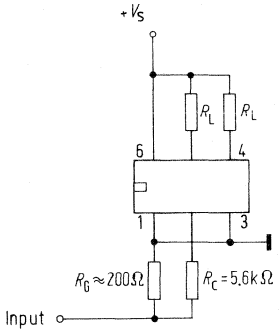
TCA 105, TCA 105 B



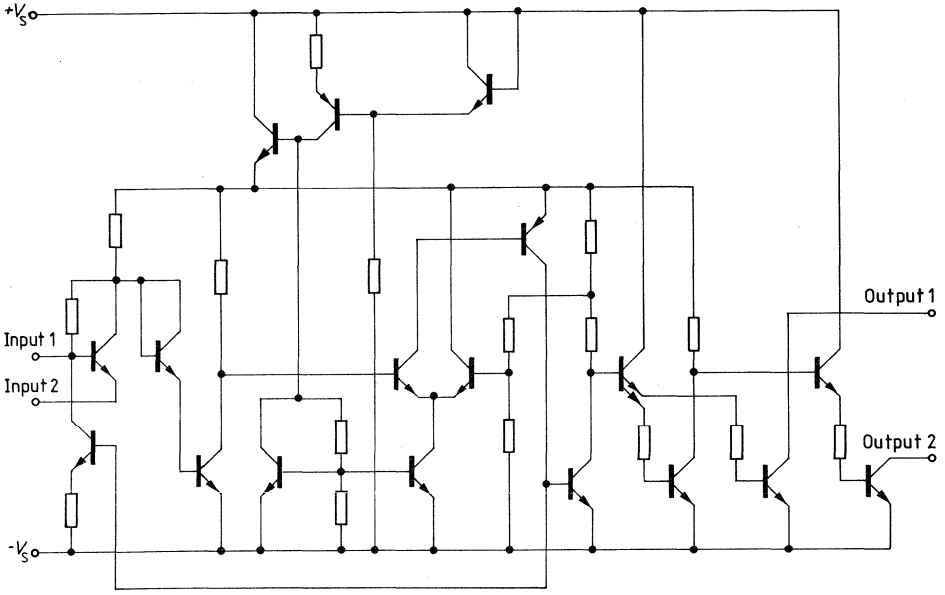
TCA 105 G



Measurement circuit

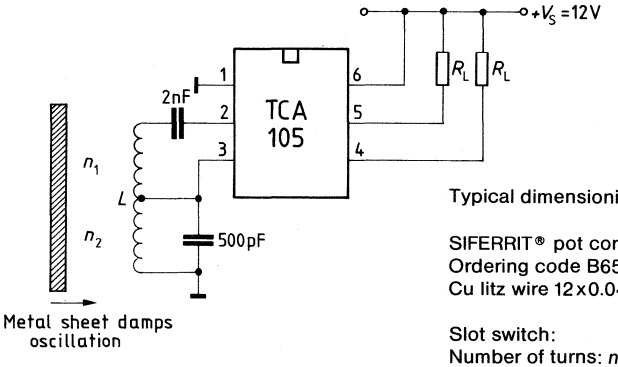


Circuit digram



Application examples

Inductive slot switch or proximity switch



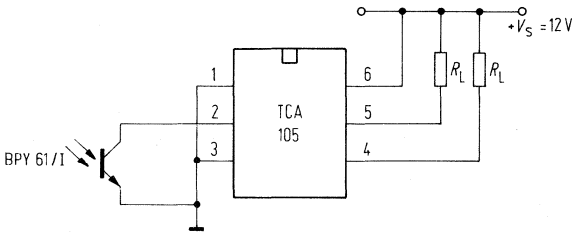
Typical dimensioning values:

SIFERRIT® pot cores, 9 mm dia.
Ordering code B65935-A-X25
Cu litz wire 12 x 0.04 mm

Slot switch:
Number of turns: $n = 2 \times 25$
Distance between pot core halves:
2.5 to 3.5 mm

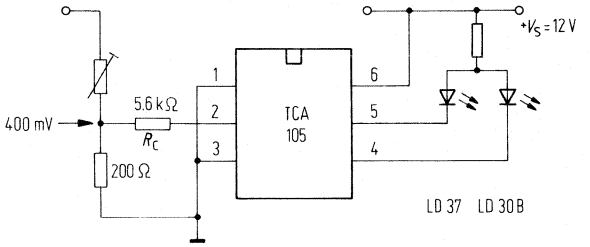
Proximity switch:
Number of turns: $n_1 = 8$, $n_2 = 40$
Distance: 2 to 3 mm

Light-operated switch (switching amplifier for phototransistor BPY 61)



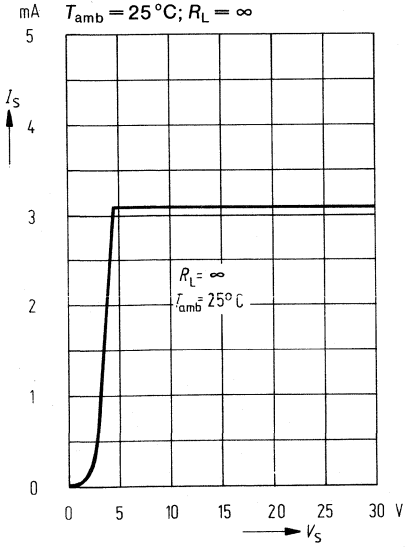
Application example

Voltage monitor



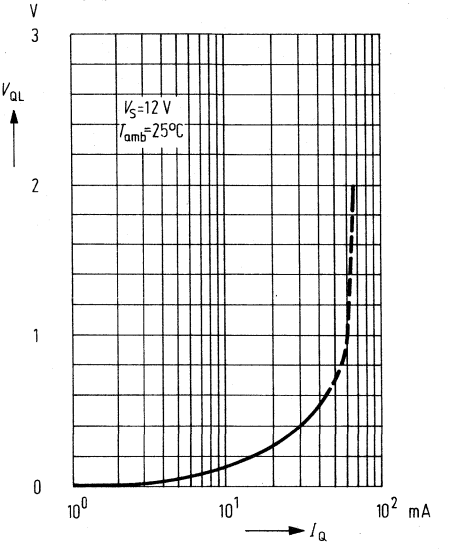
Current consumption
Supply current versus supply voltage

$T_{amb} = 25\,°C$; $R_L = \infty$

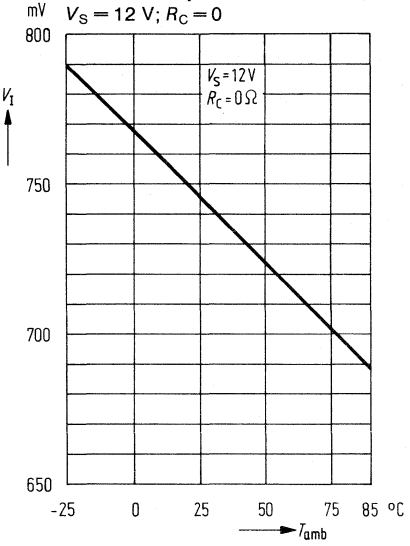


L output voltage versus output current

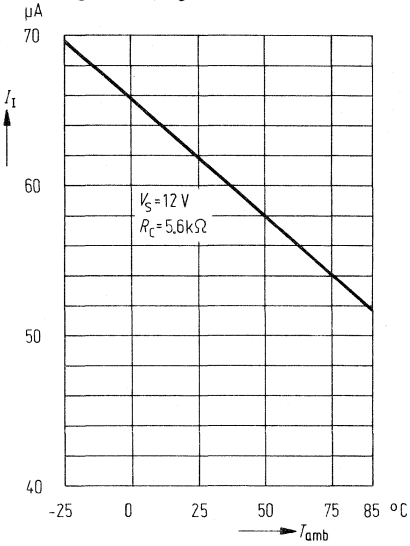
$T_{amb} = 25\,°C$; $V_S = 12$ V



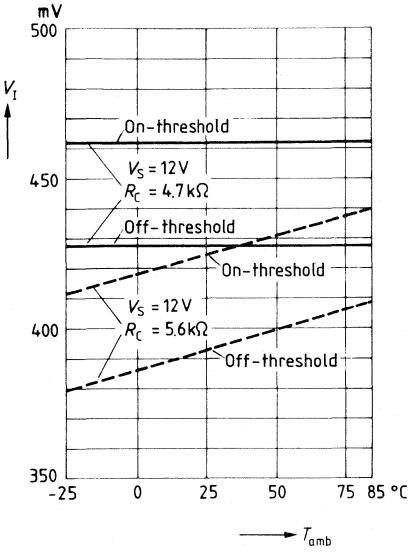
Switching threshold
Input voltage versus
ambient temperature
$V_S = 12$ V; $R_C = 0$



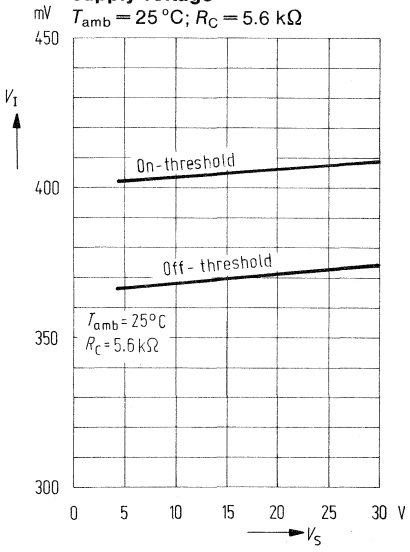
Input current versus
ambient temperature
$V_S = 12$ V; $R_C = 5.6$ kΩ



Switching threshold
Input voltage versus
ambient temperature



Switching threshold
Input voltage versus
supply voltage
$T_{amb} = 25$ °C; $R_C = 5.6$ kΩ

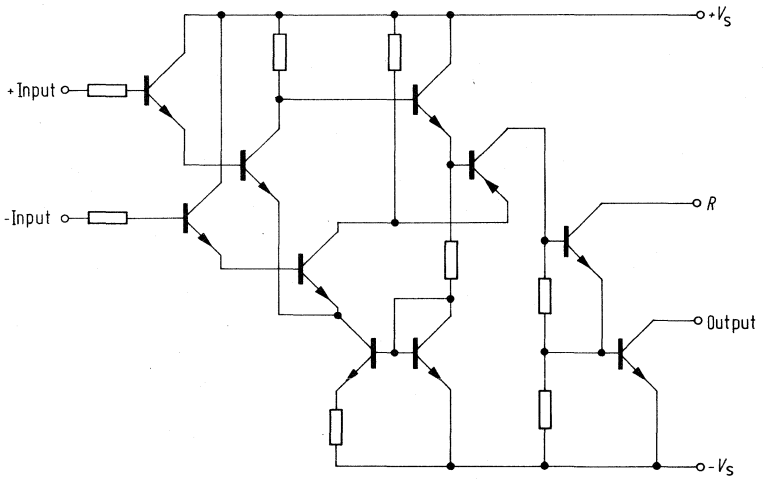


Type	Ordering code	Package	Color code	Fig. No.
TCA 312 A	Q67000-A2048	DIP 6	–	5
TCA 312 G	Q67000-A2509	similar to SO 6	red	25
TCA 315 A	Q67000-A561	DIP 6	–	5
TCA 315 G	Q67000-A1005-G1	similar to SO 6	red/yellow	25

TCA 312 and TCA 315 are suitable for use as Schmitt trigger or comparator in control engineering and automotive electronics. The output has been designed to control TTL circuits directly. In addition to high gain, low offset voltage, minor dependence on temperature and supply voltage, the amplifiers are outstanding for:

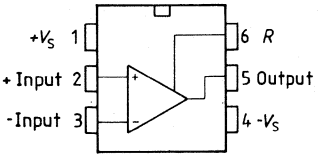
- Very high input resistance
- Wide common-mode range
- Large supply voltage range
- Large control range
- High output current
- Low output saturation voltage
- Wide temperature range (TCA 312 A)

Circuit diagram

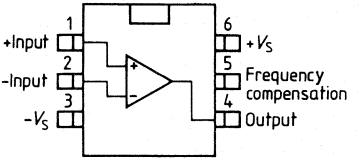


Pin configurations

TCA 312 A
TCA 315 A

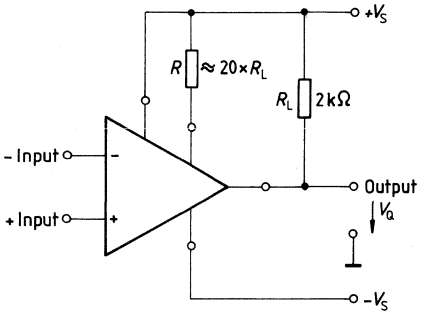


TCA 312 G
TCA 315 G



Connection diagram

R_L = load resistor



Maximum ratings

Supply voltage	V_S	± 15	V
Output current	I_Q	70	mA
Driver current	I_{dr}	10	mA
Differential input voltage V_S = 13 to 15 V	V_{ID}	± 13	V
Differential input voltage V_S = 2 to 13 V	V_{ID}	± V_S	V
Junction temperature	T_j	150	°C
Storage temperature range	T_{stg}	−55 to 125	°C
Thermal resistance (system-air) TCA 312 A	$R_{th\ SA}$	115	K/W
TCA 312 G	$R_{th\ SA}$	200	K/W

Operating range

Supply voltage range	V_S	± 2 to ± 15	V
Ambient temperature range	T_{amb}	−55 to 125	°C

Characteristics

V_S = ± 5 V to ± 15 V
R = 6.8 kΩ

		T_{amb} = 25 °C			T_{amb} = −55 to 125 °C		
		min	typ	max	min	max	
Open-loop supply current consumption	I_S		1.5	2.5		2.5	mA
Input offset voltage (R_G = 50 Ω)	V_{IO}	−10		10	−15	15	mV
Input offset current	I_{IO}	−5		5	−10	10	nA
Input current	I_I		5	15		25	nA
Input current (V_{ID} = ± 13 V)	I_I			200			nA
Output voltage (R_L = 2 kΩ, V_S = ± 15 V)	V_{Qpp}	14.9		−14.8	14.8	−14.6	V
(R_L = 620 Ω, V_S = ± 15 V)	V_{Qpp}	14.9		−14.0	14.8	−13.5	V
(R_L = 2 kΩ, V_S = ± 15 V, f = 100 kHz)	V_{Qpp}		± 10				V

Characteristics $V_S = \pm 5$ V to ± 15 V $R = 6.8$ kΩ		$T_{amb} = 25$ °C			$T_{amb} = -55$ to 125 °C		
		min	typ	max	min	max	
Input impedance ($f = 1$ kHz)	Z_i		3				MΩ
Open-loop voltage gain							
($R_L = 2$ kΩ, $f = 1$ kHz)	G_{V0}	80	83		75		dB
($R_L = 10$ kΩ, $f = 1$ kHz)	G_{V0}		88				dB
($R_L = 2$ kΩ, $f = 1$ MHz)	G_{V0}		60				dB
Common-mode input voltage range ($R_L = 2$ kΩ, $V_S = \pm 15$ V)	V_{IC}	13		−13	12	−12	V
Common-mode rejection ($R_L = 2$ kΩ)	k_{CMR}	75	80		70		dB
Supply voltage rejection ($G_V = 100$)	k_{SVR}		25	200		200	μV/V
Temperature coefficient of V_{IO} ($R_G = 50$ Ω)	α_{VIO}		12	50			μV/K
Temperature coefficient of I_{IO}	α_{IIO}		50				pA/K
Slew rate of V_q for non-inverting operation*) (see TAA 765, test circuit 1)	SR		30				V/μs
Output saturation voltage ($I_Q = 10$ mA)	V_{Qsat}			200		400	mV
Output reverse current	I_{QR}			1		5	μA
Characteristics $V_S = \pm 2$ V; $R = 6.8$ kΩ							
Input offset voltage ($R_G = 50$ Ω)	V_{IO}	−10		10	−15	15	mV
Input offset current	I_{IO}	−5		5	−10	10	nA
Input current	I_I		5	15		25	nA
Open-loop voltage gain ($R_L = 2$ kΩ, $f = 1$ kHz)	G_{V0}	75			70		dB

*) For the relationship between power bandwidth and slew rate refer to "General information" page 40

Maximum ratings

Supply voltage		V_S	± 15	V
Output current		I_Q	70	mA
Driver current		I_{dr}	10	mA
Differential input voltage V_S = 13 to 15 V		V_{ID}	± 13	V
Differential input voltage V_S = 2 to 13 V		V_{ID}	± V_S	V
Junction temperature		T_j	150	°C
Storage temperature range		T_{stg}	−55 to 125	°C
Thermal resistance (system-air)	TCA 315 A	$R_{th\ SA}$	115	K/W
	TCA 315 G	$R_{th\ SA}$	200	K/W

Operating range

Supply voltage range	V_S	± 2 to ± 15	V
Ambient temperature range	T_{amb}	−25 to 85 °C	°C

Characteristics

V_S = ± 5 V to ± 15 V
R = 6.8 kΩ

		T_{amb} = 25 °C			T_{amb} = −25 to 85 °C		
		min	typ	max	min	max	
Open-loop supply current consumption	I_S		1.5	2.5		2.5	mA
Input offset voltage (R_G = 50 Ω)	V_{IO}	−15		15	−18	18	mV
Input offset current	I_{IO}	−10		10	−20	20	nA
Input current	I_I		5	25		35	nA
Input current (V_{ID} = ± 13 V)	I_I			200			nA
Output voltage							
(R_L = 2 kΩ, V_S = ± 15 V)	V_{Qpp}	14.9		−14.8	14.8	−14.6	V
(R_L = 620 Ω, V_S = ± 15 V)	V_{Qpp}	14.9		−14.0	14.8	−13.5	V
(R_L = 2 kΩ, V_S = ± 15 V, f = 100 kHz)	V_{Qpp}		± 10				V

Characteristics
$V_S = \pm 5$ V to ± 15 V
$R = 6.8$ kΩ

		$T_{amb} = 25$ °C			$T_{amb} = -25$ to 85 °C		
		min	typ	max	min	max	
Input impedance ($f = 1$ kHz)	Z_i		3				MΩ
Open-loop voltage gain							
($R_L = 2$ kΩ, $f = 1$ kHz)	G_{V0}	75	80		75		dB
($R_L = 10$ kΩ, $f = 1$ kHz)	G_{V0}		85				dB
($R_L = 2$ kΩ, $f = 1$ MHz)	G_{V0}		60				dB
Common-mode input voltage range ($R_L = 2$ kΩ, $V_S = \pm 15$ V)	V_{IC}	13		−13	12	−12	V
Common-mode rejection ($R_L = 2$ kΩ)	k_{CMR}	70	78		70		dB
Supply voltage rejection ($G_V = 100$)	k_{SVR}		25	200		200	μV/V
Temperature coefficient of V_{IO} ($R_G = 50$ Ω)	α_{VIO}		12				μV/K
Temperature coefficient of I_{IO}	α_{IIO}		50				pA/K
Slew rate of V_q for non-inverting operation*) (see TAA 765, test circuit 1)	SR		30				V/μs
Output saturation voltage ($I_Q = 10$ mA)	V_{Qsat}			200		400	mV
Output reverse current	I_{QR}			10		20	μA

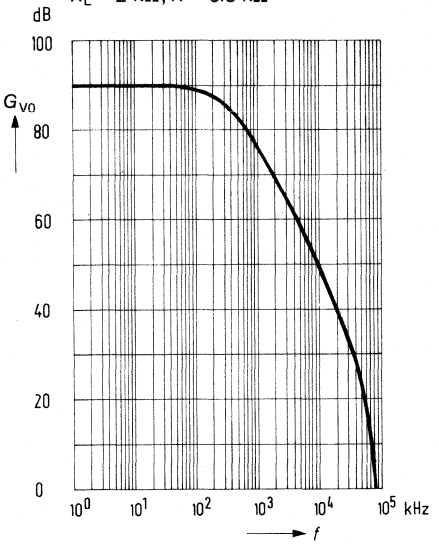
Characteristics
$V_S = \pm 2$ V; $R = 6.8$ kΩ

Input offset voltage ($R_G = 50$ Ω)	V_{IO}	−17		17	−20	20	mV
Input offset current	I_{IO}	−10		10	−20	20	nA
Input current	I_I		5	25		35	nA
Open-loop voltage gain ($R_L = 2$ kΩ, $f = 1$ kHz)	G_{V0}	70			70		dB

*) For the relationship between power bandwidth and slew rate refer to "General information" page 40

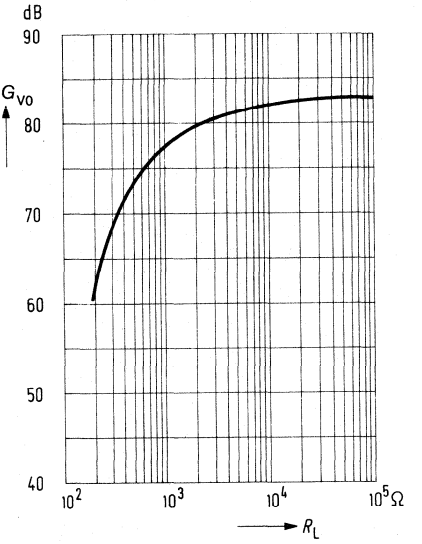
Open-loop voltage gain versus frequency

$R_L = 2\ k\Omega$; $R = 6.8\ k\Omega$



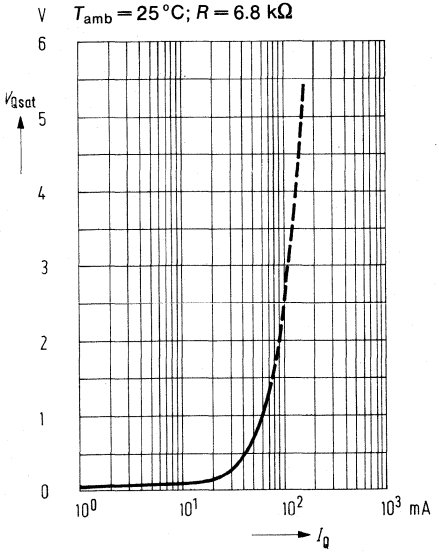
Open-loop voltage gain versus load resistance

$T_{amb} = 25\ °C$; $R = 6.8\ k\Omega$



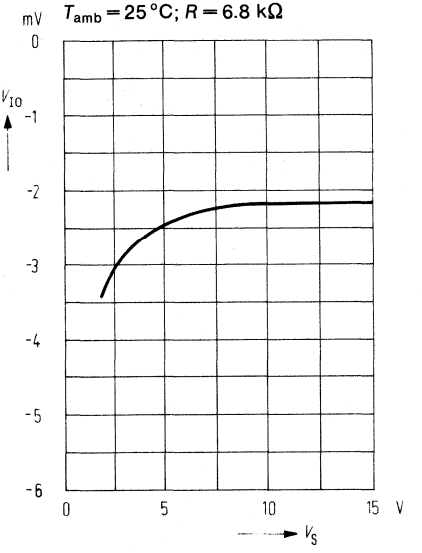
Output saturation voltage versus output current

$T_{amb} = 25\ °C$; $R = 6.8\ k\Omega$

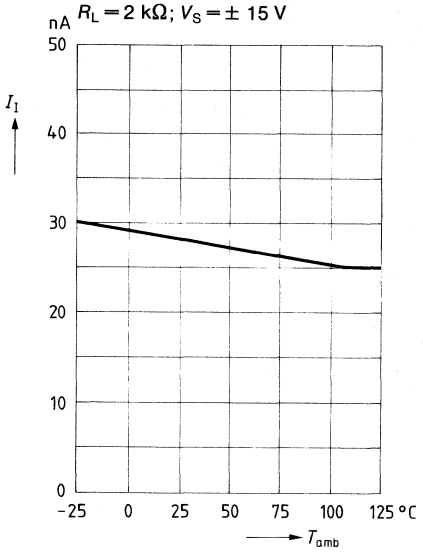


Input offset voltage versus supply voltage

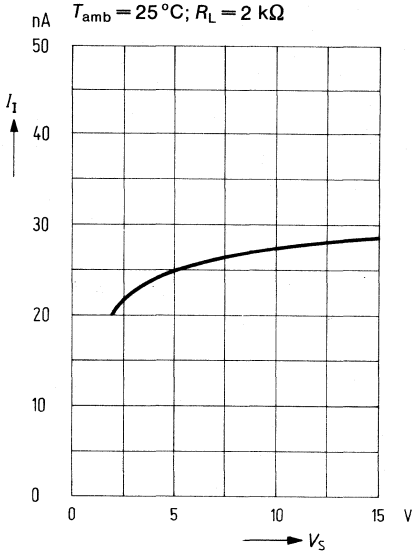
$T_{amb} = 25\ °C$; $R = 6.8\ k\Omega$



Input current versus ambient temperature
$R_L = 2\ k\Omega$; $V_S = \pm 15\ V$



Input current versus supply voltage
$T_{amb} = 25\ °C$; $R_L = 2\ k\Omega$



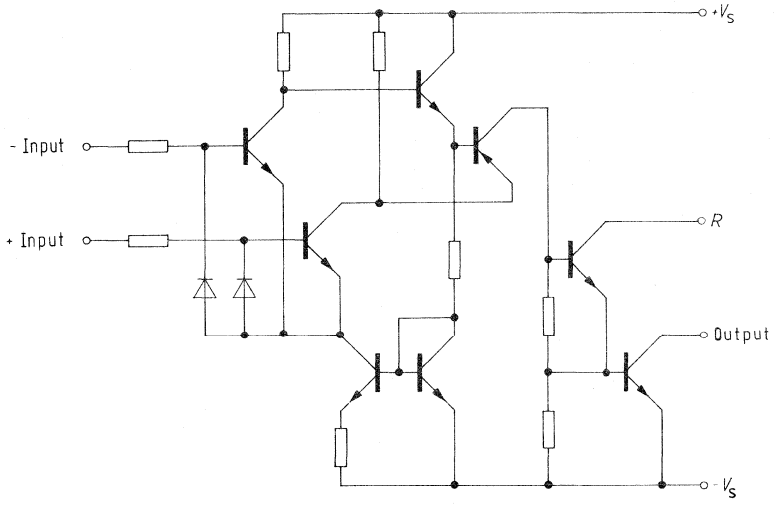
Bipolar IC

Type	Ordering code	Package	Color code	Fig. No.
TCA 322 A	Q67000-A2501	DIP 6	—	5
TCA 322 G	Q67000-A2508	similar to SO 6	brown	25
TCA 325 A	Q67000-A562	DIP 6	—	5
TCA 325 G	Q67000-A1012-G1	similar to SO 6	green/yellow	25

TCA 322 and TCA 325 are suitable for use as Schmitt trigger or comparator in control engineering and automotive electronics. The output has been designed to control TTL circuits directly. In addition to high gain, low offset voltage, minor dependence on temperature and supply voltage, the amplifiers are outstanding for:

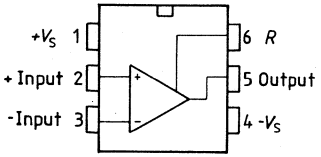
- Wide common-mode range
- Large supply voltage range
- Large control range
- High output current
- Low output saturation voltage
- Wide temperature range (TCA 322 A)

Circuit diagram

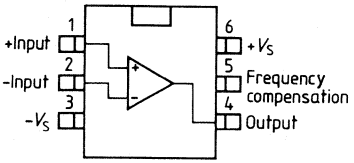


Pin configurations

TCA 322 A
TCA 325 A

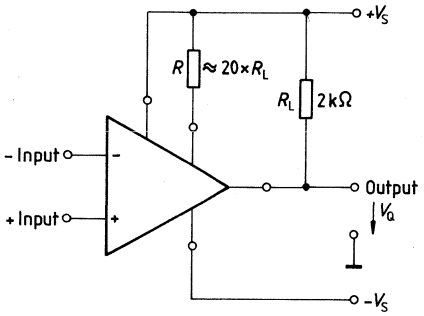


TCA 322 G
TCA 325 G



Connection diagram

R_L = load resistor



Maximum ratings

Supply voltage	V_S	± 15	V
Output current	I_Q	70	mA
Driver current at R	I_{dr}	10	mA
Differential input voltage	V_{ID}	± V_S	V
Junction temperature	T_j	150	°C
Storage temperature range	T_{stg}	−55 to 125	°C
Thermal resistance (system-air) TCA 322 A	$R_{th\ SA}$	115	K/W
TCA 322 G	$R_{th\ SA}$	200	K/W

Operating range

Supply voltage range	V_S	± 2 to ± 15	V
Ambient temperature range	T_{amb}	−55 to 125	°C

Characteristics

$V_S = \pm 5$ V to ± 15 V
$R = 6.8$ kΩ

		$T_{amb} = 25$ °C			$T_{amb} = -55$ to 125 °C		
		min	typ	max	min	max	
Open-loop supply current consumption	I_S		1.5	2.5		2.5	mA
Input offset voltage ($R_G = 50$ Ω)	V_{IO}	−4		4	−6	6	mV
Input offset current	I_{IO}	−100	± 50	100	−300	300	nA
Input current	I_I		0.3	0.7		1.0	µA
Output voltage							
($R_L = 2$ kΩ, $V_S = \pm 15$ V)	$V_{Q\ pp}$	14.9		−14.8	14.8	−14.6	V
($R_L = 620$ Ω, $V_S = \pm 15$ V)	$V_{Q\ pp}$	14.9		−14.0	14.8	−13.5	V
($R_L = 2$ kΩ, $V_S = \pm 15$ V, $f = 100$ kHz)	$V_{Q\ pp}$		± 10				V

Characteristics
$V_S = \pm 5$ V to ± 15 V
$R = 6.8$ kΩ

		$T_{amb} = 25$ °C			$T_{amb} = -55$ to 125 °C		
		min	typ	max	min	max	
Input impedance ($f = 1$ kHz)	Z_i		200				kΩ
Open-loop voltage gain							
($R_L = 2$ kΩ, $f = 1$ kHz)	G_{V0}	85	87		80		dB
($R_L = 10$ kΩ, $f = 1$ kHz)	G_{V0}		92				dB
($R_L = 2$ kΩ, $f = 1$ MHz)	G_{V0}		60				dB
Common-mode input voltage range ($R_L = 2$ kΩ, $V_S = \pm 15$ V)	V_{IC}	13		−13	12	−12	V
Common-mode rejection ($R_L = 2$ kΩ)	k_{CMR}	80	85		75		dB
Supply voltage rejection ($G_V = 100$)	k_{SVR}		25	200		200	μV/V
Temperature coefficient of V_{IO} ($R_G = 50$ Ω)	α_{VIO}		6	25			μV/K
Temperature coefficient of I_{IO} ($R_G = 50$ Ω)	α_{IIO}		0.3	1.5			nA/K
Slew rate of V_q for non-inverting operation*) (see TAA 765, test circuit 1)	SR		50				V/μs
Output saturation voltage ($I_Q = 10$ mA)	$V_{Q\,sat}$			200		400	mV
Output reverse current	I_{QR}			1		5	μA

Characteristics
$V_S = \pm 2$ V, $R = 6.8$ kΩ

Input offset voltage ($R_G = 50$ Ω)	V_{IO}	−4		4	−6	6	mV
Input offset current	I_{IO}	−70		70	−200	200	nA
Input current	I_I		0.2	0.5		0.8	μA
Open-loop voltage gain ($R_L = 2$ kΩ, $f = 1$ kHz)	G_{V0}	80			75		dB

*) For the relationship between power bandwidth and slew rate refer to "General information", page 40

Maximum ratings

Supply voltage		V_S	± 15	V
Output current		I_Q	70	mA
Driver current at R		I_{dr}	10	mA
Differential input voltage		V_{ID}	± V_S	V
Junction temperature		T_j	150	°C
Storage temperature range		T_{stg}	−55 to 125	°C
Thermal resistance (system-air)	TCA 325 A	$R_{th\ SA}$	115	K/W
	TCA 325 G	$R_{th\ SA}$	200	K/W

Operating range

Supply voltage range	V_S	± 2 to ± 15	V
Ambient temperature range	T_{amb}	−25 to 85	°C

Characteristics

$V_S = \pm 5$ V to ± 15 V
$R = 6.8$ kΩ

		$T_{amb} = 25$ °C			$T_{amb} = -25$ to 85 °C		
		min	typ	max	min	max	
Open-loop supply current consumption	I_S		1.5	2.5		2.5	mA
Input offset voltage ($R_G = 50$ Ω)	V_{IO}	−5.5		5.5	−7	7	mV
Input offset current	I_{IO}	−200	± 80	200	−300	300	nA
Input current	I_I		0.5	0.8		1.0	µA
Output voltage							
($R_L = 2$ kΩ, $V_S = \pm 15$ V)	$V_{Q\ pp}$	14.9		−14.8	14.8	−14.6	V
($R_L = 620$ Ω, $V_S = \pm 15$ V)	$V_{Q\ pp}$	14.9		−14.0	14.8	−13.5	V
($R_L = 2$ kΩ, $V_S = \pm 15$ V, $f = 100$ kHz)	$V_{Q\ pp}$		± 10				V

Characteristics
$V_S = \pm 5$ V to ± 15 V
$R = 6.8$ kΩ

		$T_{amb} = 25$ °C			$T_{amb} = -25$ to 85 °C		
		min	typ	max	min	max	
Input impedance ($f = 1$ kHz)	Z_i		200				kΩ
Open-loop voltage gain							
($R_L = 2$ kΩ, $f = 1$ kHz)	G_{V0}	80	85		80		dB
($R_L = 10$ kΩ, $f = 1$ kHz)	G_{V0}		90				dB
($R_L = 2$ kΩ, $f = 1$ MHz)	G_{V0}		60				dB
Common-mode input voltage range ($R_L = 2$ kΩ, $V_S = \pm 15$ V)	V_{IC}	13		−13	12	−12	V
Common-mode rejection ($R_L = 2$ kΩ)	k_{CMR}	75	83		75		dB
Supply voltage rejection ($G_V = 100$)	k_{SVR}		25	200		200	µV/V
Temperature coefficient of V_{IO} ($R_G = 50$ Ω)	α_{VIO}		6				µV/K
Temperature coefficient of I_{IO} ($R_G = 50$ Ω)	α_{IIO}		0.3				nA/K
Slew rate of V_q for non-inverting operation*) (see TAA 765, test circuit 1)	SR		50				V/µs
Output saturation voltage ($I_Q = 10$ mA)	$V_{Q\,sat}$			200		400	mV
Output reverse current	I_{QR}			10		20	µA

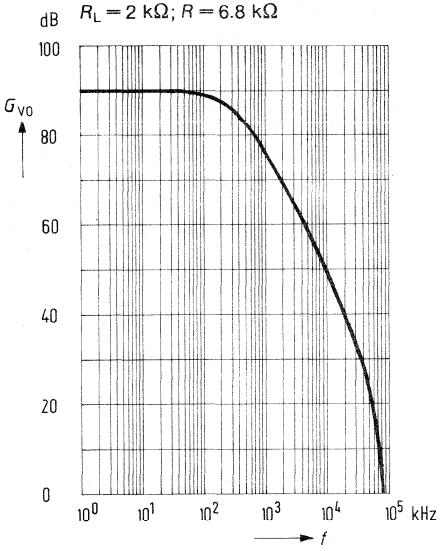
Characteristics
$V_S = \pm 2$ V, $R = 6.8$ kΩ

Input offset voltage ($R_G = 50$ Ω)	V_{IO}	−6		6	−7,5	7,5	mV
Input offset current	I_{IO}	−150		150	−200	200	nA
Input current	I_I		0.2	0.6		0.8	µA
Open-loop voltage gain ($R_L = 2$ kΩ, $f = 1$ kHz)	G_{V0}	75			75		dB

*) For the relationship between power bandwidth and slew rate refer to "General information", page 40

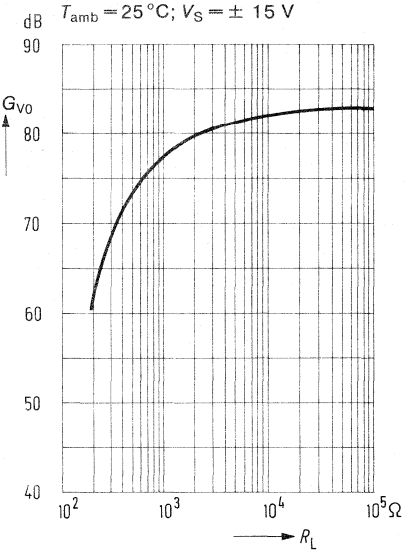
Open-loop voltage gain versus frequency

$R_L = 2\ k\Omega$; $R = 6.8\ k\Omega$



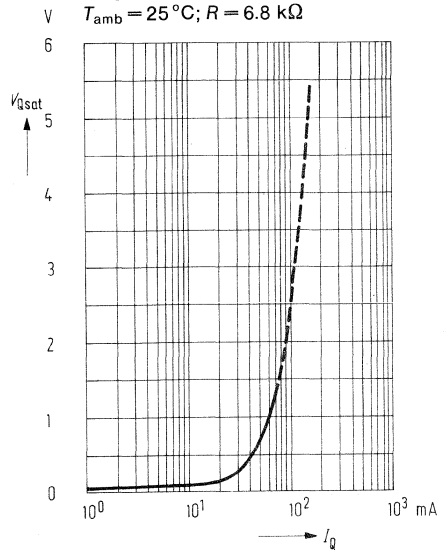
Open-loop voltage gain versus load resistance

$T_{amb} = 25\,°C$; $V_S = \pm\ 15\ V$



Output saturation voltage versus output current

$T_{amb} = 25\,°C$; $R = 6.8\ k\Omega$



Bipolar IC

Type	Ordering code	Package	Color code	Fig. No.
TCA 345 A	Q67000-A564	DIP 4	–	4
TCA 345 W	Q67000-A564-W	Miniature package, 6 pins	yellow/brown	23

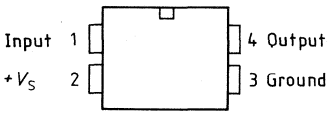
Threshold switches featuring linear, supply voltage-dependent threshold values. Inductive loads may be switched at the output without protective diode.

Features

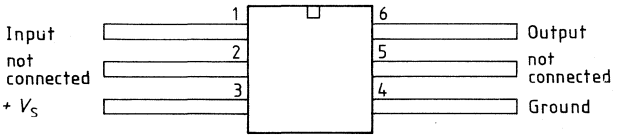
- TTL-compatible
- High output current
- Very high input impedance
- Good stability due to hysteresis
- Few external components

Pin configurations

TCA 345 A



TCA 345 W



Maximum ratings

Supply voltage	V_S	10	V
Output current	I_Q	70	mA
Input voltage	V_I	0 to V_S	V
Inductance at the output	L_Q	500	mH
Storage temperature range	T_{stg}	−55 to 125	°C
Junction temperature	T_j	125	°C
Thermal resistance (system-air) TCA 345 A	$R_{th\ SA}$	140	K/W
TCA 345 W	$R_{th\ SA}$	200	K/W

Operating range

Supply voltage range	V_S	2 to 10	V
Ambient temperature range	T_{amb}	−25 to 85	°C

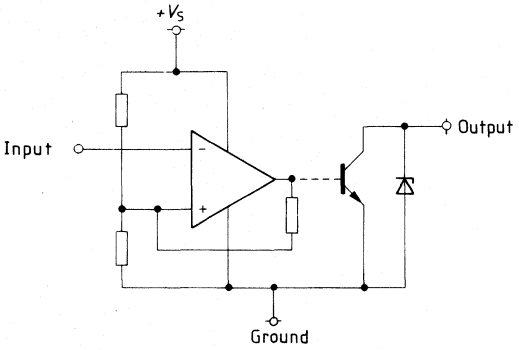
Characteristics

$T_{amb} = 25$ °C

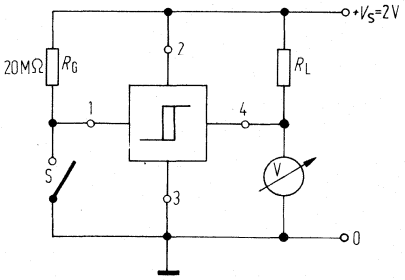
		min	typ	max	
Current consumption at output current					
$I_Q = 0$ mA; $V_S = 2$ V	$I_{S\,H}$		0.55	0.80	mA
$= 5$ V	$I_{S\,H}$		1.35	2.00	mA
$I_Q = 40$ mA; $V_S = 2$ V	$I_{S\,L}$		1.85	3.00	mA
$= 5$ V	$I_{S\,L}$		7.00	9.00	mA
L output voltage at $I_Q = 40$ mA $V_S = 2$ V	$V_{Q\,L}$		150	300	mV
Output reverse current $V_Q = 10$ V	I_{QH}			30	µA
Switching threshold ($V_S = 2$ to 10 V)[1]	V_I	$0.63 \times V_S$	$0.66 \times V_S$	$0.69 \times V_S$	V
Linearity error of the switching threshold (referred to $V_S = 2$ V)				3.0	%
Hysteresis (in % of V_S) $V_S = 2$ V	ΔV_I	6.0	10	15	%
Hysteresis (in % of V_S) $V_S = 5$ V	ΔV_I	6.0	20		%
Hysteresis (in % of V_S) $V_S = 10$ V	ΔV_I	6.0	20		%
Input current	I_I		10	30	nA
Z voltage via output	V	11.0	13.6	15.0	V
Temperature response of switching threshold			30		ppm/K

1) measured with increasing input voltage

Circuit diagram

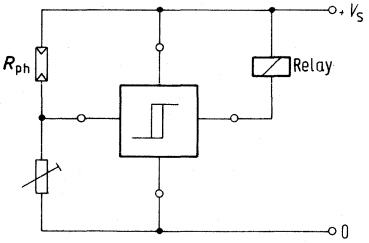


Test circuit

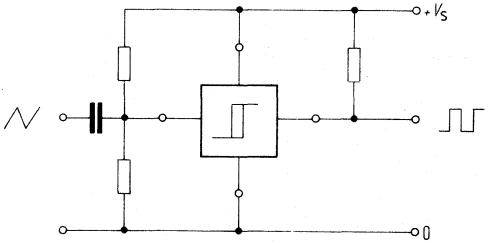


Application circuits

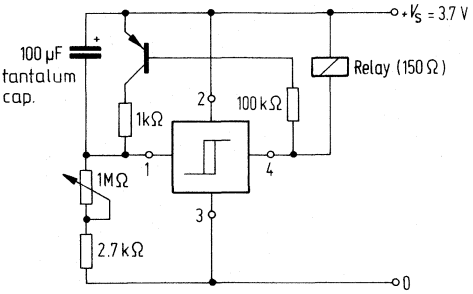
Twilight switch
(switches on light at nightfall)



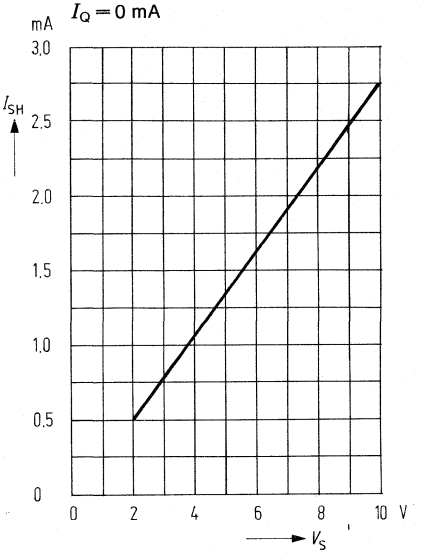
Triangle-square converter



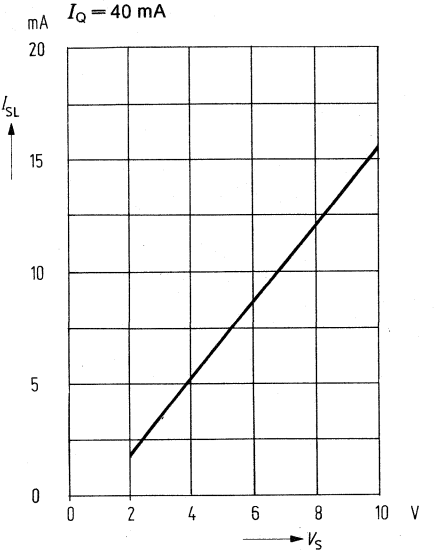
Clock generator



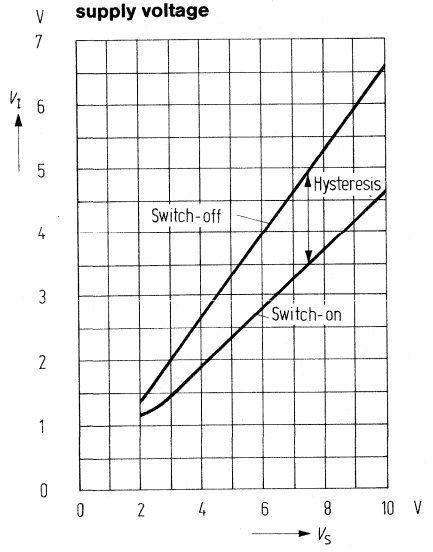
Current consumption I_{SH} versus supply voltage
$I_Q = 0$ mA



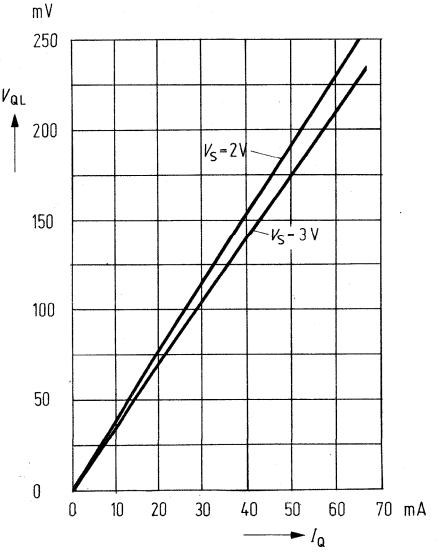
Current consumption I_{SL} versus supply voltage
$I_Q = 40$ mA



Switching threshold Input voltage versus supply voltage



L output voltage versus output current

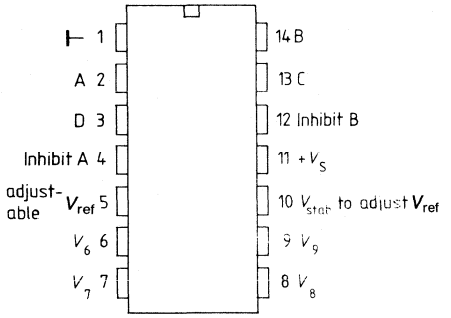


Bipolar IC

Type	Ordering code	Package	Fig. No.
TCA 965	Q67000-A982	DIP 14	7

The TCA 965 window discriminator is particularly suited for control systems as follow-up and adjusting control device with dead space. It can also be used in measuring systems for the selection of elements whose dc values should remain within tolerated deviations from required values.

Pin configuration



Maximum ratings

Supply voltage	V_S	27	V
Input voltage difference between inputs 6, 7 and 8	V_I	15	V
Input voltage (pin 9)	V_I	30	V
Output current (pin 2, 3, 13, 14)	I_Q	50	mA
Stabilized voltage output current (pin 10)	I_Q	10	mA
Junction temperature	T_j	125	°C
Storage temperature range	T_{stg}	−55 to 125	°C
Thermal resistane (system-air)	$R_{th\ SA}$	80	K/W

Operating range

Supply voltage range	V_S	4.75 to 27	V
Ambient temperature range	T_{amb}	−25 to 85	°C

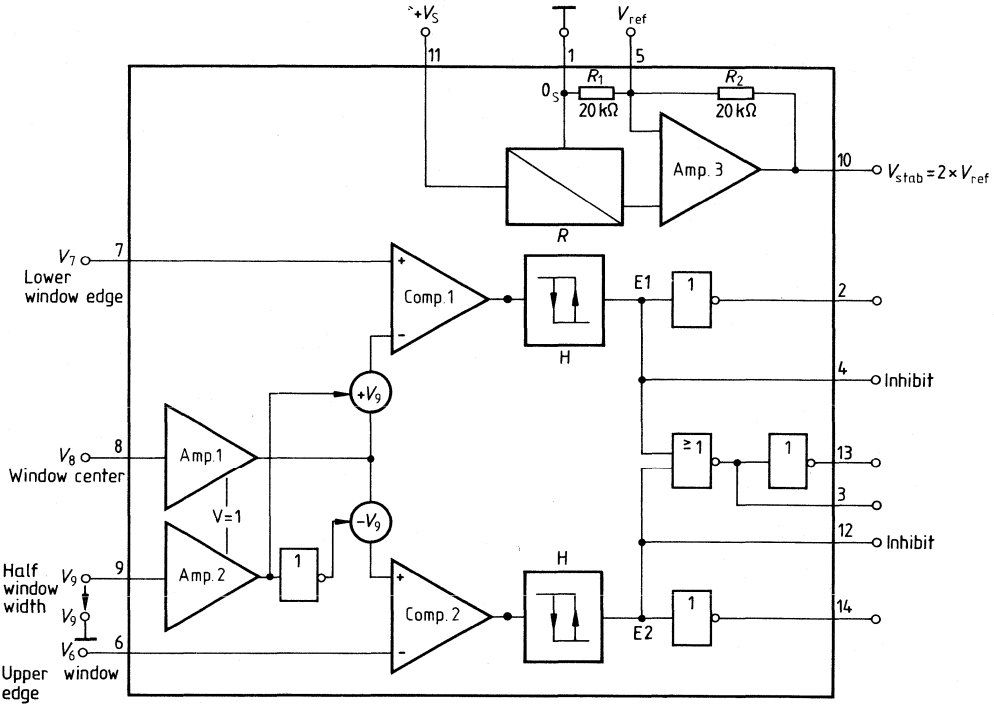
Characteristics

$V_S = 10$ V; $T_{amb} = 25$ °C

		Test conditions	min	typ	max	
Current consumption	I_S	V_2, $V_{13} = V_{QH}$		5	7	mA
Input current (pin 6, 7, 8)	I_I			20	50	nA
Input current (pin 9)	$-I_I$			400	3000	nA
Input offset voltage (pin 6/8, pin 7/8)	V_{IO}		−20	± 10	20	mV
Input voltage range (pin 6, 7, 8)	V_I	$\Delta V_I < 13$ V	1.5		$V_S - 1.0$	V
Input voltage range (pin 9)	V_I		50		$\frac{V_S}{2}$	mV
Differential input voltage	$V_6 - (V_8 - V_9)$				13	V
	$(V_8 + V_9) - V_7$				13	V
Reference voltage	V_5	$I_{ref} = 0$	2.8	3.0	3.2	V
Stabilized voltage	V_{10}	$V_S > 7.9$ V	5.5	6	6.5	V
Temperature coefficient of reference voltage	αV_5			0.5		mV/K
Sensitivity of reference voltage to supply voltage variations	$\frac{\Delta V_5}{\Delta V_S}$			3		mV/V
Output reverse current	I_{QH}				10	µA
L output voltage	V_{QL}	$I_Q = 10$ mA			200	mV
		$I_Q = 40$ mA			800	mV
Hysteresis (window edges)	V_{hy}		18	22	35	mV
Inhibit threshold[1]	$V_{4,12}$			1.5		V
Inhibit current	$I_{4,12}$			−100		µA

1) Inhibition occurs if pin 4 and 12 are grounded.

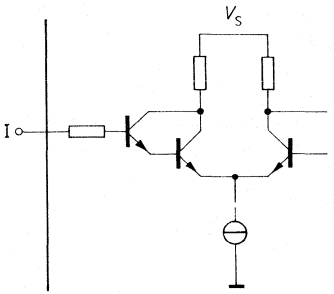
Block diagram



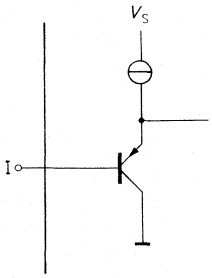
Schematic circuit diagrams

Inputs

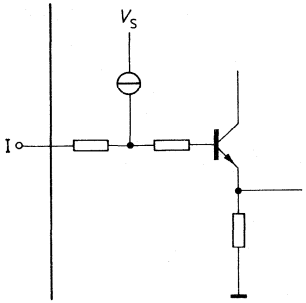
Pin 6, 7, 8



Pin 9

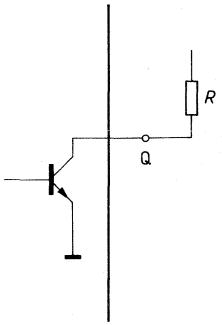


Pin 4, 12

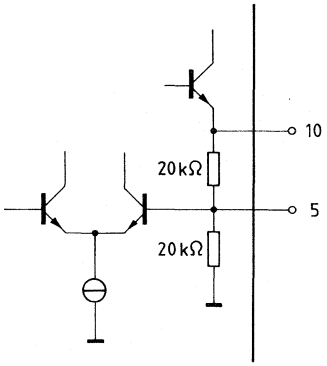


Outputs

Pin 2, 3, 13, 14



Pin 5, 10



Suggestions for application

The window discriminator analyzes the input voltage with reference to two limits that are input as voltages. The window, within which the circuit reacts »well« can be input either by an upper (V_6) and a lower limit (V_7), or by the window center (V_8) and depending upon that, by a voltage ΔV, (V_9), which corresponds to half window width and is available to ground. A Schmitt trigger characteristic with a small hysteresis is effective at the switching points. Four output signals are available having the following meanings: input signal inside, outside the window (good, bad), too high, too low. All outputs have open collectors that can carry up to 50 mA for the control of small relays, lamps, LEDs. All the usual logic families can be driven directly requiring only few external components.

Additionally, the IC contains a reference voltage source with adjustable amplifier (V_{ref}) for the generation of various reference voltages (V_{stab}) for the inputs. The reference voltage source is, to a large extent, independent of temperature and supply voltage. For stabilization purposes, it requires a capacitor of up to 10 µF (electrolytic capacitor) to ground at pin 10.

Truth table (for block diagram in connection with application circuit I and II).

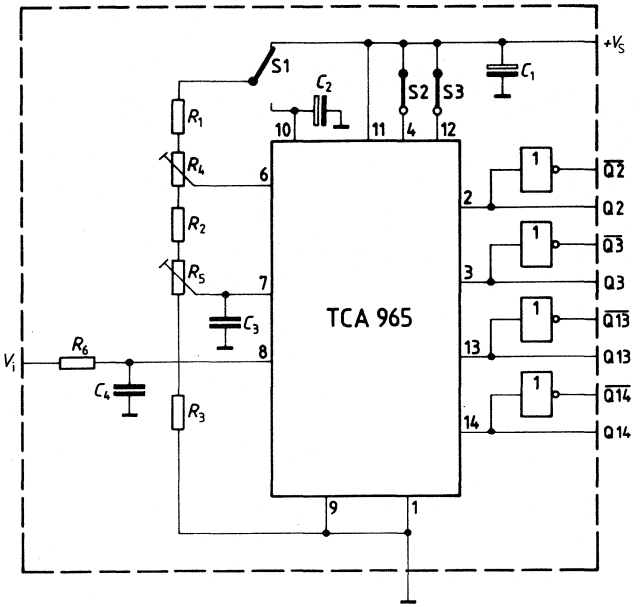
V_I	
Application circuit I $V_I = V_8$	Application circuit II $V_I = V_{6/7}$
$V_8 < (V_7 - V_9)$	$V_{6/7} > (V_8 + V_9)$
$V_8 > (V_6 + V_9)$	$V_{6/7} < (V_8 - V_9)$
$(V_6 + V_9) > V_8 > (V_7 - V_9)$	$(V_8 + V_9) > V_{6/7} > (V_8 - V_9)$
$V_6 + V_9$ – – – upper window edge $V_7 - V_9$ – – – lower window edge $(V_6 + V_9) - (V_7 - V_9)$ – – – – window width	V_8 – – – window center V_9 – – – half window width (to ground)

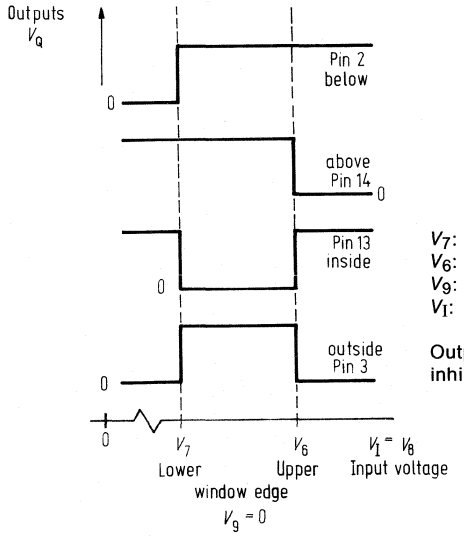
Outputs			
pin 2	14	13	3
L(H)	H(H)	H(L)	L(H)[1]
H(H)	L(H)	H(L)	L(H)[2]
H	H	L	H

Values in brackets refer to external inhibition via pin 4 and pin 12
[1] inhibition pin 4 to ground
[2] inhibition pin 12 to ground

Application circuit I

Outputs: pin 2 »below«
pin 3 »outside«
pin 13 »inside«
pin 14 »above«



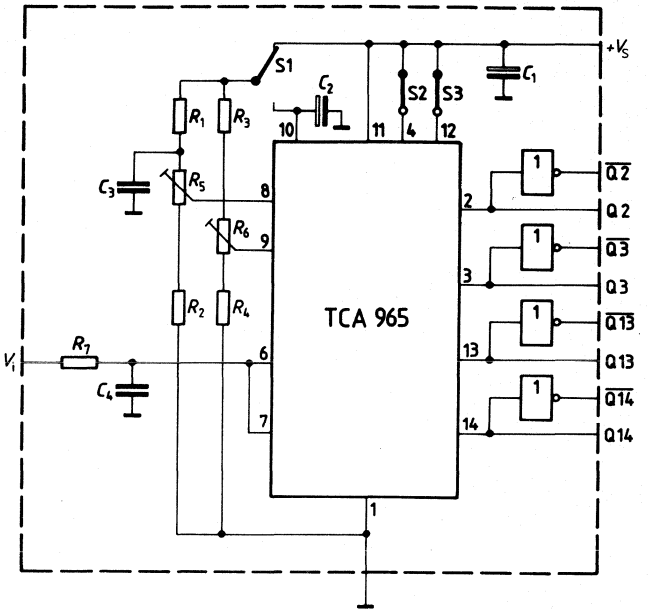


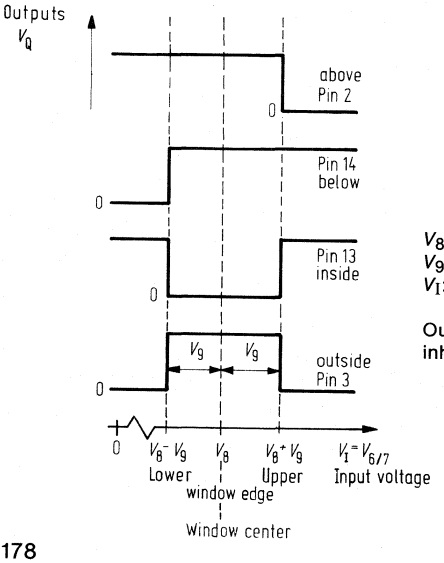
V_7: lower threshold
V_6: upper threshold
V_9: 0 V
V_I: at pin 8

Outputs pin 2 and pin 14 can be inhibited externally and are then H.

Application circuit II

Outputs: pin 2 »above«
pin 3 »outside«
pin 13 »inside«
pin 14 »below«





V_8: window center
V_9: ± half window width
V_I: pin 6 and pin 7 connected

Outputs pin 2 and pin 14 can be inhibited externally and are then H.

Examples of circuit-board design for application circuits I and II

The inputs of the TCA 965 window discriminator have a Schmitt-trigger characteristic. With an input voltage that crosses the switching threshold very slowly there is nevertheless a risk of the output concerned going into oscillation before it clearly assumes the new switching state. The following circuit boards were designed specially to allow for this factor and offer a maximum possible safeguard against oscillations.

The causes of the undesired response are as follows:

1. **Feedback effect** of the switched load on the window-edge voltage through loading or unloading of the supply voltage.
2. **Hum voltages** that are superimposed on the input signal or the window-edge voltages derived from the supply voltage.
3. Unfavorable **routing of the tracks** on the circuit board with the voltage dividers for the window edges connected to a point of the grounding that alters in potential as a result of load variations. Pin 1 of the TCA 965 can take a load current of 2 x 50 mA to ground.

Remedies for 1

Boundary conditions for non-oscillating operation	
Application circuit I $V_6 = k \cdot V_S$, $V_7 = k' \cdot V_S$	Application circuit II $V_8 = k \cdot V_S$, $V_9 = k' \cdot V_S$
Condition $k \cdot \Delta V_S < V_{hy\,min}$ $k' \cdot \Delta V_S < V_{hy\,min}$	Condition $(k + k') \cdot \Delta V_S < V_{hy\,min}$

If these conditions are not fulfilled, no holding up of the window-edge voltages with capacitors will help. Instead one of the following three measures must be taken:

use of V_{stab} for deriving the window-edge voltages,

- isolation of the supply voltage V'_S for the load from the supply voltage V_S of the TCA 965,
- increase of the edge hysteresis according to the technical note on the TCA 965.

Remedies for 2

Boundary condition

$V_{hum\ pp}/2 < V_{hy\ min}$

What decides fulfilment of the boundary condition is, depending on the particular application circuit, the sum of the hum voltages affecting the comparator concerned. The following interference suppression measures are suggested:

filtering of the input and window-edge voltage,

increase of the edge hysteresis[1].

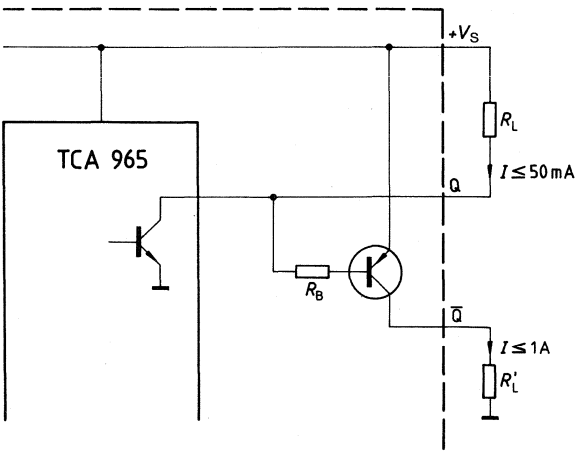
Remedies for 3

The circuit-board suggestions for the two application circuits have optimal grounding to the voltage dividers for the window edges with filtering of the supply voltage directly on the IC.

If several of the above-mentioned causes occur simultaneously, the remedies should be applied in the given sequence.

Output wiring

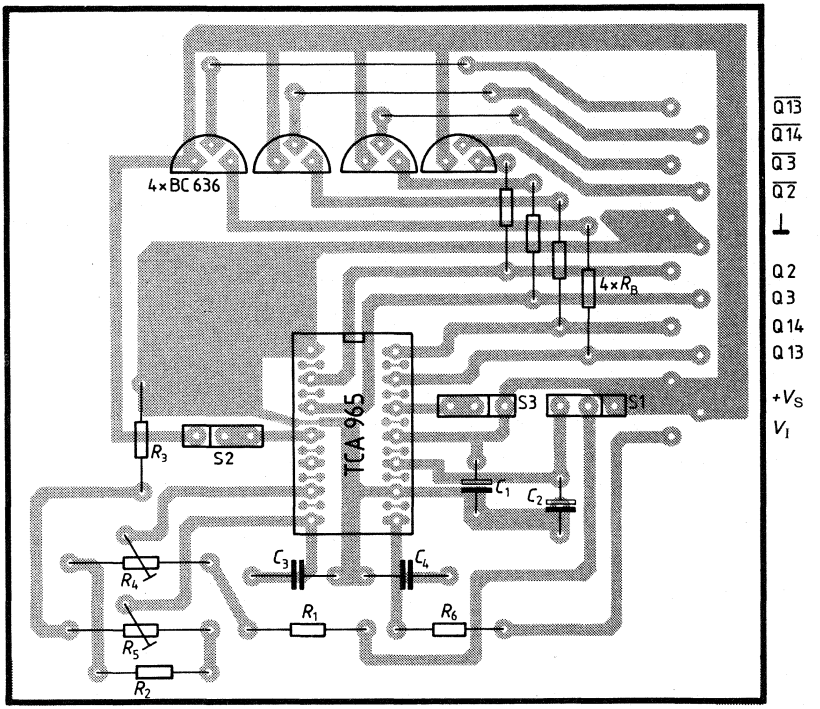
There are additional driver stages at the outputs of the TCA 965 as shown in the following diagram for switching load currents up to 1 A (outputs $\overline{Q}$)



1) Outputs 2, 3, 13, 14

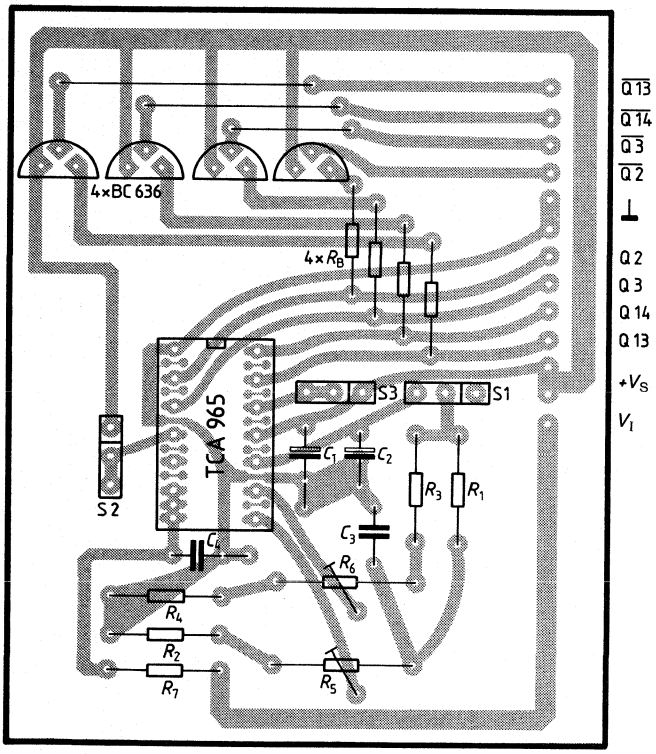
Circuit board and component layout

Application circuit I



Circuit board and component layout

Application circuit II



ICs for Switched-Mode Power Supplies
Control ICs

Control IC for Switched-Mode Power Supplies

TDA 4600-2
TDA 4600-2 D

Bipolar IC

Type	Ordering code	Package	Fig. No.
TDA 4600 – 2	Q67000-A2190	SIP 9	21
TDA 4600 – 2 D	Q67000-A2171	DIP 18 L9 (Pin 6 and pin 10 to 18 are connected to ground)	11

In addition to their use with TV receivers and video recorders, the ICs TDA 4600-2 and TDA 4600-2 D can be applied in power supplied of hi-fi sets and active speakers due to their wide operational ranges and superior voltage stability during high load changes.

Features

- Direct driving of switching transistor
- Low start-up current
- Reversing linear overload characteristic
- Collector current – proportional to base-current input

Maximum ratings

Supply voltage	V_9	20	V
Voltages			
reference output	V_1	6	V
identification input	V_2	± 0.6	V
controlled amplifier	V_3	3	V
collector current simulation	V_4	7	V
blocking input	V_5	7	V
base current cut-off point	V_7	V_9	V
base current amplifier output	V_8	V_9	V
Currents			
feedback, zero passage	$I_{i\,2}$	−3 to 3	mA
controlled amplifier	$I_{i\,3}$	−3 to 3	mA
collector current simulation	$I_{i\,4}$	5	mA
base current cut-off point	$I_{q\,7}$	1.5	mA
base current amplifier output	$I_{q\,8}$	−1.5	mA
Thermal resistances			
junction-air TDA 4600 – 2	$R_{th\,JA}$	70	K/W
junction-case TDA 4600 – 2	$R_{th\,JC}$	15	K/W
junction-air TDA 4600 – 2 D[1]	$R_{th\,JA}$	60	K/W
junction-air TDA 4600 – 2 D[2]	$R_{th\,JA\,1}$	44	K/W
Junction temperature	T_j	125	°C
Storage temperature range	T_{stg}	−55 to 125	°C

Operating range

Supply voltage range	V_9	7.8 to 18	V
Case temperature range TDA 4600 – 2	T_{case}	0 to 85	°C
Ambient temperature range TDA 4600 – 2 D[3]	T_{amb}	0 to 70	°C

1) Package soldered in PCB without cooling area

2) Package soldered in PCB with copper-clad 35 µ layer, cooling area 25 cm²

3) $R_{th\,JA\,1} = 44$ K/W and $P_V = 1$ W

Characteristics

T_{amb} = 25 °C, according to test circuit 1 and diagram

		min	typ	max	
Start operation					
Current consumption (V_1 not yet switched on)					
V_9 = 2 V	I_9			0.5	mA
V_9 = 5 V	I_9		1.5	2.0	mA
V_9 = 10 V	I_9		2.4	3.2	mA
Switching point for V_1	V_9	11	11.8	12.3	V
Normal operation (V_9 = 10 V; $V_{control}$ = −10 V; V_{clock} = ±0.5 V; f = 20 kHz; duty cycle 1:2) after switch on					
Current consumption $V_{control}$ = −10 V	I_9	110	135	160	mA
$V_{control}$ = 0 V	I_9	55	85	110	mA
Reference voltage I_1 < 0.1 mA	V_1	4.0	4.2	4,5	V
I_1 = 5 mA	V_1	4.0	4.2	4.4	V
Temperature coefficient of reference voltage	TC_1		10^{-3}		1/K
Feedback voltage	V_2*)		0.2		V
Control voltage $V_{control}$ = 0 V	V_3	2.3	2.6	2.9	V
Collector current simulation voltage					
$V_{control}$ = 0 V	V_4*)	1.8	2.2	2.5	V
$V_{control}$ = 0 V/−10 V	ΔV_4*)	0.3	0.4	0.5	V
Blocking input voltage	V_5	5.5	6.3	7.0	V
Output voltage $V_{control}$ = 0 V	V_{q7}*)	2.7	3.3	4.0	V
$V_{control}$ = 0 V	V_{q8}*)	2.7	3.4	4.0	V
$V_{control}$ = 0 V/−10 V	ΔV_{q8}*)	1.4	1.8	2.2	V
Safety operation (V_9 = 10 V; $V_{control}$ = −10 V; V_{clock} = ±0.5 V; f = 20 kHz; duty cycle 1:2)					
Current consumption (V_5 < 1.8 V)	I_9	14	22	28	mA
Switch-off voltage (V_5 < 1.8 V)	V_{q7}	1.3	1.5	1.8	V
	V_4	1.8	2.1	2.5	V
Ext. blocking input					
enable voltage $V_{control}$ = 0 V	V_5		2.4	2.7	V
disable voltage $V_{control}$ = 0 V	V_5	1.8	2.2		V
Supply voltage					
for V_8 blocked $V_{control}$ = 0 V	V_9	6.7	7.4	7.8	V
Supply voltage for V_1 off (while further decreasing V_9)	ΔV_9	0.3	0.6	1.0	V

Characteristics

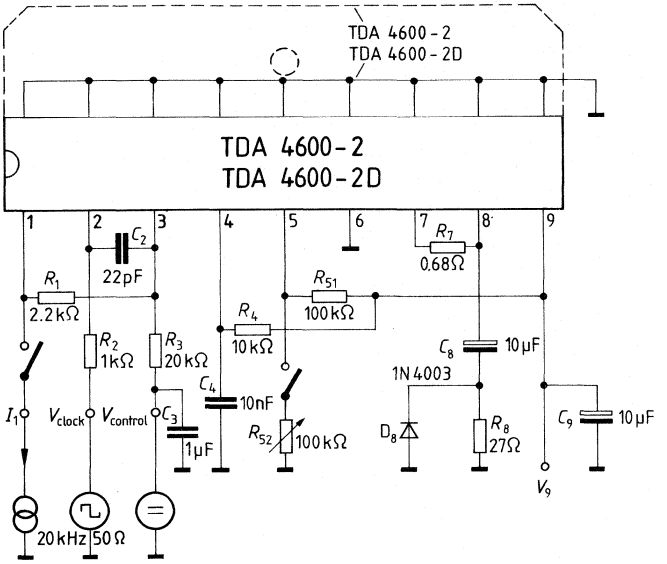
T_{amb} = 25 °C, according to test circuit 2

Switch-on time (secondary voltages)	t_{on}		350	450	ms
Voltage change					
S3 = closed (ΔN_3 = 20 W)	ΔV_2		100	500	mV
Sound output power					
S2 = closed (ΔN_2 = 15 W)	ΔV_2		500	1000	mV
Standby operation					
(secondary useful load = 3 W)					
S1 = open	ΔV_2		20	30	V
	f	70	75		kHz
	$N_{primary}$		10	12	VA

The cooling area should be optimized according to the limit values (T_{amb}, T_j, R_{thJC}, R_{thJA}, R_{thJA1})

*) only dc part

Measurement circuit 1



Circuit description

During start-up, normal and overload operations the TDA 4600-2; or -2D regulates, controls and protects the switching transistor installed in the flyback converter power supplies.

I) Start-up operation

The start-up operation is divided into three consecutive phases:

1. An internal reference voltage is built up which supplies the voltage regulator and effects the charging of the coupling electrolytic capacitor and the switching transistor. During these procedures an I_9 current less than 3.2 mA will be maintained, if the supply voltage V_9 does not exceed ≈ 12 V.
2. At V_9 ≈ 12 V an internal reference voltage V_1 = 4 V is suddenly released to provide all IC components with the exception of the control logic with a thermally stable and overload-resistant current.
3. In concurrence with the release of the reference voltage the control logic is activated by an additional stabilization circuit, and the IC is now ready for operation.

Above sequential start-up phases ensure the charging of the switching transistor by the coupling electrolytic capacitor and subsequent precision switching.

II) Normal operation

Zero passages of the feedback coil are registered at pin 2 and forwarded to the control logic.

At pin 3 (input control, overload, and standby recognition) the rectified amplitude variations of the feedback coil are applied. The regulating (control) amplifier operates with an input voltage of about 2 V and a current of about 1.4 mA. According to the internal reference voltage, the operating region of the regulating amplifier will be defined by the collector current simulation pin 4 and the overload recognition. The simulation of the collector current is generated by an external *RC* network at pin 4 and an internally set voltage level. By increasing the capacitance (10 nF), the collector current of the switching transistor is increased as well and establishes the desired control range. The control range extends between a 2 V clamped dc voltage and an ac voltage rising as a sawtooth wave, which may vary up to a maximum amplitude of 4 V (reference voltage).

By reducing the secondary load to 20 W, the switching frequency increases to about 50 kHz at an almost constant pulse duty factor (on-time to period approx. 1/3). During additional secondary load reduction to about 1 W, the switching frequency will change to approx. 70 kHz, while the pulse duty factor falls to approx. 1/11. At the same time, the collector peak current falls below 1 A.

The output level of the regulating (control) amplifier, the overload recognition, and the collector current simulation are compared in the trigger and the control logic is instructed accordingly. Pin 5 will provide additional blocking alternatives, i.e. the output at pin 8 is blocked at a voltage of equal to or less than 2.2 V at pin 5.

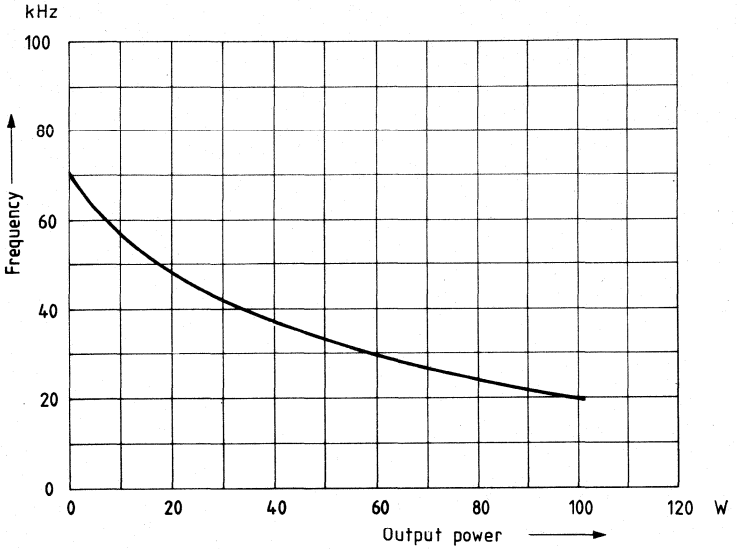
Based on the start-up circuit, the zero crossing identification, and the trigger-activated release, the control logic flipflops are set which control both the base current amplification and shut-down. The base current amplifier forwards the sawtooth voltage V_4 to pin 8. Also, a current feedback with an external resistance of $R \approx 0.68\ \Omega$ is inserted between pin 8 and pin 7. The resistance value determines the maximum amplitude of the base current for the switching transistor.

III) Safety features

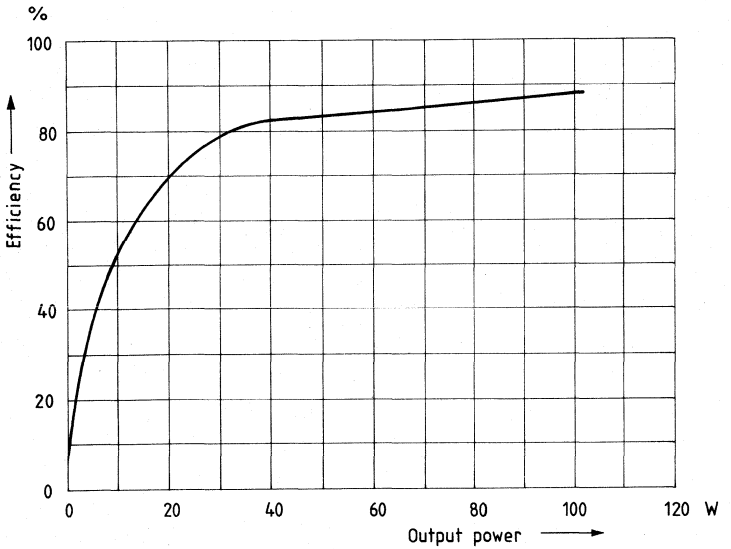
The base current shut-down, released by the control logic, clamps the output of pin 7 at 1.6 V and thus blocks the driving of the switching transistor. This preventive method will go into effect, if the voltage at pin 9 falls below typ. 7.4 V or if voltages of less than typ. 22 V are present at pin 5. In case of short-circuited secondary windings in the SMPS, the fault condition will be continuously monitored by the IC.

With the load completely removed from the secondary winding in the SMPS, the IC is set at a small pulse duty factor. The total power consumption of the SMPS is kept below $n = 6$ to 10 W during both operating conditions. After the output has been blocked at a supply voltage V_9 of less than or equal to typ. 7.4 V, an additional voltage reduction of $\Delta V_9 = 0.6$ V will switch off the reference voltage (4 V).

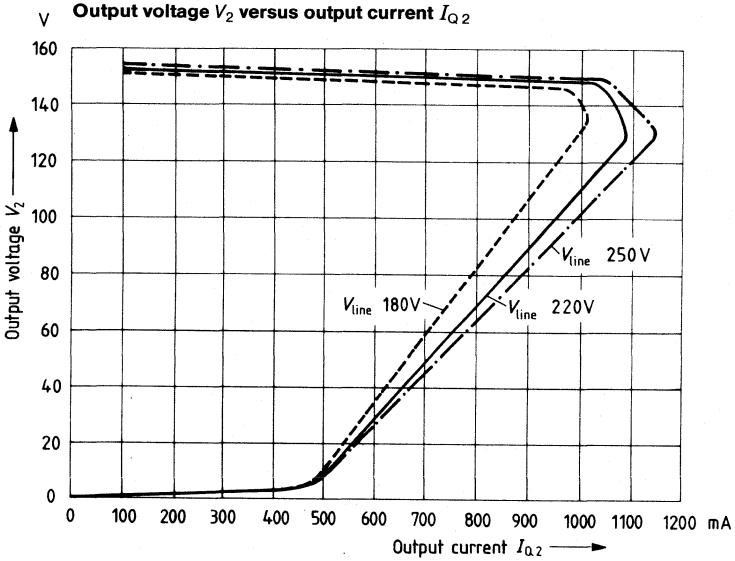
Frequency versus output power



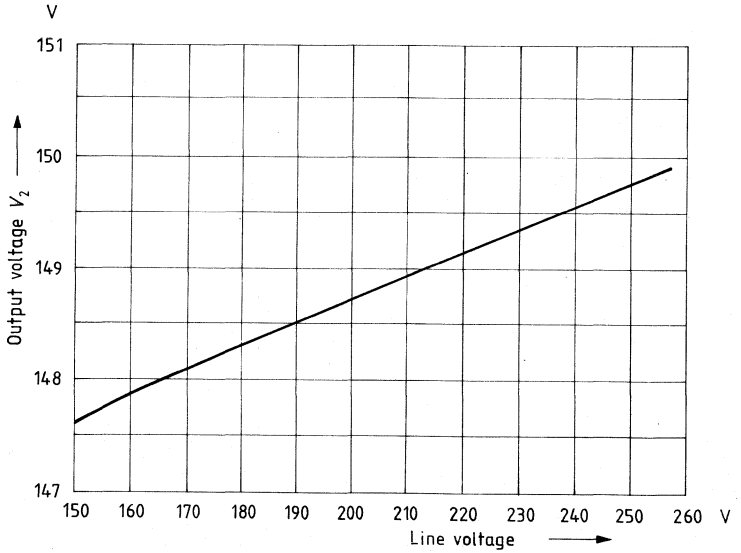
Efficiency versus output power



Load characteristic
Output voltage V_2 versus output current I_{Q2}



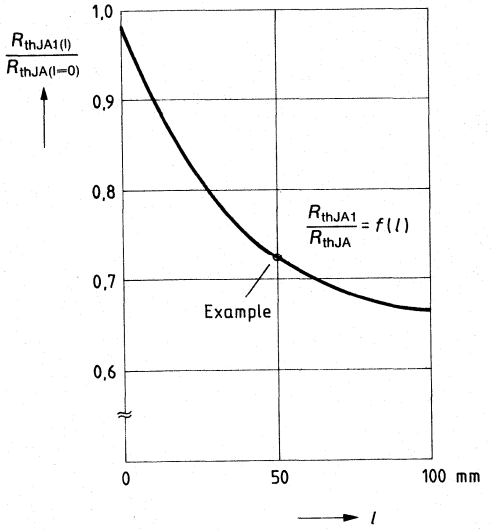
Output voltage V_2 versus line voltage alterations



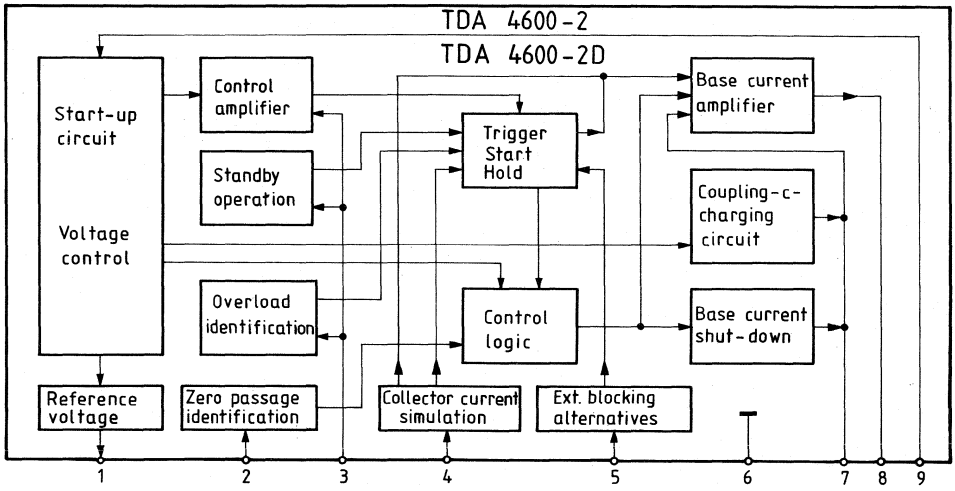
Thermal resistance (only applicable to TDA 4600-2 D)

Standardized, ambience-related thermal resistance $R_{th\ JA\,1}$ versus lateral length l of a square copper-clad cooling area (35 µm copper lamination).

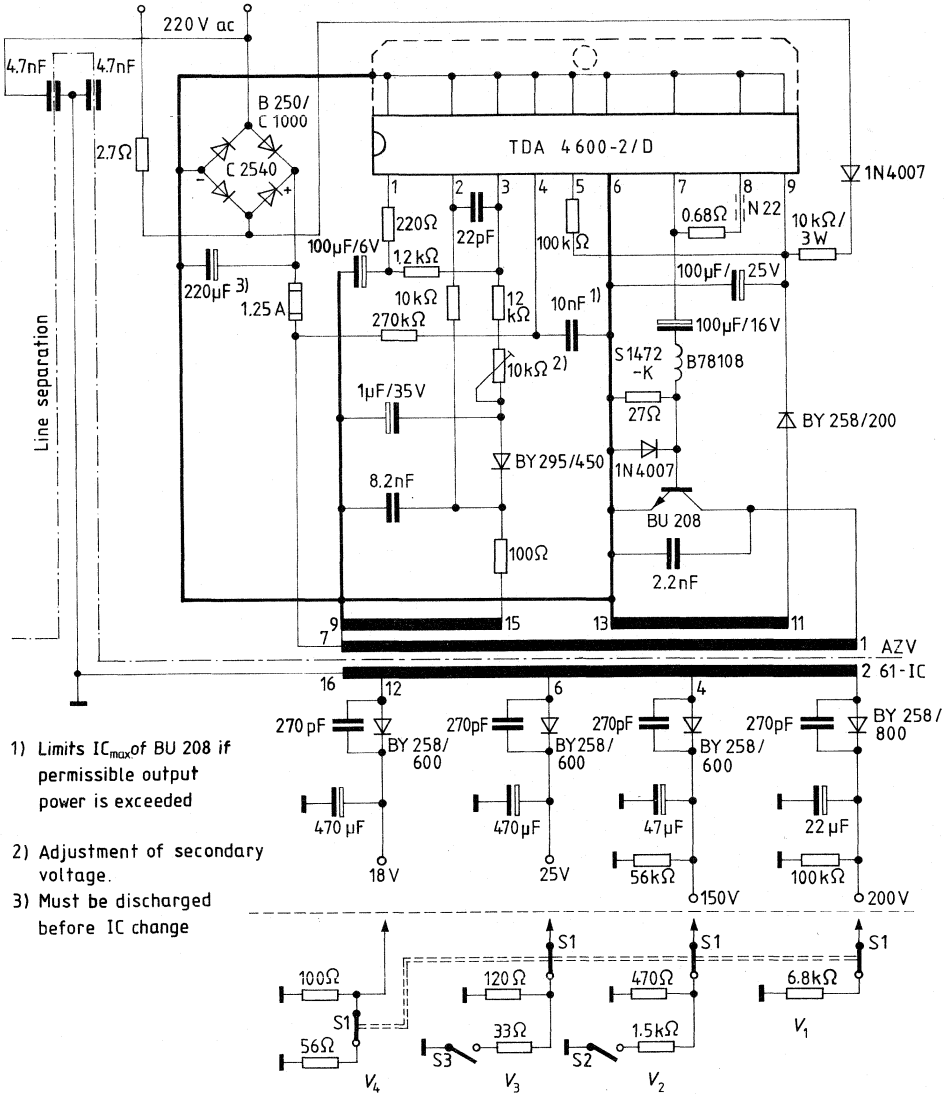
$R_{th\ JA}$ ($l = 0$) = 60 K/W
$T_{amb} \leq 70$ °C
$P_V = 1$ W
PCB in vertical position
circuit in vertical position
static air



Block diagram



Measurement circuit 2 and application circuit

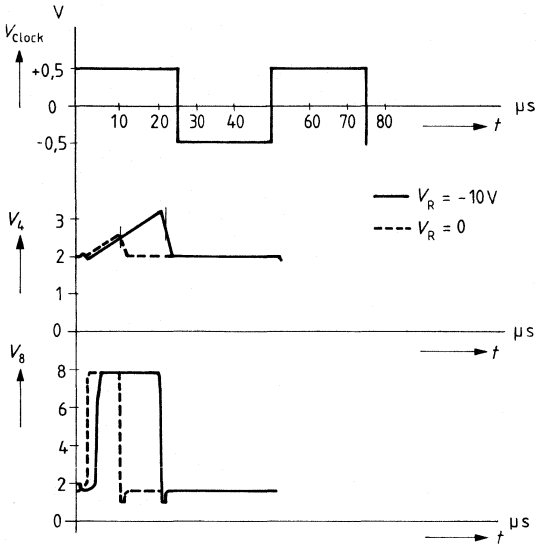


1) Limits IC_{max} of BU 208 if permissible output power is exceeded

2) Adjustment of secondary voltage.

3) Must be discharged before IC change

Measurement diagram for overload operations



Pin configuration

Pin No.	Function
1	V_{ref} output
2	Zero passage identification
3	Input regulating amplifier, overload amplifier
4	Collector current simulation
5	Possible connection for additional protective circuit
6	Ground
7	DC voltage output for charging the coupling capacitor
8	Pulse output – driving the switching transistor
9	Current supply input

only applicable to TDA 4600-2D

10 11 12 13 14 15 16 17 18	interconnected (ground)

Control IC for Switched-Mode Power Supplies

TDA 4601
TDA 4601 D

Bipolar IC

Type	Ordering code	Package	Fig. No.
TDA 4601	Q67000-A2379	SIP 9 (lead frame: pin 6 rigidly connected to substrate mounting plate)	22
TDA 4601 D	Q67000-A2390	DIP 18 (pin 6 and pins 10 to 18 connected to ground)	11

During start-up, normal and overload operations the TDA 4601 or – D regulates, controls and protects the switching transistor installed in the flyback converter power supplies. It also protects the complete SMPS by preventing an increase in the secondary voltage in case of errors. In addition to their use with TV receivers and video recorders, these ICs can be applied in power supplies of hi-fi sets and active speakers due to their wide operational ranges and superior voltage stability during high load changes.

Features

- Direct driving of switching transistor
- Low start-up current
- Reversing linear overload characteristic
- Collector current – proportional to base-current input
- Protective circuit for the event of errors

Maximum ratings

		Lower limit	Upper limit	
Supply voltage	V_9	0	20	V
Voltages				
reference output	V_1	0	6	V
zero-passage identification	V_2	−0.6	0.6	V
control amplifier	V_3	0	3	V
collector-current simulation	V_4	0	8	V
blocking input	V_5	0	8	V
base-current cut-off point	V_7	0	V_9	V
base-current amplifier output	V_8	0	V_9	V
Currents				
zero-passage identification	I_{I2}	−3	3	mA
control amplifier	I_{I3}	−3	3	mA
collector-current simulation	I_{I4}	0	5	mA
blocking input	I_{I5}	0	5	mA
base-current cut-off point	I_{Q7}	0	1.5	mA
base-current amplifier output	I_{Q8}	−1.5	0	mA
Thermal resistance				
junction-air TDA 4601	$R_{th\ JA}$		70	K/W
junction-case TDA 4601	$R_{th\ JC}$		15	K/W
junction-air TDA 4601 D[1]	$R_{th\ JA}$		60	K/W
junction-air TDA 4601 D[2]	$R_{th\ JA\ 1}$		44	K/W
Junction temperature	T_j		125	°C
Storage temperature	T_{stg}	−55	125	°C

Operating range

Supply voltage range		V_9	7.8 to 18	V
Case temperature range	TDA 4601	T_{case}	0 to 85	°C
Ambient temperature range[3]	TDA 4601 D	T_{amb}	0 to 70	°C

1) Package soldered in PCB without cooling area.
2) Package soldered in PCB with copper-clad 35-µm layer, cooling area 25 cm²
3) $R_{th\ JA\ 1} = 44$ K/W and $P_V = 1$ W

Characteristics

$T_{amb} = 25$ °C
according to test circuit 1 and diagram

		min	typ	max	
Start operation					
Current consumption (V_1 not yet applied)					
$V_9 = 2$ V	I_9			0.5	mA
$V_9 = 5$ V	I_9		1.5	2.0	mA
$V_9 = 10$ V	I_9		2.4	3.2	mA
Switching point for V_1	V_9	11.0	11.8	12.3	V
Normal operation					
($V_9 = 10$ V; $V_{control} = -10$ V; $V_{clock} = \pm 0.5$ V; $f = 20$ kHz; duty cycle 1 : 2) after switch-on					
Current consumption					
$V_{control} = -10$ V	I_9	110	135	160	mA
$V_{control} = 0$ V	I_9	50	75	100	mA
Reference voltage					
$I_1 < 0.1$ mA	V_1	4.0	4.2	4.5	V
$I_1 = 5$ mA	V_1	4.0	4.2	4.4	V
Temperature coefficient of reference voltage	TC_1		10^{-3}		1/K
Control voltage $V_{control} = 0$ V	V_3	2.3	2.6	2.9	V
Collector-current simulation voltage					
$V_{control} = 0$ V	V_4*)	1.8	2.2	2.5	V
$V_{control} = 0$ V/−10 V	ΔV_4*)	0.3	0.4	0.5	V
Blocking voltage	V_5	6.0	7.0	8.0	V
Output voltages					
$V_{control} = 0$ V	V_{q7}*)	2.7	3.3	4.0	V
$V_{control} = 0$ V	V_{q8}*)	2.7	3.4	4.0	V
$V_{control} = 0$ V/−10 V	ΔV_{q8}*)	1.6	2.0	2.4	V
Feedback voltage	V_2		0.2		V

*) only dc part

Characteristics

$T_{amb} = 25\ °C$

Safety operation

($V_9 = 10$ V; $V_{control} = -10$ V; $V_{clock} = \pm 0.5$ V; $f = 20$ kHz; duty cycle 1 : 2)

		min	typ	max	
Current consumption ($V_5 < 1.9$ V)	I_9	14	22	28	mA
Switch-off voltage ($V_5 < 1.9$ V)	$V_{q\,7}$	1.3	1.5	1.8	V
Blocking input	V_4	1.8	2.1	2.5	V
Blocking voltage ($V_{control} = 0$ V)	V_5	$\frac{V_1}{2} - 0.1$	$\frac{V_1}{2}$		V
Supply voltage for V_8 blocked ($V_{control} = 0$ V)	V_9	6.7	7.4	7.8	V
(with further decrease of V_9)	ΔV_9	0.3	0.6	1	V

Characteristics

$T_{amb} = 25\ °C$ acc. to test circuit 2

Turn-on time (secondary voltage)	t_{on}		350	450	ms
Voltage change with S3 = closed ($\Delta N_3 = 20$ W)	$\Delta V_{2\,s}$		100	500	mV
Voltage change with S2 = closed ($\Delta N_2 = 15$ W)	$\Delta V_{2\,s}$		500	1000	mV
Standby operation with S1 = open (secondary useful load = 3 W)	$\Delta V_{2\,s}$		20	30	V
	f	70	75		kHz
	$N_{primary}$		10	12	VA

The cooling area should be optimized in consideration of the limit values (T_{case}; T_j; $R_{th\,JC}$; $R_{th\,JA}$).

Circuit description

During start-up, normal, overload, and disturbed operations the TDA 4601/D regulates, controls and protects the switching transistor installed in the flyback converter power supplies. If an error occurs, the driving of the switching transistor is blocked and the voltage on the secondary side is prevented from increasing.

I) Start-up operation

The start-up operation is divided into three consecutive phases:

1. An internal reference voltage is built up which supplies the voltage regulator and effects the charging of the coupling electrolytic capacitor and the switching transistor. During these procedures an I_9 current less than 3.2 mA will be maintained, if the supply voltage V_9 does not exceed $\approx$ 12 V.
2. At $V_9 \approx 12$ V an internal reference voltage $V_1 = 4$ V is suddenly released to provide all IC components with the exception of the control logic with a thermally stable and overload-resistant current.
3. In concurrence with the release of the reference voltage the control logic is activated by an additional stabilization circuit, and the IC is now ready for operation.

Above sequential start-up phases ensure the charging of the switching transistor by the coupling electrolytic capacitor and subsequent precision switching.

II) Normal operation

Zero passages of the feedback coil are registered at pin 2 and forwarded to the control logic.

At pin 3 (input control, overload, and standby recognition) the rectified amplitude variations of the feedback coil are applied. The regulating (control) amplifier operates with an input voltage of about 2 V and a current of about 1.4 mA. According to the internal reference voltage, the operating region of the regulating amplifier will be defined by the collector current simulation pin 4 and the overload recognition. The simulation of the collector current is generated by an external *RC* network at pin 4 and an internally set voltage level. By increasing the capacitance (10 nF), the collector current of the switching transistor is increased as well and establishes the desired control range. The control range extends between a 2 V clamped dc voltage and an ac voltage rising as a sawtooth wave, which may vary up to a maximum amplitude of 4 V (reference voltage).

By reducing the secondary load to 20 W, the switching frequency increases to about 50 kHz at an almost constant pulse duty factor (on-time to period approx. 1/3). During additional secondary load reduction to about 1 W, the switching frequency will change to approx. 70 kHz, while the pulse duty factor falls to approx. 1/11. At the same time, the collector peak current falls below 1 A.

The output level of the regulating (control) amplifier, the overload recognition, and the collector current simulation are compared in the trigger and the control logic is instructed accordingly. Pin 5 will provide additional blocking alternatives, i.e. the output at pin 8 is blocked at a voltage of equal to or less than $V_{ref}/2 - 0.1$ V at pin 5.

Based on the start-up circuit, the zero crossing identification, and the trigger-activated release, the control logic flipflops are set which control both the base current amplification and shut-down. The base current amplifier forwards the sawtooth voltage V_4 to pin 8. Also, a current feedback with an external resistance of $R \approx 0.68\ \Omega$ is inserted between pin 8 and pin 7. The resistance value determines the maximum amplitude of the base current for the switching transistor.

III) Safety features

The base current shut-down, released by the control logic, clamps the output of pin 7 at 1.6 V and thus blocks the driving of the switching transistor. This preventive method will go into effect, if the voltage at pin 9 falls below typ. 6.7 V or if voltages of equal to or less than $V_{ref}/2 - 0.1$ V are present at pin 5. In case of short-circuited secondary windings in the SMPS, the fault condition will be continuously monitored by the IC.

With the load completely removed from the secondary winding in the SMPS, the IC is set at a small pulse duty factor. The total power consumption of the SMPS is kept below $n = 6$ to 10 W during both operating conditions. After the output has been blocked at a supply voltage V_9 of less than or equal to typ. 6.7 V, an additional voltage reduction of $\Delta V_9 = 0.6$ V will switch of the reference voltage (4 V).

Protective operation for faults with pin 5

For protection against disturbances such as primary undervoltages and/or secondary overvoltages (e.g. as a result of alterations in the parameters of components of the SMPS), it is possible to implement applications of the following kind:

● **Protective operation with periodic sampling**

In the event of the fault condition, falling below the protective threshold V_5 of typically $V_{1/2}$ causes the output pulses on pin 8 to be inhibited and pin 5 to be clamped internally to ground across typically 300 Ω. The current consumption of the IC reduces ($I_9 \geq 14$ mA for $V_9 = 10$ V).

With a suitably **high-impedance** starting resistor*) the supply voltage V_9 then falls below the minimal turn-off threshold (5.7 V) for the reference voltage V_1. As a result V_1 is turned off and the blocking of pin 5 is cancelled.

Because of the renewed reduction in the current consumption of the IC ($I_9 \leq 3.2$ mA for $V_9 \leq 10$ V) the supply voltage can again climb to the turn-on threshold $V_9 \geq 12.3$ V. The protective threshold on pin 5 is released and the switched-mode power supply attempts to turn on.

If the same fault is still present or another ($V_5 \leq V_{1/2} - 0.1$ V), the turn-on will be interrupted by the above, periodic protective operation, i.e. pin 8 is disabled, pin 5 is blocked, V_9 falls off, etc.

*) 10 kΩ/3 W in application circuit 1

● **Protective operation with capture circuit**

The starting resistor on pin 9 is chosen sufficiently low-impedance so that in the event of a fault V_9 does not fall below the maximum turn-off threshold (7.5 V) for V_1. The blocking of pin 5 is preserved because V_1 will not have been turned off. A one-time fault is thus captured and turning the SMPS on again is not possible, for example, until the supply voltage has been manually turned off (power switch).

In the designing of the starting resistor it should be considered that in protective operation the current consumption reduces to $I_9 \leq 28$ mA for $V_9 = 10$ V.

IV) Turn-on in wide-range power supply (90 to 270 Vac)
(application circuit 2)

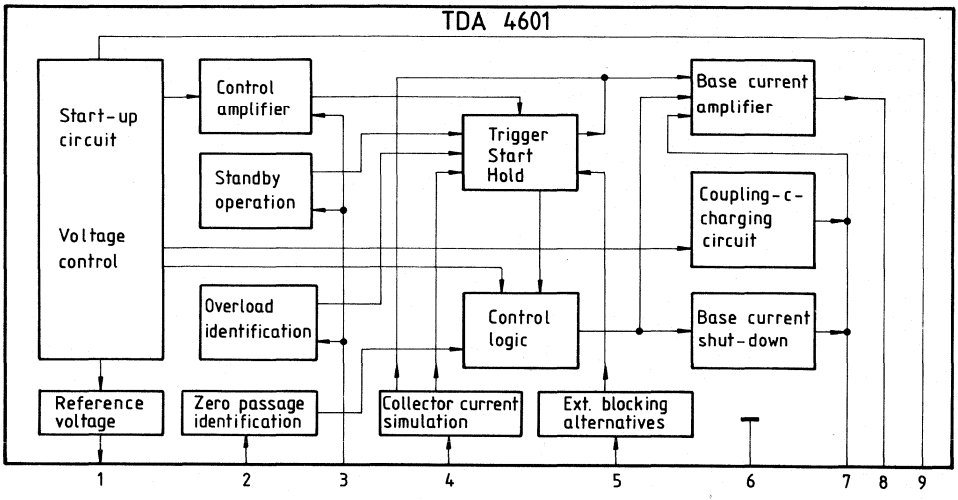
Free-running flyback converters used as wide-range power supplies call for a power supply to the TDA 4601 that is independent of the rectified line voltage, thus the sense of the winding 11/13 corresponds to the secondary side of the flyback-converter transformer. Turning on is hampered by the fact that the TDA 4601 must be supplied by the start-up circuit until the entire load secondary side is charged. This leads to long turn-on times, especially with a low line voltage.

If the special start-up circuit is used (marked by dashed lines) this time can be shortened. The unregulated phase of the feedback control winding 15/9 is used as a turn-on aid. The transistor T1 blocks after turn-on, when the winding 11/13 has taken over the power supply to the TDA 4601, thus eliminating any effects on the control circuit during operation.

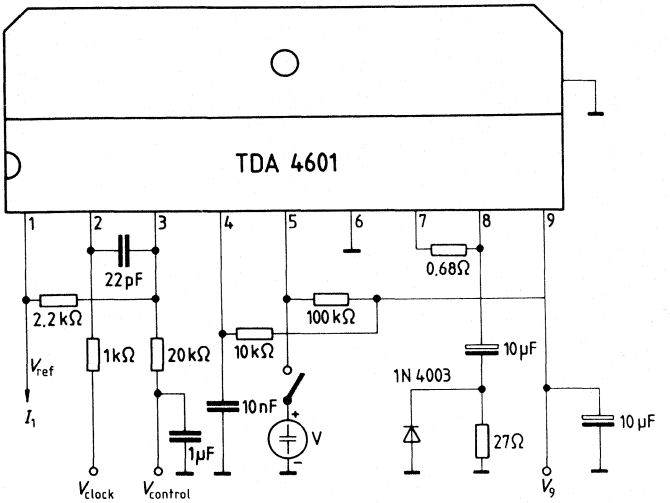
Pin configuration

Pin No.	Function
1	V_{ref} output
2	Zero-passage identification
3	Input regulating amplifier, overload amplifier
4	Collector-current simulation
5	Possible connection for additional protective circuit
6	Ground (rigidly connected to substrate mounting plate)
7	DC voltage output for charging the coupling capacitor
8	Pulse output, driving the switching transistor
9	Power supply

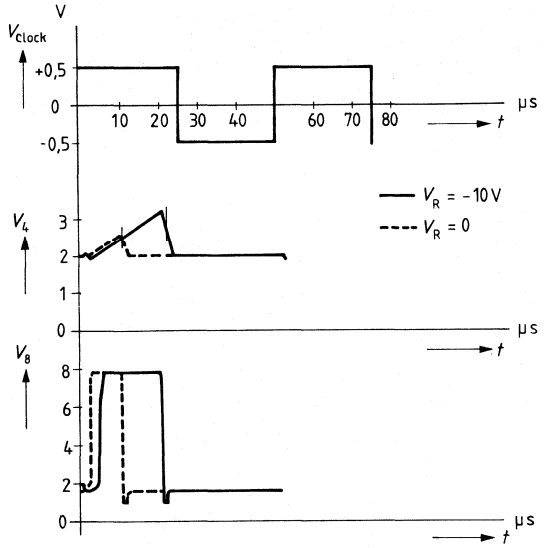
Block diagram



Test and measurement circuit 1

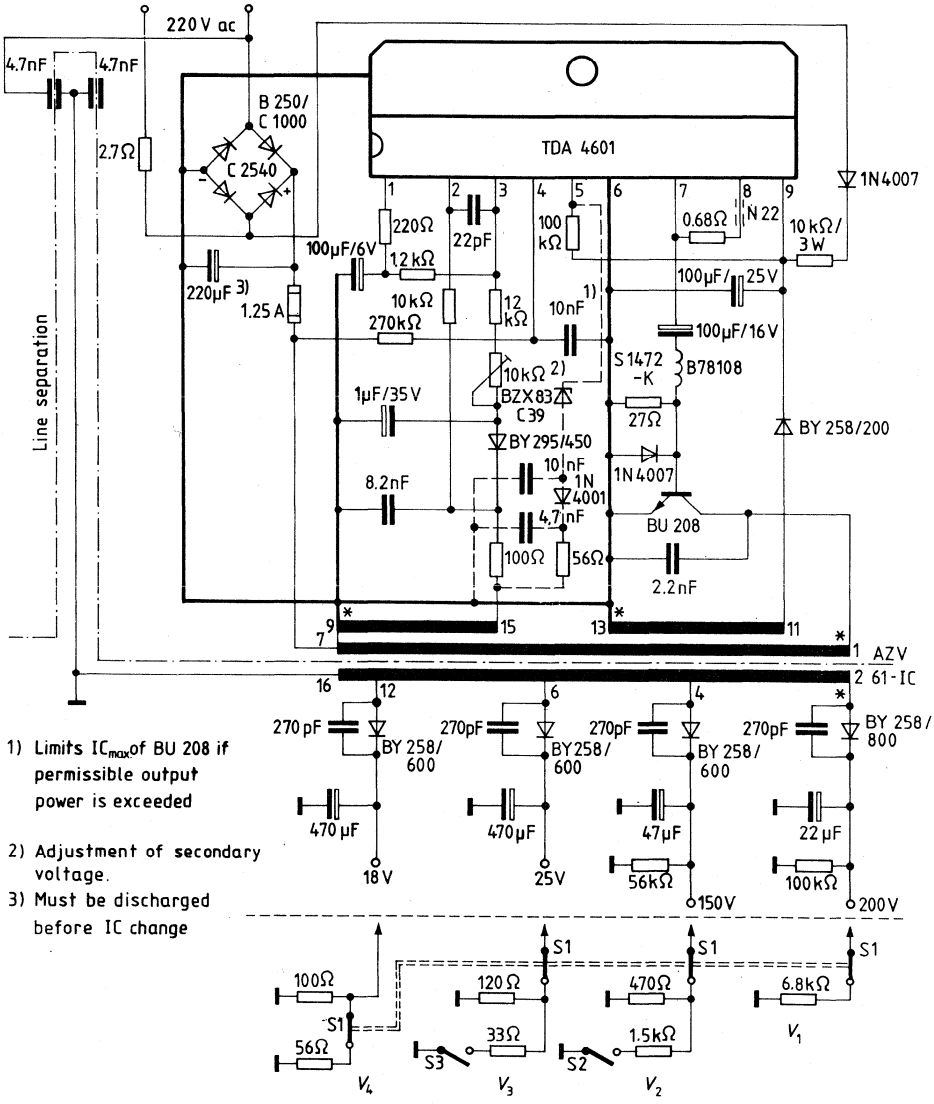


Test diagram: overload operation



Test and measurement circuit 2

Application circuit 1



1) Limits IC_{max} of BU 208 if permissible output power is exceeded

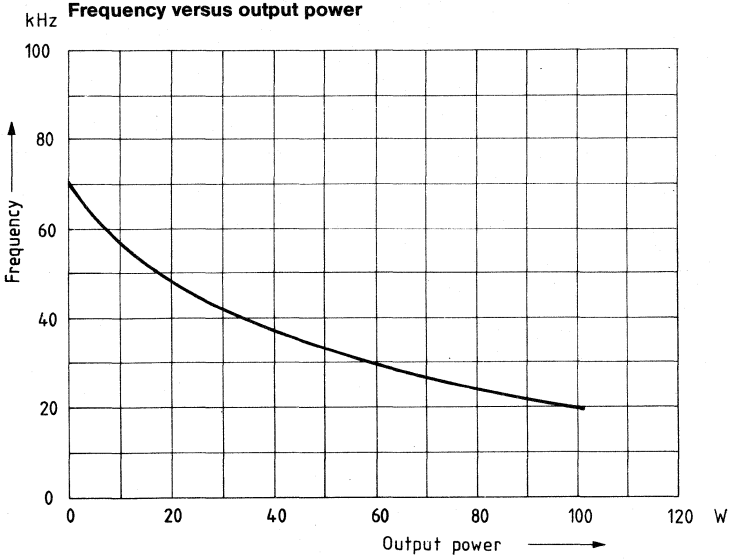
2) Adjustment of secondary voltage.

3) Must be discharged before IC change

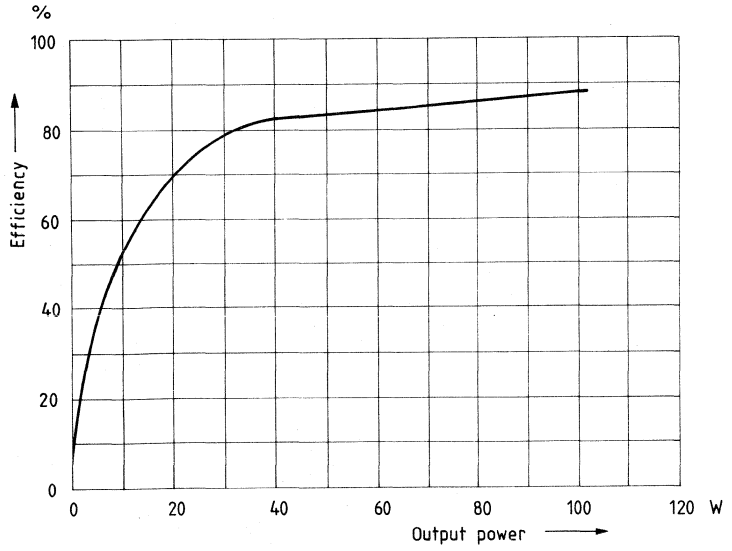
— — — Protective circuit to prevent increase of secondary voltage when fault occurs

Additions to test circuit 2

Frequency versus output power

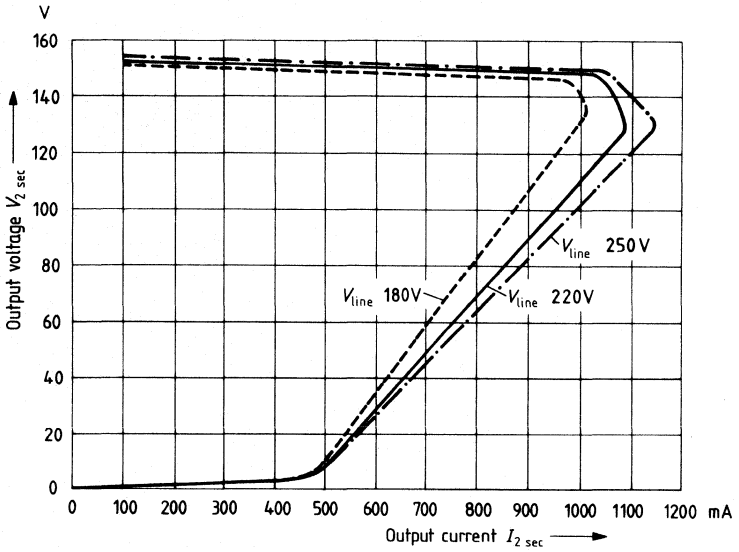


Efficiency versus output power

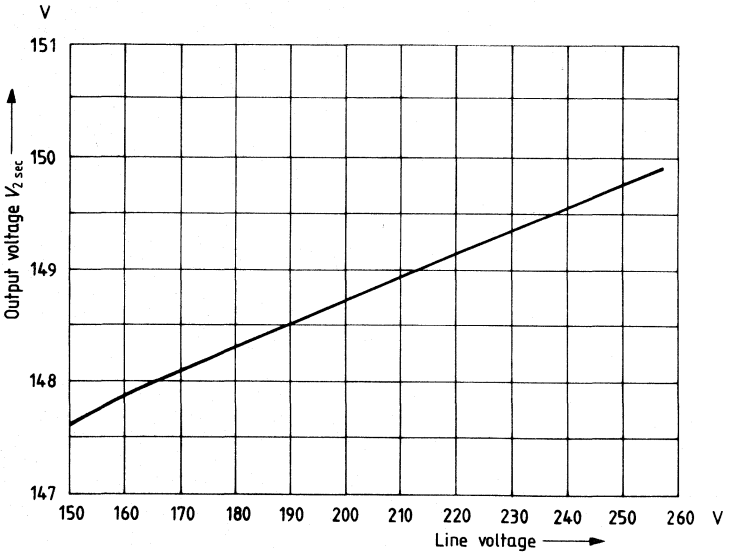


Additions to test circuit 2

Load characteristic $V_{2\,sec}$ versus output current $I_{2\,sec}$

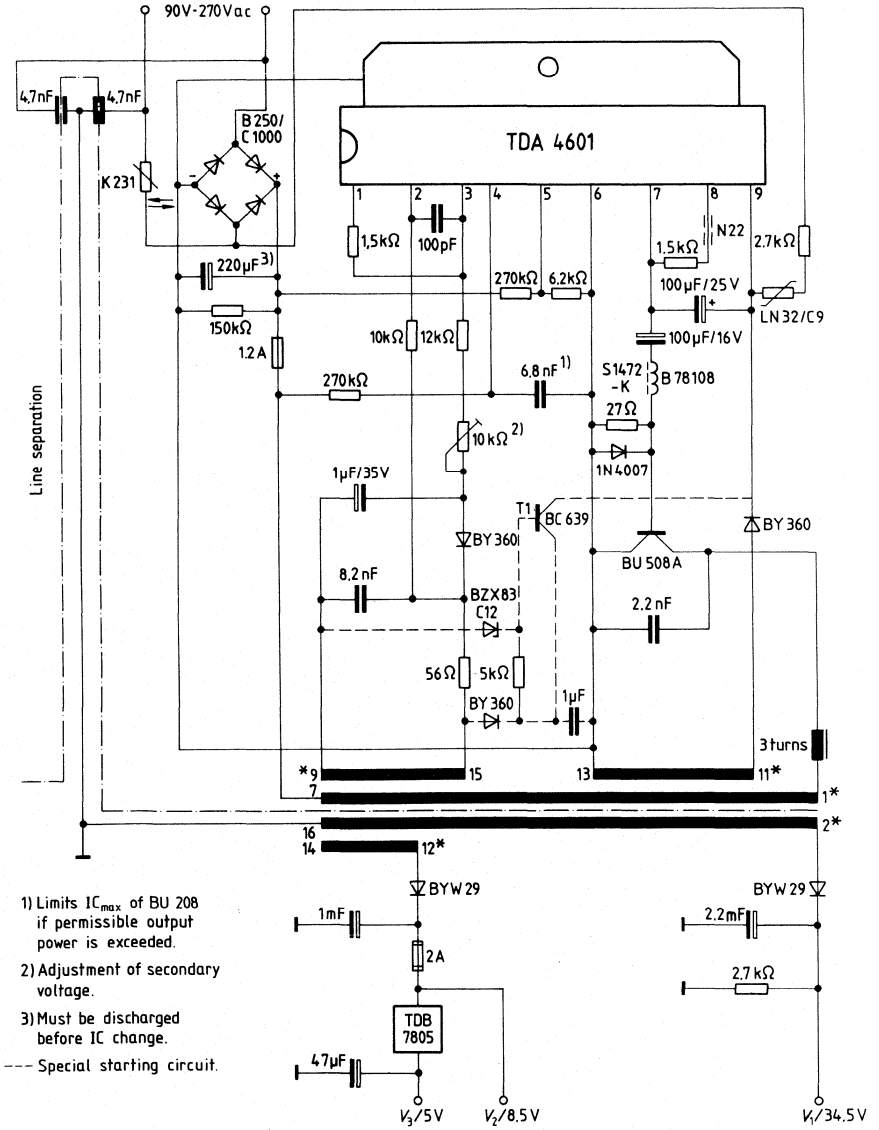


Output voltage $V_{2\,sec}$ versus line-voltage alterations



Application circuit 2

Wide range 90 Vac to 270 Vac



1) Limits IC_{max} of BU 208 if permissible output power is exceeded.

2) Adjustment of secondary voltage.

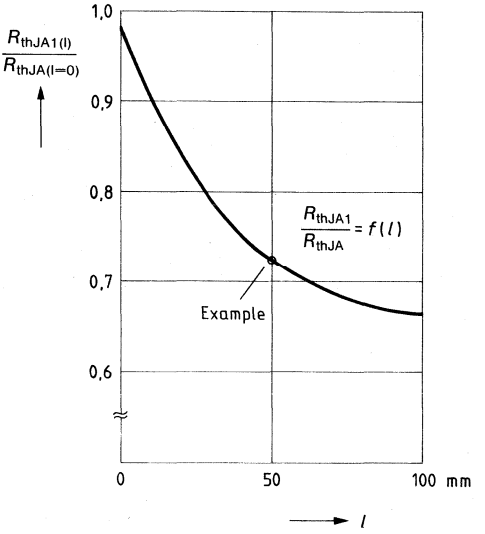
3) Must be discharged before IC change.

--- Special starting circuit.

Thermal resistance (only applies to TDA 4601 D)

Standardized, ambience-related thermal resistance $R_{th\ JA\,1}$ versus lateral length l of a square copper-clad cooling area (35 µm copper lamination).

$R_{th\ JA}$ ($l = 0$) = 60 K/W
$T_{amb} \leq 70$ °C
$P_V = 1$ W
PCB in vertical position
circuit in vertical position
static air



Control ICs for Single-Ended and Push-Pull Switched-Mode Power Supplies (SMPS)

The TDA 47xx family of control ICs for SMPS consists of four basic types that, in line with the particular application, will enable optimal adaptation to the SMPS concept that is called for. These devices include all the important basic functions that are expected of a modern SMPS, such as feed-forward control, soft start, dynamic current limitation, error comparators, reference-voltage source, undervoltage shut-down and push-pull open-collector outputs.

TDA 4714A; B is the most economic version. TDA 4700; A is the version with the largest selection of functions. The devices are available with the following temperature ranges:

Type	Package	Ambient temperature range
TDA 4700	DIC 24	−25 to 85 °C
TDA 4700A	DIP 24	0 to 70 °C
TDA 4718	DIC 18	−25 to 85 °C
TDA 4718A	DIP 18	0 to 70 °C
TDA 4716A	DIP 16	0 to 70 °C
TDA 4716B	DIP 16	−25 to 85 °C
TDA 4714A	DIP 14	0 to 70 °C
TDA 4714B	DIP 14	−25 to 85 °C

Control IC for Single-Ended and Push-Pull Switched-Mode Power Supplies

TDA 4700
TDA 4700 A

Bipolar IC

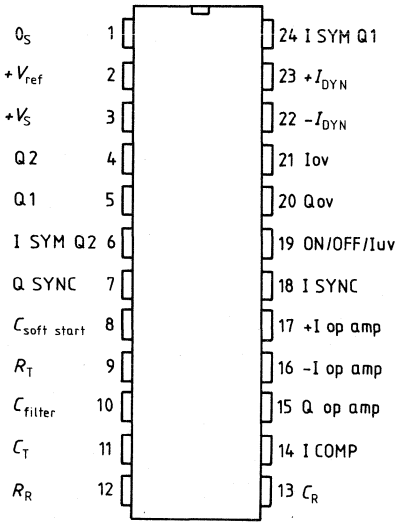
Type	Ordering code	Package	Fig. No.
TDA 4700	Q67000-Y595	DIC 24	15
TDA 4700 A	Q67000-Y594	DIP 24	14

This versatile SMPS control IC comprises digital and analog functions which are required to design high-quality flyback, single-ended and push-pull converters in normal, half-bridge and full-bridge configurations. The component can also be used in single-ended voltage multipliers and speed-controlled motors. Malfunctions in electrical operation are recognized by the integrated operational amplifiers and activate protective functions.

In addition to the noticeable reduction in components, our SMPS ICs offer a number of advantages:

- Feed-forward control (line hum suppression)
- Symmetry inputs for push-pull converter
- Dynamic output current limitation
- Overvoltage protection
- Undervoltage protection
- Soft start
- Double pulse suppression

Pin configuration,
top view



Pin designation

Pin No.	Function
1	0_S
2	Reference voltage V_{ref}
3	Supply voltage V_S
4	Output Q 2
5	Output Q 1
6	Symmetry Q 2
7	Sync. output
8	Soft start $C_{soft\ start}$
9	VCO R_T
10	Capacitance C_{filter}
11	VCO C_T
12	Ramp generator R_R
13	Ramp generator C_R
14	Comparator input
15	Operational amplifier output
16	Operational amplifier input (−)
17	Operational amplifier input (+)
18	Sync. input
19	ON/OFF, undervoltage
20	Overvoltage output
21	Overvoltage input
22	Dynamic current limitation (−)
23	Dynamic current limitation (+)
24	Symmetry Q 1

Circuit description

Voltage controlled oscillator (VCO)

The VCO generates a sawtooth voltage. The duration of the falling edge is determined by the value of C_T. The duration of the rising edge of the waveform and, therefore, approximately the frequency, is determined by the value of R_T. By varying the voltage at C_{filter}, the oscillator frequency can be changed by its rated value. During the fall time, the VCO provides a trigger signal for the ramp generator, as well as an L signal for a number of IC parts to be controlled.

Ramp generator

The ramp generator is triggered by the VCO and oscillates at the same frequency. The duration of the falling edge of the ramp generator waveform is to be shorter than the fall time of the VCO. To control the pulse width at the output, the voltage of the rising edge of the ramp generator signal is compared with a dc voltage at comparator K2. The slope of the rising edge of the ramp generator signal is controlled by the current through R_R. This offers the possibility of an additional, superimposed control of the output duty cycle. **This additional control capability, called »feed-forward control«, is utilized to compensate for known interference such as ripple on the input voltage.**

Phase comparator

If the component is operated without external synchronization, the sync input must be connected to the sync output for the phase comparator to set the rated voltage at C_{filter}. The VCO then oscillates with rated frequency. In the case of external synchronization, other components can be synchronized with the sync output. **The component can be frequency-synchronized, but not phase-synchronized, with the sync input.** The duty cycle of the square-wave voltage at the sync input is arbitrary. The best stability as to small phase and frequency interference deviation is achieved with a duty cycle as offered by the sync output.

Push-pull flipflop

The push-pull flipflop is switched by the falling edge of the VCO. This ensures that only one output of the two push-pull outputs is enabled at a time.

Comparator K2

The two plus inputs of the comparator are switched such that the lower plus level is always compared with the level of the minus input. As soon as the voltage of the rising sawtooth edge exceeds the lower of the two plus levels, both outputs are disabled via the pulse turn-off flipflop. The period during which the respective, active output is low can be infinitely varied. As the frequency remains constant, this process corresponds to a change in duty cycle.

Operational amplifier K1

The K1 op amp is a high-quality amplifier. Fluctuations in the output voltage of the power supply are amplified by K1 and applied to the free + input of comparator K2. Variations in output voltage are, in this way, converted to a corresponding change in output duty cycle. K1 has a common-mode input voltage range between 0 V and +5 V.

Pulse turn-off flipflop

The pulse turn-off flipflop enables the outputs at the start of each half cycle. If an error signal from comparator K7 or a turn-off signal from K2 is present, the outputs will immediately be switched off.

Comparator K3

Comparator K3 limits the voltage at capacitance $C_{\text{soft start}}$ (and also at K2) to a maximum of +5 V. The voltage at the ramp generator output may, however, rise to 5.5 V. With a corresponding slope of the rising ramp generator edge, the duty cycle can be limited to a desired maximum value.

Comparator K4

The comparator has its switching threshold at 1.5 V and sets the error flipflop with its output if the voltage at capacitance $C_{\text{soft start}}$ is below 1.5 V. However, the error flipflop accepts the set signal only if no reset pulse (error) is applied. In this way the outputs cannot be turned on again as long as an error signal is present.

Soft start

The lower one of the two voltages at the plus inputs of K2 is a measure for the duty cycle at the output. At the instant of turning on the component, the voltage at capacitor $C_{\text{soft start}}$ equals 0 V. As long as no error is present, this capacitor is charged with a current of 6 μA to the maximum value of 5 V. In case of an error, $C_{\text{soft start}}$ is discharged with a current of 2 μA. A set signal is pending at the error flipflop below a charge of 1.5 V and the outputs are enabled if no reset signal is pending simultaneously. As the minimum ramp generator voltage, however, is 1.8 V, the duty cycle at the outputs is actually increased slowly and continuously not before the voltage at $C_{\text{soft start}}$ exceeds 1.8 V.

Error flipflop

Error signals which are led to input $\overline{R}$ of the error flipflop cause an immediate disabling of the outputs, and after the error has been eliminated, the component to switch on again using the soft start.

Comparator K5, K6, K8, V_{ref} overcurrent load

These are error detectors which cause immediate disabling of the outputs via the error flipflop when an error occurs. After elimination of the error, the component switches on again using the soft start. The output of K5 can be fed back to the input. This causes the IC output stage to remain disabled even after elimination of the overvoltage. However, it requires high-ohmic overvoltage coupling.

Comparator K7

K7 serves to recognize overcurrents. This is the reason why both inputs of the op amp have been brought out. Turning on is resumed after error recovery at the beginning of the next half period but without using the soft start.

The K7 common-mode range covers 0 V to +4 V. The delay time between occurrence of an error and disabling of the outputs is only 250 ns.

Symmetry

In push-pull converters, a saturation of the transformer core must be prevented. The degree of saturation of the transformer can be determined with an external circuit, thus the active periods of the outputs can be decreased unsymmetrically at the symmetry inputs.

Outputs

Both outputs are transistors with open collectors and operate in a push-pull arrangement. They are active low. The time in which only one of the two outputs is conductive can be varied infinitely. The length of the falling edge at VCO is equal to the minimum time during which both outputs are disabled simultaneously. The minimum L voltage is 0.7 V.

Reference voltage

The reference voltage source is a highly constant source with regard to its temperature behavoir. It can be utilized in the external wiring of the op amp, the error comparators, the ramp generator, or other external components.

Maximum ratings

		Notes	Lower limit B	Upper limit A	
Supply voltage	V_S		−0.3	33	V
Voltage at Q1, Q2	V_Q	Q1, Q2 high	−0.3	33	V
Current at Q1, Q2	I_Q	Q1, Q2 low		70	mA
Symmetry 1, 2	V_{SYM}		−0.3	33	V
Sync output	$V_{SYNC\,Q}$	SYNC Q high	−0.3	7	V
	$I_{SYNC\,Q}$	SYNC Q low	0	10	mA
Sync input	$V_{SYNC\,I}$		−0.3	33	V
Input C_{filter}	$V_{I\,Cf}$		−0.3	7	V
Input R_T	$V_{I\,RT}$		−0.3	7	V
Input C_T	$V_{I\,CT}$		−0.3	7	V
Input R_R	$V_{I\,RR}$		−0.3	7	V
Input C_R	$I_{I\,CR}$		−10	10	mA
Input comparator					
K 2, K 5, K 6, K 7	$V_{I\,K}$		−0.3	33	V
Output K 5	$V_{Q\,K5}$		−0.3	33	V
Input op amp	$V_{I\,op\,amp}$		−0.3	33	V
Output op amp	$V_{Q\,op\,amp}$		−0.3	V_S−1	V
				max. 7	V
Reference voltage	V_{ref}		−0.3	V_{ref}	V
Input $C_{soft\,start}$	$V_{I\,soft\,start}$		−0.3	7	V
Junction temperature	T_j			125	°C
Storage temperature	T_{stg}		−55	125	°C
Thermal resistance (system-air)					
TDA 4700	$R_{th\,SA}$			65	K/W
TDA 4700 A	$R_{th\,SA}$			65	K/W

Operating range

Supply voltage	V_S		10.5	30	V
Ambient temperature					
TDA 4700	T_{amb}		−25	85	°C
TDA 4700 A	T_{amb}		0	70	°C
VCO frequency	f		40	250000	Hz
Ramp generator frequency	f_{RG}		40	250000	Hz

Characteristics

$V_S = 11$ V to 30 V;
$T_{amb} = -25$ °C to +85 °C

		Test conditions	Lower limit B	typ	Upper limit A	
Supply current	I_S	$C_T = 1$ nF, $f_{VCO} = 100$ kHz	8		20	mA
Reference						
Reference voltage	V_{ref}	0mA<I_{ref}<5mA	2.35	2.5	2.65	V
Reference voltage change	ΔV_{ref}	14 V ± 20%		8		mV
Reference voltage change	ΔV_{ref}	25 V ± 20%		15		mV
Reference voltage change	ΔV_{ref}	0mA<I_{ref}<5mA			15[1]	mV
Temperature coefficient	TC			0.25	0.4	mV/K
Response threshold of I_{ref} overcurrent	I_{ref}			10		mA
Oscillator (VCO)						
Frequency range	f_{VCO}		40		100000	Hz
Frequency change	$\Delta f/f_{VCO}$	14 V ± 20%		0.5		%
Frequency change	$\Delta f/f_{VCO}$	25 V ± 20%	−1		1	%
Tolerance	$\Delta f/f_{VCO}$	$\Delta R_T = 0, \Delta C_T = 0$	−7		7	%
Fall time sawtooth	t	$C_T =$ 1 nF		1		µs
	t	$C_T = 10$ nF		10		µs
RC combination	C_T		0.82		47	nF
VCO	R_T		5		700	kΩ
Ramp generator						
Frequency range	f		40		100000	Hz
Maximum voltage at C_R	V_H			5.5		V
Minimum voltage at C_R	V_L			1.8		V
Input current through R_R	I_{RR}		0		400	µA
Current transformation ratio	I_{RR}/I_{CR}			1/4		
Synchronization						
Sync output	V_{QH}	$I_{QH} = -200$ µA	4			V
	V_{QL}	$I_{QL} = 1.6$ mA			0.4	V
Sync input	V_{IH}		2			V
	V_{IL}				0.8	V
Input current	$-I_I$				5	µA
Comparator K2						
Input current	$-I_{IK2}$				2	µA
Turn-off delay[2]	$t_{d\,off}$				500	ns
Input voltage	V_{IK2}	for duty cycle				
		$\nu = 0$		1.8		V
		$\nu =$ max.		5		V
Common-mode input voltage range	V_{IC}		0		5.5	V

1) At $T_{amb} = 0$ °C to 70 °C, this value falls to max. 5 mV.
2) At the input: step function $\Delta V = -100$ mV ↛ $\Delta V = +100$ mV

Characteristics

$V_S = 11$ V to 30 V;
$T_{amb} = -25$ °C to +85 °C

		Test conditions	Lower limit B	typ	Upper limit A	
Soft start K3, K4						
Charging current for $C_{soft\ start}$	I_{ch}			6		µA
Discharging current for $C_{soft\ start}$	I_{dch}			2		µA
Upper limiting voltage	V_{lim}			5		V
Switching voltage K4	V_{K4}			1.5		V
Operational amplifier						
Open-loop voltage gain	G_{V0}		60	80		dB
Input offset voltage	V_{IO}		−10		10	mV
Temperature coefficient of V_{IO}	TC		−30		30	µV/K
Input current	$-I_I$				2	µA
Common-mode input voltage range	V_{IC}		0		5	V
Output current	I_Q		−3		1.5	mA
Rise time of output voltage	$\Delta V/\Delta t$			1		V/µs
Transition frequency	f_T			3		MHz
Phase at f_T	φ_T			120		degrees
Output voltage	$V_{QH/L}$	$-3\,mA < I < 1.5\,mA$	1.5		5.5	V
Symmetry						
Input voltage	V_{IH}		2.0			V
	V_{IL}				0.8	V
Input current	$-I_I$				2	µA
Output stages Q1, Q2						
Output voltage	V_{QH}				30	V
	V_{QL}	$I_Q = 20$ mA			1.1	V
Output leakage current	I_Q	$V_{QH} = 30$ V			2	µA
ON, OFF, undervoltage K6						
Switching voltage	V		V_{ref}-30mV		V_{ref}+30mV	V
Input current	$-I_I$				2	µA
Turn-off delay time[1]	$t_{d\ off}$			250		ns
Error detection time[1]	t			50		ns

1) At the input: step function $V_{ref} = -100$ mV ↛ $V_{ref} = +100$ mV

Characteristics

$V_S = 11$ V to 30 V; $T_{amb} = -25$ °C to +85 °C

		Test conditions	Lower limit B	typ	Upper limit A	
Dynamic current limitation K 7						
Common-mode input voltage range	V_{IC}		0		4	V
Input offset voltage	V_{IO}		−10		10	mV
Input current	$-I_I$				2	µA
Turn-off delay time[1]	$t_{d\,off}$			250		ns
Error detection time[1]	t			50		ns
Overvoltage K 5						
Switching voltage	V		V_{ref}−30 mV		V_{ref}+30 mV	V
Input current	$-I_I$				2	µA
Output current	$-I_Q$	$V_{QHmin} = 5$ V	0		200	µA
Turn-off delay time[2]	$t_{d\,off}$			250		ns
Error detection time[2]	t			50		ns
Supply undervoltage						
Turn-on threshold for V_S rising	V_S	0°C<T_{amb}<70°C	8.8		11	V
					10.5	V
Turn-off threshold for V_S falling	V_S	0°C<T_{amb}<70°C	8.5		10.5	V
					10	V
Input C_{filter}						
Rated voltage for rated frequency	V_R			4		V
Frequency approx. proportional to voltage within the range	V_R		3		5	V
Voltage at open sync input	$V_{C\,filter}$			1.6		V

1) At the input: step function $\Delta V = -100$ mV ⌟→ $\Delta V = +100$ mV
2) At the input: step function $V_{ref} = -100$ mV⌟→ $V_{ref} = +100$ mV

Dimensioning notes for RC network

1. Determination of the minimum time during which both outputs must be disabled
   → selection of C_T; selection of $C_R \leq C_T$

2. Determination of the VCO frequency = 2 x output frequency
   → selection of R_T.

3. Determination of the rated slope of the rising ramp generator voltage, which the maximum possible turn-on period per half wave depends on
   → selection of R_R.

4. Duration of the soft start process
   → selection of $C_{soft\ start}$.

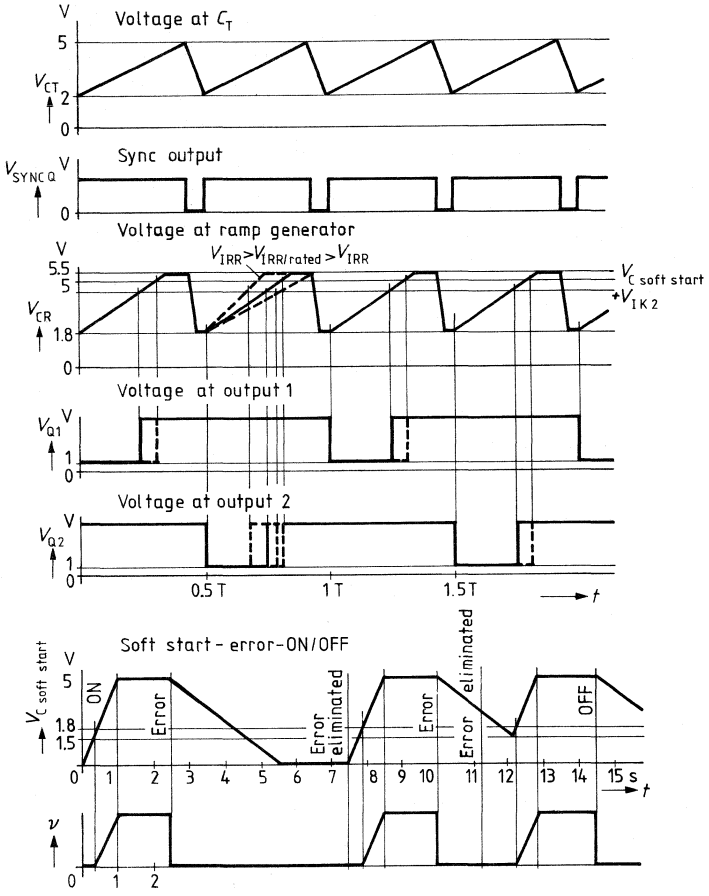
5. In the case of a free-running VCO: connect sync output with sync input.

6. Wiring of the op amp according to the dynamic requirements and connection of its output with the free input of K2.

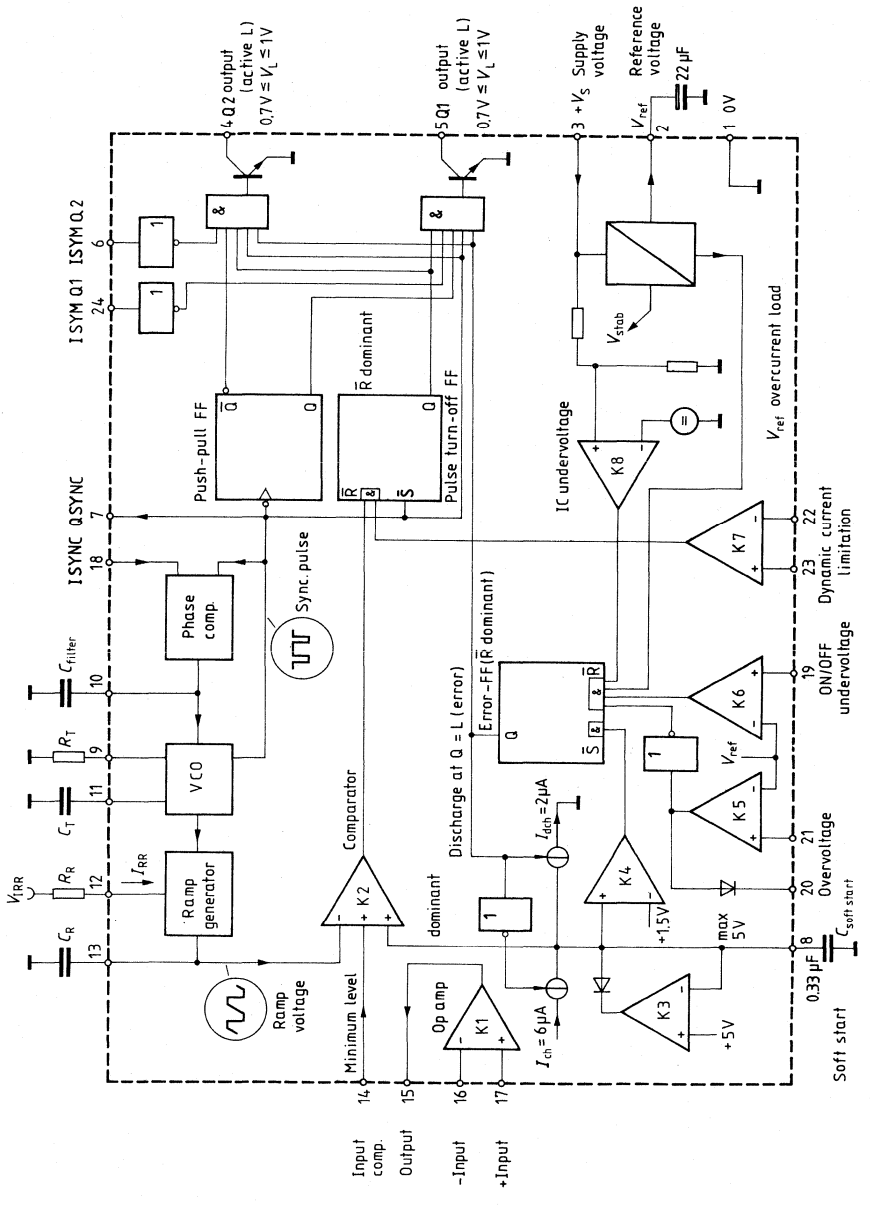
7. Capacitance C_{filter} is not required in the free-running operation (sync input connected with sync output).
   In the case of external synchronization, that value depends on the selected operating frequency and the required maximum phase interference deviation.

Rated VCO frequency:	100 kHz	50 Hz
C_{filter} favorable:	10 nF	1 µF

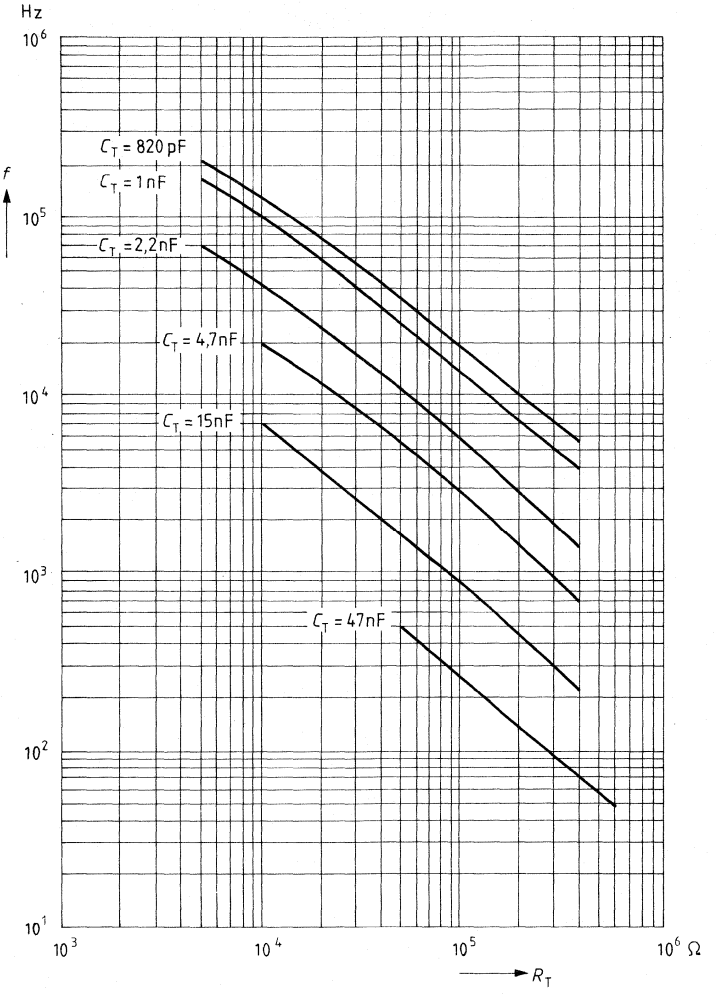
Pulse diagram



Block diagram

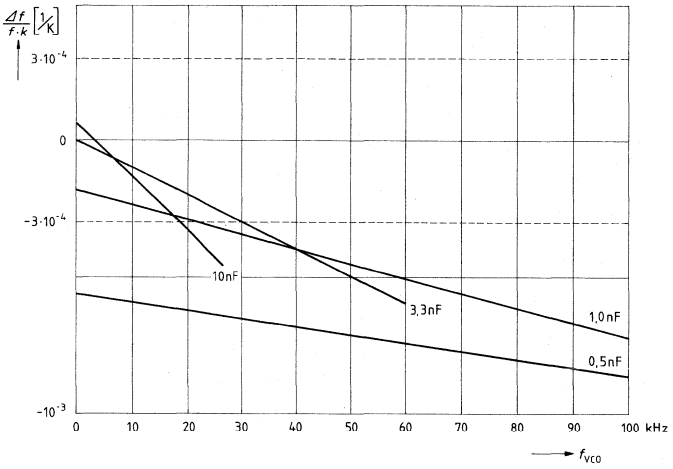


VCO frequency versus R_T and C_T.

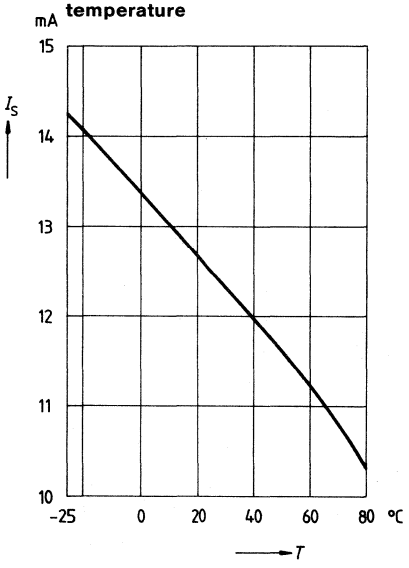


VCO temperature response
$V_S = 12$ V; ν = max.

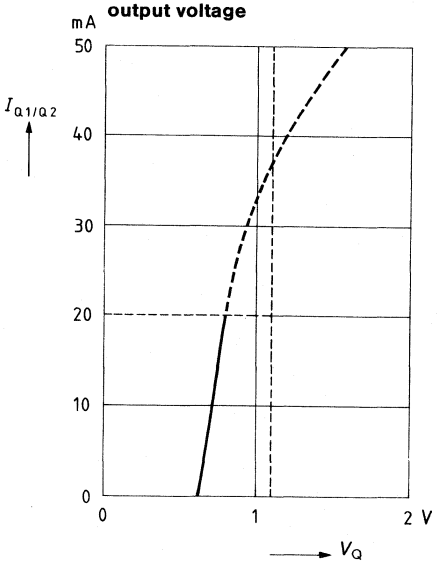
$\frac{\Delta f_{VCO}}{f_K \cdot K}\left[\frac{1}{K}\right]$ with C_T as parameter



Current consumption versus temperature



Output current versus output voltage



Control IC for Single-Ended and Push-Pull Switched-Mode Power Supplies

TDA 4718
TDA 4718 A

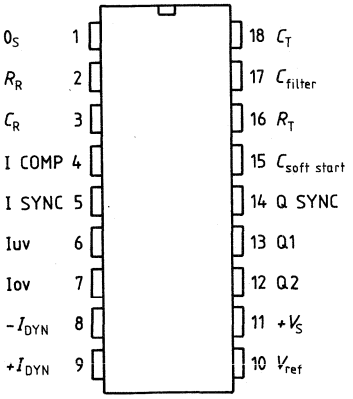
Bipolar IC

Type	Ordering code	Package	Fig. No.
TDA 4718	Q67000-Y638	DIC 18	10
TDA 4718 A	Q67000-Y639	DIP 18	11

This 18-pin SMPS control IC comprises digital and analog functions which are required to design high-quality flyback, single-ended, and push-pull converters in normal and half-bridge configurations. In addition to the control functions, the circuit contains operational amplifiers which detect malfunctions during electrical operation and suitable protective measures. A PLL circuit for synchronization is one of the special advantages offered by this IC in addition to the following features:

- Feed-forward control (line hum suppression)
- Push-pull outputs
- Dynamic current limitation
- Overvoltage protection
- Undervoltage protection
- Soft start
- Double pulse suppression

Pin configuration
top view



Pin designation

Pin No.	Function
1	0_S
2	Ramp generator R_R
3	Ramp generator C_R
4	+ input comparator K 2
5	Sync input
6	Input undervoltage, ON/OFF
7	Input overvoltage
8	Input dynamic current limitation (−)
9	Input dynamic current limitation (+)
10	Reference voltage V_{ref}
11	Supply voltage V_S
12	Output Q 2
13	Output Q 1
14	Sync output
15	Soft start
16	VCO R_T
17	Capacitance C_{filter}
18	VCO C_T

Circuit description

Voltage controlled oscillator (VCO)

The VCO generates a sawtooth voltage. The duration of the falling edge is determined by the value of C_T. The duration of the rising edge of the waveform and, therefore, approximately the frequency, is determined by the value of R_T. By varying the voltage at C_{filter}, the oscillator frequency can be changed by its rated value. During the fall time, the VCO provides a trigger signal for the ramp generator, as well as an L signal for a number of IC parts to be controlled.

Ramp generator

The ramp generator is triggered by the VCO and oscillates at the same frequency. The duration of the falling edge of the ramp generator waveform is to be shorter than the fall time of the VCO. To control the pulse width at the output, the voltage of the rising edge of the ramp generator signal is compared with a dc voltage comparator K2. The slope of the rising edge of the ramp generator signal is controlled by the current through R_R. This offers the possibility of an additional, superimposed control of the output duty cycle. **This additional control capability, called »feed-forward control«, is utilized to compensate for known interference such as ripple on the input voltage.**

Phase comparator

If the component is operated without external synchronization, the sync input must be connected to the sync output for the phase comparator to set the rated voltage at C_{filter}. The VCO then oscillates with rated frequency. In the case of external synchronization, other components can be synchronized with the sync output. **The component can be frequency-synchronized, but not phase-synchronized, with the sync input.** The duty cycle of the square-wave voltage at the sync input is arbitrary. The best stability as to small phase and frequency interference is achieved with a duty cycle as offered by the sync output.

Push-pull flipflop

The push-pull flipflop is switched by the falling edge of the VCO. This ensures that only one output of the two push-pull outputs is enabled at a time.

Comparator K2

The two plus inputs of the comparator are switched such that the lower plus level is always compared with the level of the minus input. As soon as the voltage of the rising sawtooth edge exceeds the lower of the plus levels, both outputs are disabled via the pulse turn-off flipflop. The period during which the respective, active output is low can be infinitely varied. As the frequency remains constant, this process corresponds to a change in duty cycle.

Pulse turn-off flipflop

The pulse turn-off flipflop enables the outputs at the start of each half cycle. If an error signal from comparator K7 or a turn-off signal from K2 is present, the outputs will immediately be switched off.

Comparator K3

Comparator K3 limits the voltage at capacitance $C_{soft\ start}$ (and also at K2!) to a maximum of +5 V. The voltage at the ramp generator output may, however, rise to 5.5 V. With a corresponding slope of the rising ramp generator edge, the duty cycle can be limited to a desired maximum value.

Comparator K 4

The comparator has its switching threshold at 1.5 V and sets the error flipflop with its output if the voltage at capacitance $C_{soft\ start}$ is below 1.5 V. However, the error flipflop accepts the set signal only if no reset pulse (error) is applied. In this way the outputs cannot be turned on again as long as an error signal is present.

Soft start

The lower one of the two voltages at the plus inputs of K 2 is a measure for the duty cycle at the output. At the instant of turning on the component, the voltage at capacitor $C_{soft\ start}$ equals 0 V. As long as no error is present, this capacitor is charged with a current of 6 µA to the maximum value of 5 V. In case of an error, $C_{soft\ start}$ is discharged with a current of 2 µA. A set signal is pending at the error flipflop below a charge of 1.5 V and the outputs are enabled if no reset signal is pending simultaneously. As the minimum ramp generator voltage, however, is 1.8 V, the duty cycle at the outputs is actually increased slowly and continuously not before the voltage at $C_{soft\ start}$ exceeds 1.8 V.

Error flipflop

Error signals, which are led to input $\overline{R}$ of the error flipflop, cause an immediate disabling of the outputs, and after the error has been eliminated, the component to switch on again using the soft start.

Comparator K 5, K 6, K 8, V_{ref} overcurrent load

These are error detectors which cause immediate disabling of the outputs via the error flipflop when an error occurs. After elimination of the error, the component switches on again using the soft start.

Comparator K 7

K 7 serves to recognize overcurrents. This is the reason why both inputs of the op amp have been brought out. Turning on is resumed after error recovery at the beginning of the next half period but without using the soft start.

Outputs

Both outputs are transistors with open collectors and operate in a push-pull arrangement. They are actively low. The time in which only one of the two outputs is conductive, can be varied infinitely. The length of the falling edge at VCO is equal to the minimum time during which both outputs are disabled simultaneously.

Reference voltage

The reference voltage source is a highly constant source with regard to its temperature behavior. It can be utilized in the external wiring of the op amp, the error comparators, the ramp generator, or other external components.

Maximum ratings

		Notes	Lower limit B	Upper limit A	
Supply voltage	V_S		−0.3	33	V
Voltage at Q1, Q2	V_Q	Q1, Q2 high	−0.3	33	V
Current at Q1, Q2	I_Q	Q1, Q2 low		70	mA
Sync output	$V_{SYNC\ Q}$	SYNC Q high	−0.3	7	V
	$I_{SYNC\ Q}$	SYNC Q low	0	10	mA
Sync input	$V_{SYNC\ I}$		−0.3	33	V
Input C_{filter}	$V_{I\ Cf}$		−0.3	7	V
Input R_T	$V_{I\ RT}$		−0.3	7	V
Input C_T	$V_{I\ CT}$		−0.3	7	V
Input R_R	$V_{I\ RR}$		−0.3	7	V
Input C_R	$I_{I\ CR}$		−10	10	mA
Input comparator K2, K5, K6, K7	$V_{I\ K}$		−0.3	33	V
Output K5	$V_{Q\ K5}$		−0.3	33	V
Reference voltage	V_{ref}		−0.3	V_{ref}	V
Input $C_{soft\ start}$	$V_{I\ soft\ start}$		−0.3	7	V
Junction temperature	T_j			125	°C
Storage temperature	T_{stg}		−55	125	°C
Thermal resistance (system-air)					
TDA 4718	$R_{th\ SA}$			70	K/W
TDA 4718 A	$R_{th\ SA}$			60	K/W

Operating range

Supply voltage	V_S		10.5	30	V
Ambient temperature					
TDA 4718	T_{amb}		−25	85	°C
TDA 4718 A	T_{amb}		0	70	°C
Max. VCO frequency	f		40	250000	Hz
Ramp generator frequency	f_{RG}		40	250000	Hz

Characteristics $V_S = 11$ V to 30 V; $T_{amb} = -25$ °C to +85 °C		Test conditions	Lower limit B	typ	Upper limit A	
Supply current	I_S	$C_T = 1$ nF $f_{VCO} = 100$ kHz	8		20	mA
Reference						
Reference voltage	V_{ref}	$0\,mA < I_{ref} < 5$ mA	2.35	2.5	2.65	V
Reference voltage change	ΔV_{ref}	14 V ± 20%		8		mV
Reference voltage change	ΔV_{ref}	25 V ± 20%		15		mV
Reference voltage change	ΔV_{ref}	$0\,mA < I_{ref} < 5$ mA			15[1]	mV
Temperature coefficient	TC			0.25	0.4	mV/K
Response threshold of I_{ref} overcurrent	I_{ref}			10		mA
Oscillator (VCO)						
Frequency range	f_{VCO}		40		100 000	Hz
Frequency change	$\Delta f/f_{VCO}$	14 V ± 20%		0.5		%
Frequency change	$\Delta f/f_{VCO}$	25 V ± 20%	−1		1	%
Tolerance	$\Delta f/f_{VCO}$	$\Delta R_T = 0, \Delta C_T = 0$	−7		7	%
Fall time sawtooth	t	$C_T =$ 1 nF		1		µs
	t	$C_T = 10$ nF		10		µs
RC combination	C_T		0.82		47	nF
VCO	R_T		5		700	kΩ
Ramp generator						
Frequency range	f		40		100 000	Hz
Maximum voltage at C_R	V_H			5.5		V
Minimum voltage at C_R	V_L			1.8		V
Input current through R_R	I_{RR}		0		400	µA
Current transformation ratio	I_{RR}/I_{CR}			1/4		
Synchronization						
Sync output	V_{QH}	$I_{QH} = -200$ µA	4			V
	V_{QL}	$I_{QL} = 1.6$ mA			0.4	V
Sync input	V_{IH}		2			V
	V_{IL}				0.8	V
Input current	$-I_I$				5	µA
Comparator K2						
Input current	$-I_{IK2}$				2	µA
Turn-off delay[2]	$t_{d\,off}$				500	ns
Input voltage	V_{IK2}	for duty cycle				
		$\nu = 0$		1.8		V
		$\nu =$ max		5		V
Common-mode input voltage range	V_{IC}		0		5.5	V

1) At $T_{amb} = 0$ °C to 70 °C, this value falls to max. 5 mV
2) At the input: step function $\Delta V = -100$ mV ⌐→ $\Delta V = +100$ mV

Characteristics V_S = 11 V to 30 V; T_{amb} = −25 °C to +85 °C		Test conditions	Lower limit B	typ	Upper limit A	
Soft start K3, K4						
Charging current for $C_{soft\ start}$	I_{ch}			6		µA
Discharging current for $C_{soft\ start}$	I_{dch}			2		µA
Upper limiting voltage	V_{lim}			5		V
Switching voltage K4	V_{K4}			1.5		V
Output stages Q1, Q2						
Output voltage	V_{QH}				30	V
	V_{QL}	I_Q = 20 mA			1.1	V
Output current	I_Q	V_{QH} = 30 V			2	µA
ON, OFF, undervoltage K6						
Switching voltage	V		V_{ref}−30 mV		V_{ref}+30 mV	V
Input current	$-I_I$				2	µA
Turn-off delay time[1]	$t_{d\ off}$			250		ns
Error detection time[1]	t			50		ns
Dynamic current limitation K7						
Common-mode input voltage	V_{IC}		0		4	V
Input offset voltage	V_{IO}		−10		10	mV
Input current	$-I_I$				2	µA
Turn-off delay time[2]	$t_{d\ off}$			250		ns
Error detection time[2]	t			50		ns
Overvoltage K5						
Switching voltage	V		V_{ref}−30 mV		V_{ref}+30 mV	V
Input current	$-I_I$				2	µA
Turn-off delay time[1]	$t_{d\ off}$			250		ns
Error detection time[1]	t			50		ns
Supply undervoltage						
Turn-on threshold for V_S	V_S		8.8		11	V
rising		0°C<T_{amb}<70°C			10.5	V
Turn-off threshold for V_S	V_S		8.5		10.5	V
falling		0°C<T_{amb}<70°C			10	V
Input C_{filter}						
Rated voltage for rated frequency	V_R			4		V
Frequency approx. proportional to voltage within the range	V_R		3		5	V
Voltage at open sync input	$V_{C\ filter}$			1.6		V

1) At the input: step function V_{ref} = −100 mV ⌐→ V_{ref} = +100 mV
2) At the input: step function ΔV = −100 mV ⌐→ ΔV = +100 mV

Dimensioning notes for RC network

1. Determination of the minimum time during which both outputs must be disabled
   → selection of C_T; selection of $C_R \leq C_T$.

2. Determination of the VCO frequency = 2 x output frequency
   → selection of R_T.

3. Determination of the rated slope of the rising ramp generator voltage, which the maximum possible turn-on period per half wave depends on
   → selection of R_R.

4. Duration of the soft start process
   → selection of $C_{soft\ start}$.

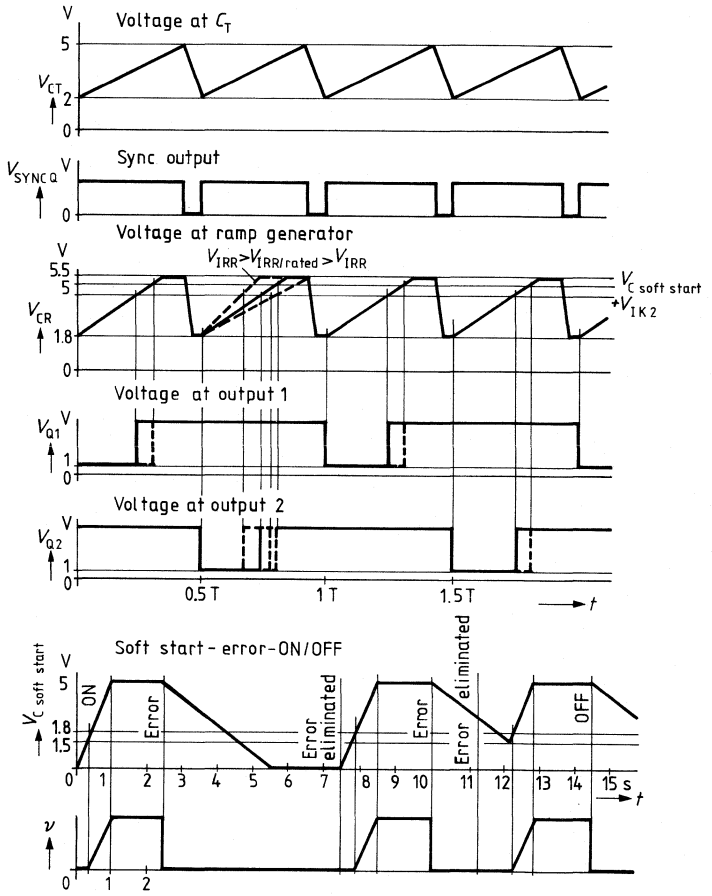
5. In the case of a free-running VCO: connect sync output with sync input.

6. Capacitance C_{filter} is not required in the free-running operation (sync input connected with sync output).

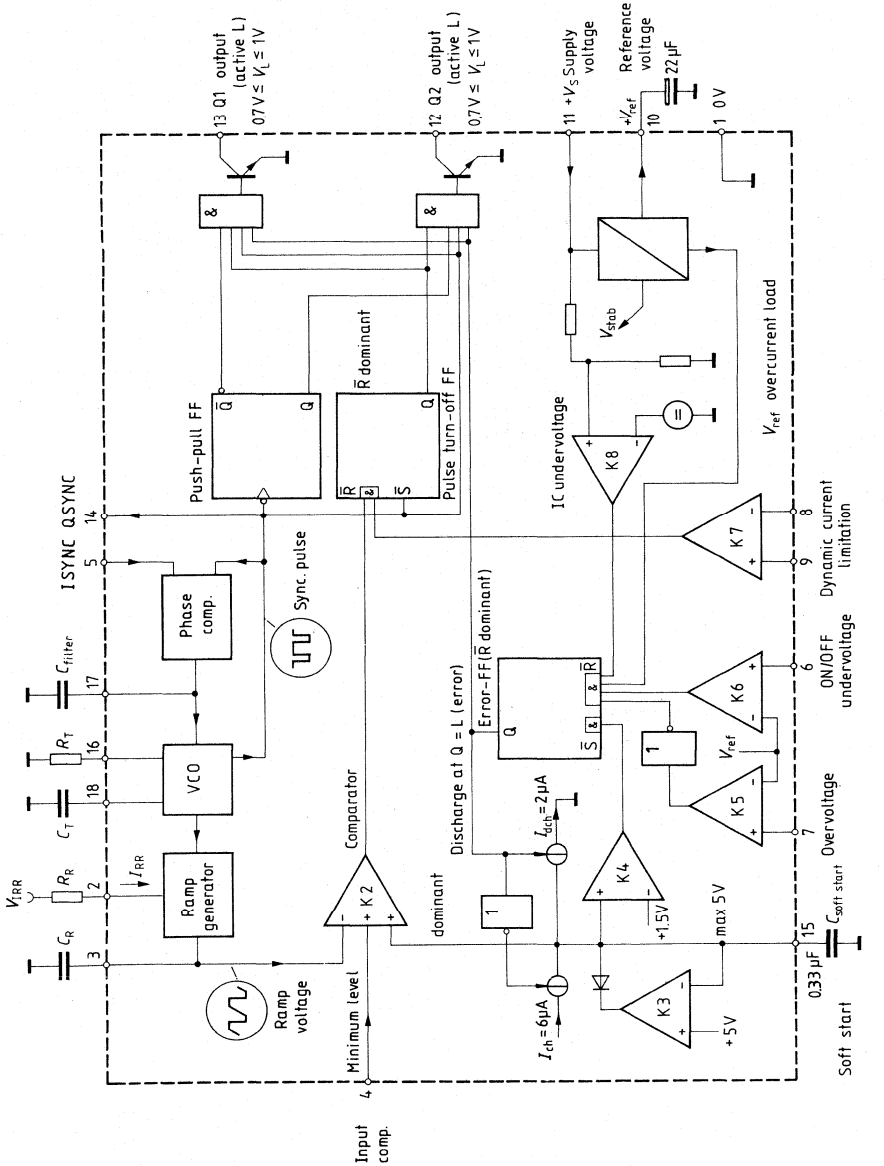
   In the case of external synchronization, that value depends on the selected operating frequency and the required maximum phase interference deviation.

Rated VCO frequency:	100 kHz	50 Hz
C_{filter} favorable:	10 nF	1 µF

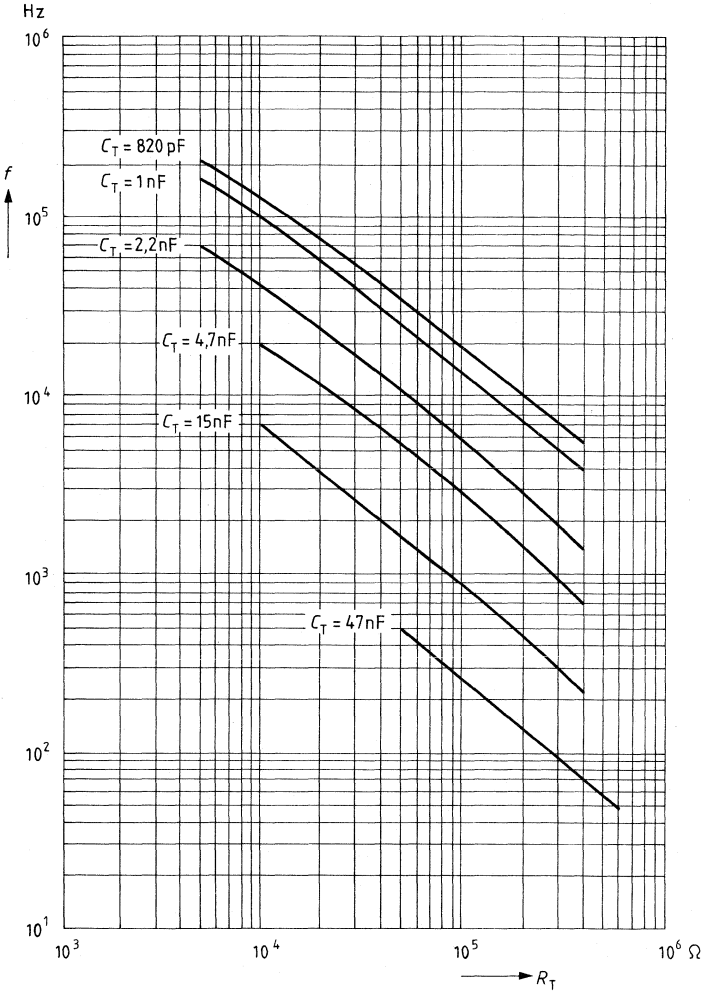
Pulse diagram



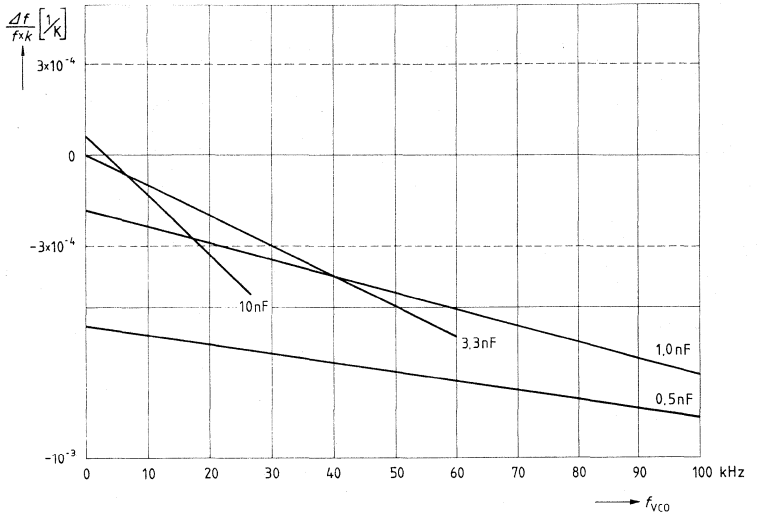
Block diagram



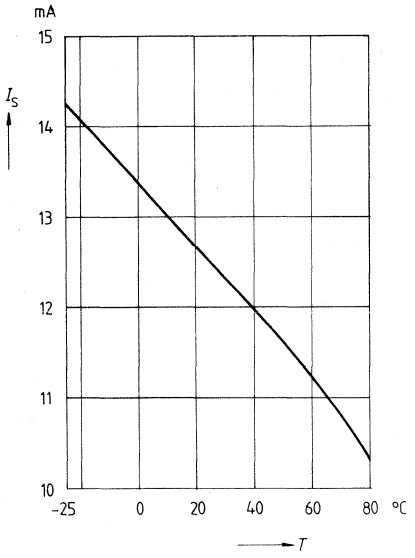
VCO frequency versus R_T and C_T



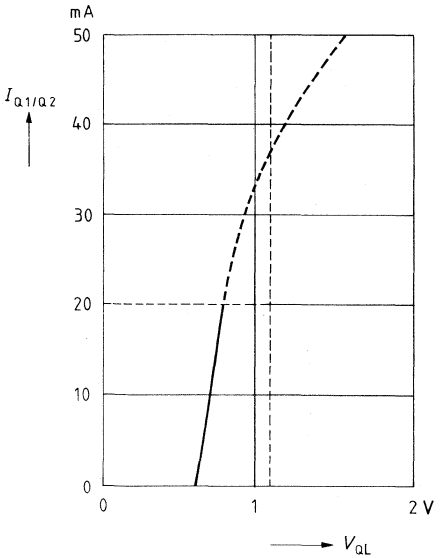
VCO temperature response
$V_S = 12$ V; ν = max.
$\frac{\Delta f_{VCO}}{f_K \times K}\left[\frac{1}{K}\right]$ with C_T as parameter



Current consumption versus temperature



Output current versus output voltage



Bipolar IC

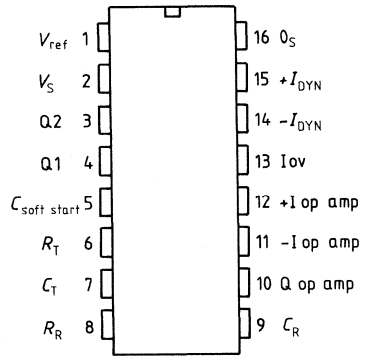
Type	Ordering code	Package	Fig. No.
TDA 4716 A	Q67000-Y865	DIP 16	8
TDA 4716 B	Q67000-Y870		

This versatile, 16-pin SMPS IC comprises digital and analog functions which are required to design high-quality flyback, single-ended, and push-pull converters in normal, half-bridge and full-bridge configurations. The component can also be used in single-ended voltage multipliers and speed-controlled motors. Malfunctions in electrical operation are recognized by the integrated op amps, and activate protective functions.

Features

- Push-pull outputs (open collector)
- Double pulse suppression
- Dynamic current limitation
- Overvoltage protection
- IC undervoltage protection
- Reference voltage source (± 2% for TDA 4716 B)
- Reference overload protection
- Feed-forward control
- Operational amplifier
- Soft start

Pin configuration
top view



Pin designation

Pin. No.	Function
1	Reference voltage V_{ref}
2	Supply voltage V_S
3	Output Q 2
4	Output Q 1
5	Soft start $C_{soft\ start}$
6	VCO R_T
7	VCO C_T
8	Ramp generator R_R
9	Ramp generator C_R
10	Operational amplifier output
11	Operational amplifier input (−)
12	Operational amplifier input (+)
13	Input overvoltage
14	Dynamic current limitation (−)
15	Dynamic current limitation (+)
16	0_S

Circuit description

The following is a description of the individual functional units and their interaction.

Voltage controlled oscillator (VCO)

The VCO generates a sawtooth voltage. The duration of the falling edge is determined by the value of C_T. The duration of the rising edge of the waveform and, therefore, approximalety the frequency, is determined by the value of R_T. During the fall time, the VCO provides a trigger signal for the ramp generator, as well as an L signal for a number of IC parts to be controlled.

Ramp generator

The ramp generator is triggered by the VCO and oscillates at the same frequency. The duration of the falling edge of the ramp generator waveform is to be shorter than the fall time of the VCO. To control the pulse width at the output, the voltage of the rising edge of the ramp generator signal is compared with a dc voltage at comparator K2. The slope of the rising edge of the ramp generator signal is controlled by the current through R_R. This offers the possibility of an additional, superimposed control of the output duty cycle. This additional control capability, called »feed-forward control«, is utilized to compensate for known interference such as ripple on the input voltage.

Push-pull flipflop

The push-pull flipflop is switched by the falling edge of the VCO. This ensures that only one output of the two push-pull outputs is enabled at a time.

Comparator K2

The two plus inputs of the comparator are switched such that the lower plus level is always compared with the level of the minus input. As soon as the voltage of the rising sawtooth edge exceeds the lower of the two plus levels, both outputs are disabled via the pulse turn-off flipflop. The period during which the respective, active output is low can be infinitely varied. As the frequency remains constant, this process corresponds to a change in duty cycle.

Operational amplifier K1

The op amp K1 is a high-quality amplifier. Fluctuations in the output voltage of the power supply are amplified by K1 and applied to the free + input of comparator K2. Variations in output voltage are, in this way, converted to a corresponding change in output duty cycle. K1 has a common-mode input voltage range between 0 V and +5 V.

Pulse turn-off flipflop

The pulse turn-off flipflop enables the outputs at the start of each half cycle. If an error signal from comparator K7 or a turn-off signal from K2 is present, the outputs will immediately be switched off.

Comparator K3

Comparator K3 limits the voltage of capacitance $C_{\text{soft start}}$ (and also at K2!) to a maximum of 5 V. The voltage at the ramp generator output may, however, rise to 5.5 V. With a corresponding slope of the rising ramp generator edge, the duty cycle can be limited to a desired maximum value.

Comparator K4

The comparator has its switching threshold at 1.5 V and sets the error flipflop with its output if the voltage at capacitance $C_{\text{soft start}}$ is below 1.5 V. However, the error flipflop accepts the set signal only if no reset pulse (error) is applied. In this way the outputs cannot be turned on again as long as an error signal is present.

Soft start

The lower one of the two voltages at the plus inputs of K2 is a measure for the duty cycle at the output. At the instant of turning on the component, the voltage at capacitor $C_{\text{soft start}}$ equals 0 V. As long as no error is present, this capacitor is charged with a current of 6 μA at the maximum value of 5 V. In case of an error, $C_{\text{soft start}}$ is discharged with a current of 2 μA. A set signal is pending at the error flipflop below a charge of 1.5 V and the outputs are enabled if no reset signal is pending simultaneously. As the minimum ramp generator voltage, however, is 1.8 V, the duty cycle at the outputs is actually increased slowly and continuously not before the voltage at $C_{\text{soft start}}$ exceeds 1.8 V.

Error flipflop

Error signals, which are led to input $\overline{R}$ of the error flipflop cause an immediate disabling of the outputs, and after the error has been eliminated, the component to switch on again using the soft start.

Comparator K5, K8, V_{ref} overcurrent load

These are error detectors which cause immediate disabling of the outputs via the error flipflop when an error occurs. After elimination of the error, the component switches on again using the soft start.

Comparator K7

K7 serves to recognize overcurrents. This is the reason why both inputs of the operational amplifier have been brought out. Turning on is resumed after error recovery at the beginning of the next half period but without using the soft start. K7 has a common-mode input voltage range between 0 V and +4 V. The delay time between occurrence of an error and disabling of the outputs is only 250 ns.

Outputs

Both outputs are transistors with open collectors and operate in a push-pull arrangement. They are actively low. The time in which only one of the two outputs is conductive can be varied infinitely. The length of the falling edge at VCO is equal to the minimum time during which both outputs are disabled simultaneously. The minimum L voltage is 0.7 V.

Reference voltage

The reference voltage source is a highly constant source with regard to its temperature behavior. It can be utilized in the external wiring of the op amp, the error comparators, the ramp generator, or other external components.

Maximum ratings

		Lower limit B	Upper limit A	
Supply voltage	V_S	−0.3	33	V
Voltage at Q1, Q2	V_Q	−0.3	33	V
Q 1/2 high				
Current at Q1, Q2	I_Q		70	mA
Q 1/2 low				
Input R_T	$V_{I\,RT}$	−0.3	7	V
Input C_T	$V_{I\,CT}$	−0.3	7	V
Input R_R	$V_{I\,RR}$	−0.3	7	V
Input C_R	$I_{I\,CR}$	−10	10	mA
Input comparator				
K5, K7	$V_{IK\,5,7}$	−0.3	33	V
Output K5	$V_{QK\,5}$	−0.3	33	V
Input op amp	$V_{I\,op\,amp}$	−0.3	33	V
Output op amp	$V_{Q\,op\,amp}$	−0.3	V_S-1	V
		but max. 7 V		
Reference voltage	$V_{Q\,ref}$	−0.3	V_{ref}	V
Input $C_{soft\,start}$	$V_{I\,soft\,start}$	−0.3	7	V
Junction temperature	T_j		125	°C
Storage temperature	T_{stg}	−55	125	°C
Thermal resistance (system-air)	$R_{th\,SA}$		60	K/W

Operating range

Supply voltage TDA 4716 A	V_S	10.5	30	V
TDA 4716 B	V_S	11	30	V
Ambient temperature TDA 4716 A	T_{amb}	0	70	°C
TDA 4716 B	T_{amb}	−25	85	°C
Frequency	f	40	100 000	Hz
VCO frequency	f_{VCO}	40	250 000	Hz
Ramp generator frequency	f_{RG}	40	250 000	Hz

Characteristics		TDA 4716 A			TDA 4716 B			
		Lower limit B	typ	Upper limit A	Lower limit B	typ	Upper limit A	
Supply voltage	V_S	10.5		30	11		30	V
Ambient temperature	T_{amb}	0		70	−25		85	°C
Supply current $C_T = 1$ nF $f_{VCO} = 100$ kHz	I_S	8		16	8		20	mA
Reference								
Reference voltage 0 mA $< I_{ref} <$ 5 mA	V_{ref}	2.35	2.5	2.65	2.45	2.5	2.55	V
Voltage change $V_S = 14$ V ± 20%	ΔV_{ref}		8			8		mV
Voltage change $V_S = 25$ V ± 20%	ΔV_{ref}		15			15		mV
Voltage change 0 mA $< I_{ref} <$ 5 mA	ΔV_{ref}			5			15	mV
Temperature coefficient	TC		0.25	0.4		0.25	0.4	mV/K
Response threshold of I_{ref} overcurrent	I_{ref}		10			10		mA
Oscillator (VCO)								
Frequency range	f	40		100000	40		100000	Hz
Frequency change $V_S = 14$ V ± 20%	$\Delta f/f$		0.5			0.5		%
Frequency change $V_S = 25$ V ± 20%	$\Delta f/f$	−1		1	−1		1	%
Tolerance $\Delta R_T = 0; \Delta C_T = 0$	$\Delta f/f$	−7		7	−7		7	%
Fall time sawtooth								
$C_T =$ 1 nF			1			1		µs
$C_T = 10$ nF			10			10		µs
RC combination	C_T	0.82		47	0.82		47	nF
VCO	R_T	5		700	5		700	kΩ
Ramp generator								
Frequency range	f_{RG}	40		100000	40		100000	Hz
Maximum voltage at C_R	V_H		5.5			5.5		V
Minimum voltage at C_R	V_L		1.8			1.8		V
Input current through R_R	I_{RR}	0		400	0		400	µA
Current transformation ratio	I_{RR}/I_{CR}		1/4			1/4		

		TDA 4716 A			TDA 4716 B			
		Lower limit B	typ	Upper limit A	Lower limit B	typ	Upper limit A	
Comparator K2								
Input current	$-I_{K2}$			2			2	µA
Turn-off delay time[1]	$t_{d\,off}$			500			500	ns
Input voltage	$V_{I\,K2}$							
Duty cycle $\nu = 0$			1.8			1.8		V
$\nu = \max$			5			5		V
Common-mode input voltage range	V_{IC}	0		5.5	0		5.5	V
Soft start K 3, K 4								
Charging current for $C_{soft\,start}$	I_{ch}		6			6		µA
Discharging current for $C_{soft\,start}$	I_{dch}		2			2		µA
Upper limiting voltage	V_{lim}		5			5		V
Switching voltage K4	V_{K4}		1.5			1.5		V
Operational amplifier								
Open-loop voltage gain	G_{V0}	60	80		60	80		dB
Input offset voltage	V_{IO}	−10		10	−10		10	mV
Temperature coefficient of V_{IO}	TC	−30		30	−30		30	µV/K
Incupt current	$-I_I$			2			2	µA
Common-mode input voltage range	V_{IC}	0		5	0		5	V
Output current	I_Q	−3		1.5	−3		1.5	mA
Rise time of output voltage	$\Delta V/\Delta t$		1			1		V/µs
Transition frequency	f_T		3			3		MHz
Phase at f_T	φ_T		120			120		degr
Output voltage $-3\ mA < I < 1.5\ mA$	$V_{Q\,H/L}$	1.5		5.5	1.5		5.5	V
Output stages Q1, Q2								
Output voltage	V_{QH}			30			30	V
$I_Q = 20$ mA	V_{QL}			1.1			1.1	V
Output current $V_{QH} = 30$ V	I_Q			2			2	µA
Dynamic current limitation K 7								
Common-mode input voltage range	V_{IC}	0		4	0		4	V
Input offset voltage	V_{IO}	−10		10	−10		10	mV
Input current	$-I_I$			2			2	µA
Turn-off delay time[1]	$t_{d\,off}$		250			250		ns
Error detection time[1]	t		50			50		ns

1) At the input: step function $\Delta V = -100$ mV ⇁ $\Delta V = +100$ mV

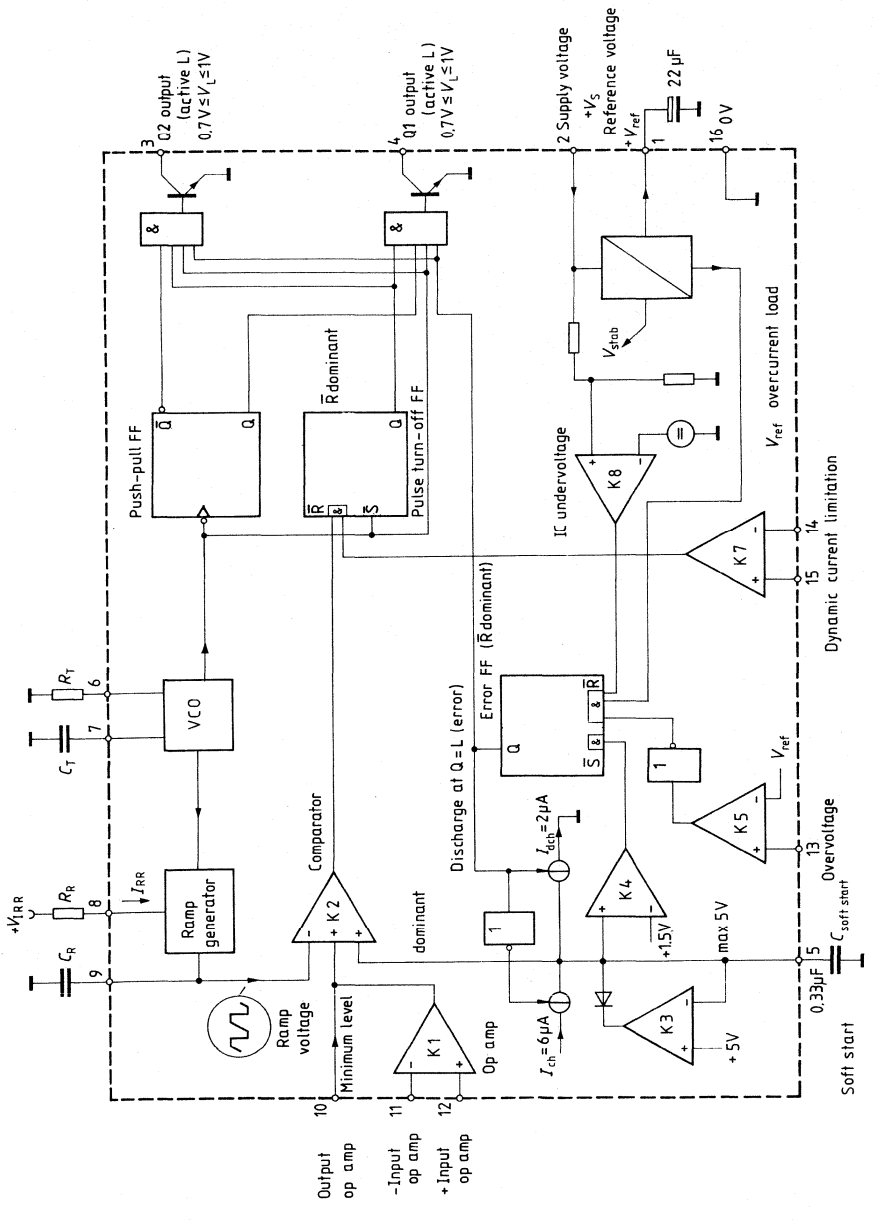
		TDA 4716 A			TDA 4716 B			
		Lower limit B	typ	Upper limit A	Lower limit B	typ	Upper limit A	
Overvoltage K 5								
Switching voltage	V	$V_{ref}-$ 30		$V_{ref}+$ 30	$V_{ref}-$ 30		$V_{ref}+$ 30	V mV
Input current	$-I_I$			2			2	µA
Turn-off delay time[1]	$t_{d\,off}$		250			250		ns
Error detection time[1]	t		50			50		ns
Supply undervoltage								
Turn-on threshold for V_S, rising	V_S	8.8		10.5	8.8		11	V
Turn-on threshold for V_S, falling	V_S	8.5		10	8.5		10.5	V

Dimensioning notes for RC network

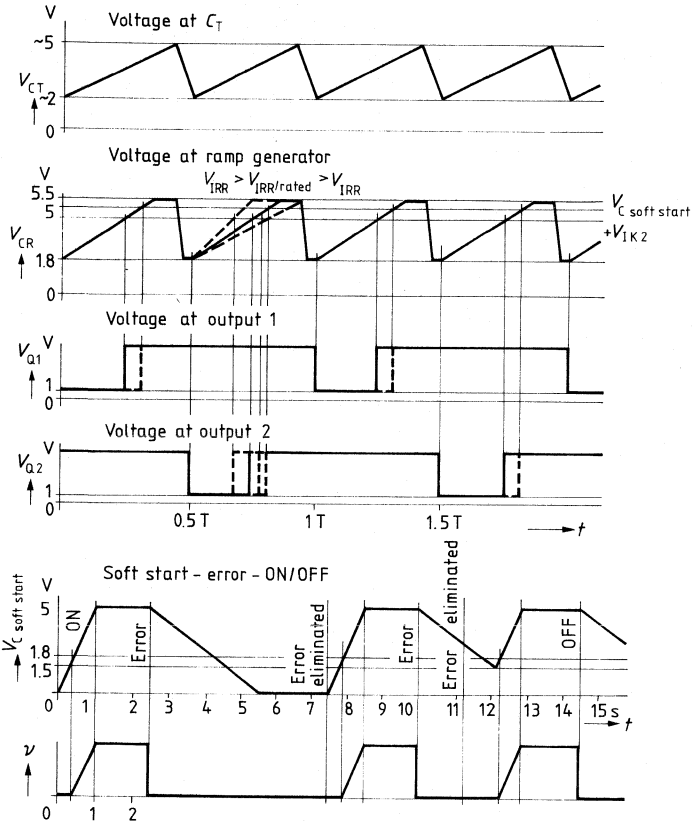
1. Determination of the minimum time during which both outputs must be disabled
   → selection of C_T; selection of $C_R \leq C_T$.
2. Determination of the VCO frequency = 2 x output frequency
   → selection of R_T.
3. Determination of the rated slope of the rising ramp generator voltage, which the maximum possible turn-on period per half wave depends on
   → selection of R_R.
4. Duration of the soft start process
   → selection of $C_{soft\,start}$
5. Wiring of the operational amplifier according to the dynamic requirements

1) At the input: step function $V_{ref} = -100$ mV ⇀↽ $V_{ref} = +100$ mV

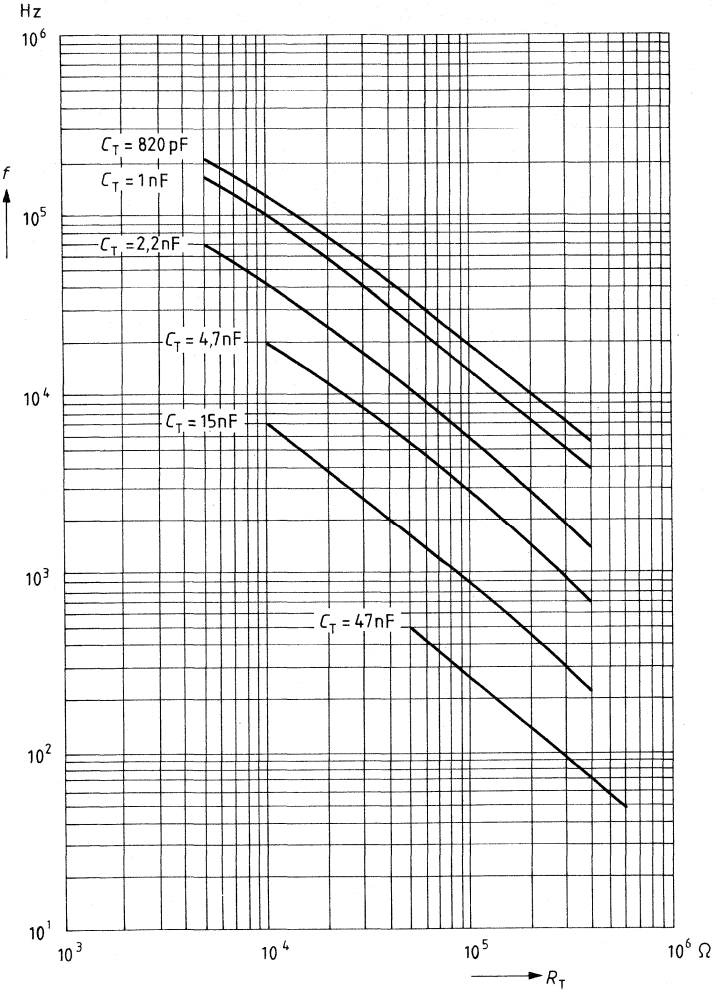
Block diagram



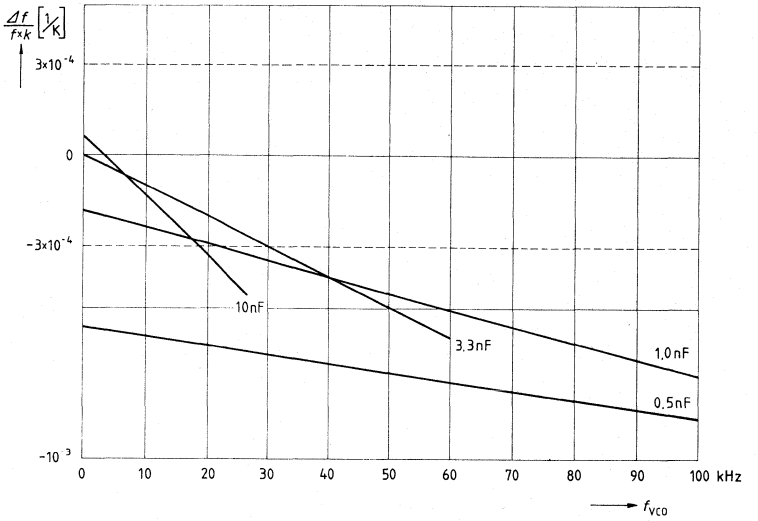
Pulse diagram



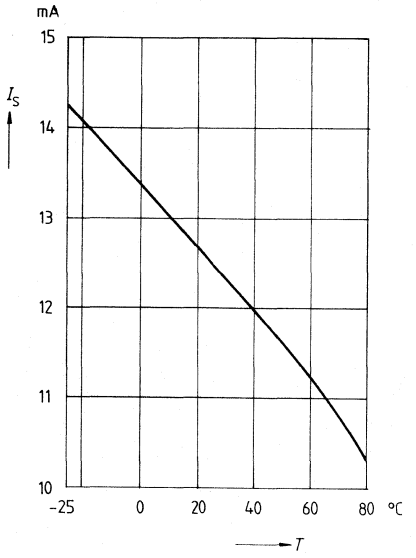
VCO frequency versus R_T and C_T



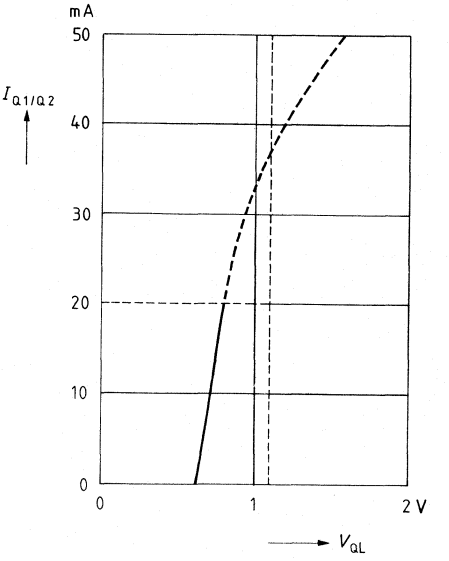
VCO temperature response
$V_S = 12$ V; $\nu = \max.$
$\frac{\Delta f_{VCO}}{f_K \times K}\left[\frac{1}{K}\right]$ with C_T as parameter



Supply current versus temperature



Output current versus L output voltage



Bipolar IC

Type	Ordering code	Package	Fig. No.
TDA 4714 A	Q67000-Y864	DIP 14	7
TDA 4714 B	Q67000-Y869		

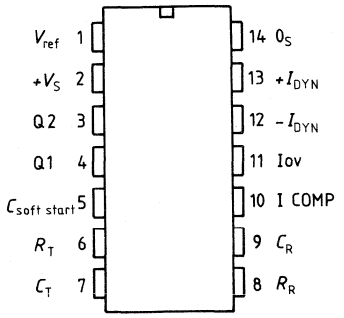
This versatile, 14-pin SMPS IC comprises digital and analog functions which are required to design high-quality flyback, single-ended, and push-pull converters in normal, half-bridge and full-bridge configurations. The component can also be used in single-ended voltage multipliers and speed-controlled motors. Malfunctions in electrical operation are recognized by the integrated op amps and activate protective functions.

Features

- Push-pull outputs (open collector)
- Double pulse suppression
- Dynamic current limitation
- Overvoltage protection
- IC undervoltage protection
- Reference voltage source (± 2% for TDA 4714 B)
- Reference overload protection
- Soft start
- Feed-forward control

Pin configuration

top view



Pin designation

Pin No.	Function
1	Reference voltage V_{ref}
2	Supply voltage V_S
3	Output Q 2
4	Output Q 1
5	Soft start $C_{soft\ start}$
6	VCO R_T
7	VCO C_T
8	Ramp generator R_R
9	Ramp generator C_R
10	Input comparator
11	Input overvoltage
12	Dynamic current limitation (−)
13	Dynamic current limitation (+)
14	0_S

Circuit description

The following is a description of the individual functional units and their interaction.

Voltage controlled oscillator (VCO)

The VCO generates a sawtooth voltage. The duration of the falling edge is determined by the value of C_T. The duration of the rising edge of the waveform and, therefore, approximately the frequency, is determined by the value of R_T. During the fall time, the VCO provides a trigger signal for the ramp generator, as well as an L signal for a number of IC parts to be controlled.

Ramp generator

The ramp generator is triggered by the VCO and oscillates at the same frequency. The duration of the falling edge of the ramp generator waveform is to be shorter than the fall time of the VCO. To control the pulse width at the output, the voltage of the rising edge of the ramp generator signal is compared with a dc voltage at comparator K2. The slope of the rising edge of the ramp generator signal is controlled by the current through R_R. This offers the possibility of an additional, superimposed control of the output duty cycle. **This additional control capability, called »feed-forward control«, is utilized to compensate for known interference such as ripple on the input voltage.**

Push-pull flipflop

The push-pull flipflop is switched by the falling edge of the VCO. This ensures that only one output of the two push-pull outputs is enabled at a time.

Comparator K2

The two plus inputs of the comparator are switched such that the lower plus level is always compared with the level of the minus input. As soon as the voltage of the rising sawtooth edge exceeds the lower of the two plus levels, both outputs are disabled via the pulse turn-off flipflop. The period during which the respective, active output is low can be infinitely varied. As the frequency remains constant, this process corresponds to a change in duty cycle.

Pulse turn-off flipflop

The pulse turn-off flipflop enables the outputs at the start of each half cycle. If an error signal from comparator K7 or a turn-off signal from K2 is present, the outputs will immediately be switched off.

Comparator K3

Comparator K3 limits the voltage at capacitance $C_{\text{soft start}}$ (and also at K2!) to a maximum of 5 V. The voltage at the ramp generator output may, however, rise to 5.5 V. With a corresponding slope of the rising ramp generator edge, the duty cycle can be limited to a desired maximum value.

Comparator K4

The comparator has its switching threshold at 1.5 V and sets the error flipflop with its output if the voltage at capacitance $C_{\text{soft start}}$ is below 1.5 V. However, the error flipflop accepts the set signal only if no reset pulse (error) is applied. In this way, the outputs cannot be turned on again as long as an error signal is present.

Soft start

The lower one of the two voltages at the plus inputs of K2 is a measure for the duty cycle at the output. At the instant of turning on the component, the voltage at capacitor $C_{\text{soft start}}$ equals 0 V. As long as no error is present, this capacitor is charged with a current of 6 µA to the maximum value of 5 V. In case of an error, $C_{\text{soft start}}$ is discharged with a current of 2 µA. A set signal is pending at the error flipflop below a charge of 1.5 V and the outputs are enabled if no reset signal is pending simultaneously. As the minimum ramp generator voltage, however, is 1.8 V, the duty cycle at the outputs is actually increased slowly and continuously not before the voltage at $C_{\text{soft start}}$ exceeds 1.8 V.

Error flipflop

Error signals, which are led to input $\overline{R}$ of the error flipflop cause an immediate disabling of the outputs, and after the error has been eliminated, the component to switch on again using the soft start.

Comparator K5, K8, V_{ref} overcurrent load

These are error detectors which cause immediate disabling of the outputs via the error flipflop when an error occurs. After elimination of the error, the component switches on again using the soft start.

Comparator K7

K7 serves to recognize overcurrents. This is the reason why both inputs of the op amp have been brought out. Turning on is resumed after error recovery at the beginning of the next half period but without using the soft start. K7 has a common-mode input voltage range between 0 V and 4 V. The delay time between occurrence of an error and disabling of the outputs is only 250 ns.

Outputs

Both outputs are transistors with open collectors and operate in a push-pull arrangement. They are actively low. The time in which only one of the two outputs is conductive can be varied infinitely. The length of the falling edge at VCO is equal to the minimum time during which both outputs are disabled simultaneously. The minimum L voltage is 0.7 V.

Reference voltage

The reference voltage source is a highly constant source with regard to its temperature behavior. It can be utilized in the external wiring of the op amp, the error comparators, the ramp generator, or other external components.

Maximum ratings

		Lower limit B	Upper limit A	
Supply voltage	V_S	−0.3	33	V
Voltage at Q1, Q2	V_Q	−0.3	33	V
Q 1/2 high				
Current at Q1, Q2	I_Q		70	mA
Q 1/2 low				
Input R_T	$V_{I\,RT}$	−0.3	7	V
Input C_T	$V_{I\,CT}$	−0.3	7	V
Input R_R	$V_{I\,RR}$	−0.3	7	V
Input C_R	$I_{I\,CR}$	−10	10	mA
Input comparator				
K2, K5, K7	$V_{IK\,2,5,7}$	−0.3	33	V
Output K5	$V_{QK\,5}$	−0.3	33	V
Reference voltage	$V_{Q\,ref}$	−0.3	V_{ref}	V
Input $C_{soft\,start}$	$V_{I\,soft\,start}$	−0.3	7	V
Junction temperature	T_j		125	°C
Storage temperature	T_{stg}	−55	125	°C
Thermal resistance (system-air)	$R_{th\,SA}$		60	K/W

Operating range

Supply voltage TDA 4714 A	V_S	10.5	30	V
TDA 4714 B	V_S	11	30	V
Ambient temperature TDA 4714 A	T_{amb}	0	70	°C
TDA 4714 B	T_{amb}	−25	85	°C
Frequency range	f	40	100000	Hz
VCO frequency	f_{VCO}	40	250000	Hz
Ramp generator frequency	f_{RG}	40	250000	Hz

Characteristics		TDA 4714 A			TDA 4714 B			
		Lower limit B	typ	Upper limit A	Lower limit B	typ	Upper limit A	
Supply voltage	V_S	10.5		30	11		30	V
Ambient temperature	T_{amb}	0		70	−25		85	°C
Supply current C_T = 1 nF f_{VCO} = 100 kHz	I_S	8		16	8		20	mA
Reference								
Reference voltage 0 mA < I_{ref} < 5 mA	V_{ref}	2.35	2.5	2.65	2.45	2.5	2.55	V
Voltage change V_S = 14 V ± 20%	ΔV_{ref}		8			8		mV
Voltage change V_S = 25 V ± 20%	ΔV_{ref}		15			15		mV
Voltage change 0 mA < I_{ref} < 5 mA	ΔV_{ref}			5			15	mV
Temperature coefficient	TC		0.25	0.4		0.25	0.4	mV/K
Response threshold of I_{ref} overcurrent	I_{ref}		10			10		mA
Oscillator (VCO)								
Frequency range	f	40		100 000	40		100 000	Hz
Frequency change V_S = 14 ± 20%	$\Delta f/f$		0.5			0.5		%
Frequency change V_S = 25 V ± 20%	$\Delta f/f$	−1		1	−1		1	%
Tolerance $\Delta R_T = 0; \Delta C_T = 0$	$\Delta f/f$	−7		7	−7		7	%
Fall time sawtooth C_T = 1 nF			1			1		µs
C_T = 10 nF			10			10		µs
RC combination	C_T	0.82		47	0.82		47	nF
VCO	R_T	5		700	5		700	kΩ
Ramp generator								
Frequency range	f_{RG}	40		100 000	40		100 000	Hz
Maximum voltage at C_R	V_H		5.5			5.5		V
Minimum voltage at C_R	V_L		1.8			1.8		V
Input current through R_R	I_{RR}	0		400	0		400	µA
Current transformation ratio	I_{RR}/I_{CR}		1/4			1/4		

		TDA 4714 A			TDA 4714 B			
		Lower limit B	typ	Upper limit A	Lower limit B	typ	Upper limit A	
Comparator K2								
Input current	$-I_{K2}$			2			2	µA
Turn-off delay time[1]	$t_{d\,off}$			500			500	ns
Input voltage	$V_{I\,K2}$							
Duty cycle $\nu = 0$			1.8			1.8		V
Duty cycle ν = max.			5			5		V
Common-mode input voltage range	V_{IC}	0		5.5	0		5.5	V
Soft start K 3, K 4								
Charging current for $C_{soft\ start}$	I_{ch}		6			6		µA
Discharging current for $C_{soft\ start}$	I_{dch}		2			2		µA
Upper limiting voltage	V_{lim}		5			5		V
Switching voltage K4	V_{K4}		1.5			1.5		V
Output stages Q1, Q2								
Output voltage	V_{QH}			30			30	V
$I_Q = 20$ mA	V_{QL}			1.1			1.1	V
Output current	I_Q			2			2	µA
$V_{QH} = 30$ V								
Dynamic current limitation K 7								
Common-mode input voltage range	V_{IC}	0		4	0		4	V
Input offset voltage	V_{IO}	−10		10	−10		10	mV
Input current	$-I_I$			2			2	µA
Turn-off delay time[1]	$t_{d\,off}$		250			250		ns
Error detection time[1]	t		50			50		ns
Overvoltage K 5								
Switching voltage	V	$V_{ref}-$ 30		$V_{ref}+$ 30	$V_{ref}-$ 30		$V_{ref}+$ 30	V mV
Input current	$-I_I$			2			2	µA
Turn-off delay time[2]	$t_{d\,off}$		250			250		ns
Error detection time[2]	t		50			50		ns
Supply undervoltage								
Turn-on threshold for V_S, rising	V_S	8.8		10.5	8.8		11	V
Turn-on threshold for V_S, falling	V_S	8.5		10	8.5		10.5	V

1) At the input: step function $\Delta V = -100$ mV ⌐→ $\Delta V = +100$ mV
2) At the input: step function $V_{ref} = -100$ mV ⌐→ $V_{ref} = +100$ mV

Dimensioning notes for RC network

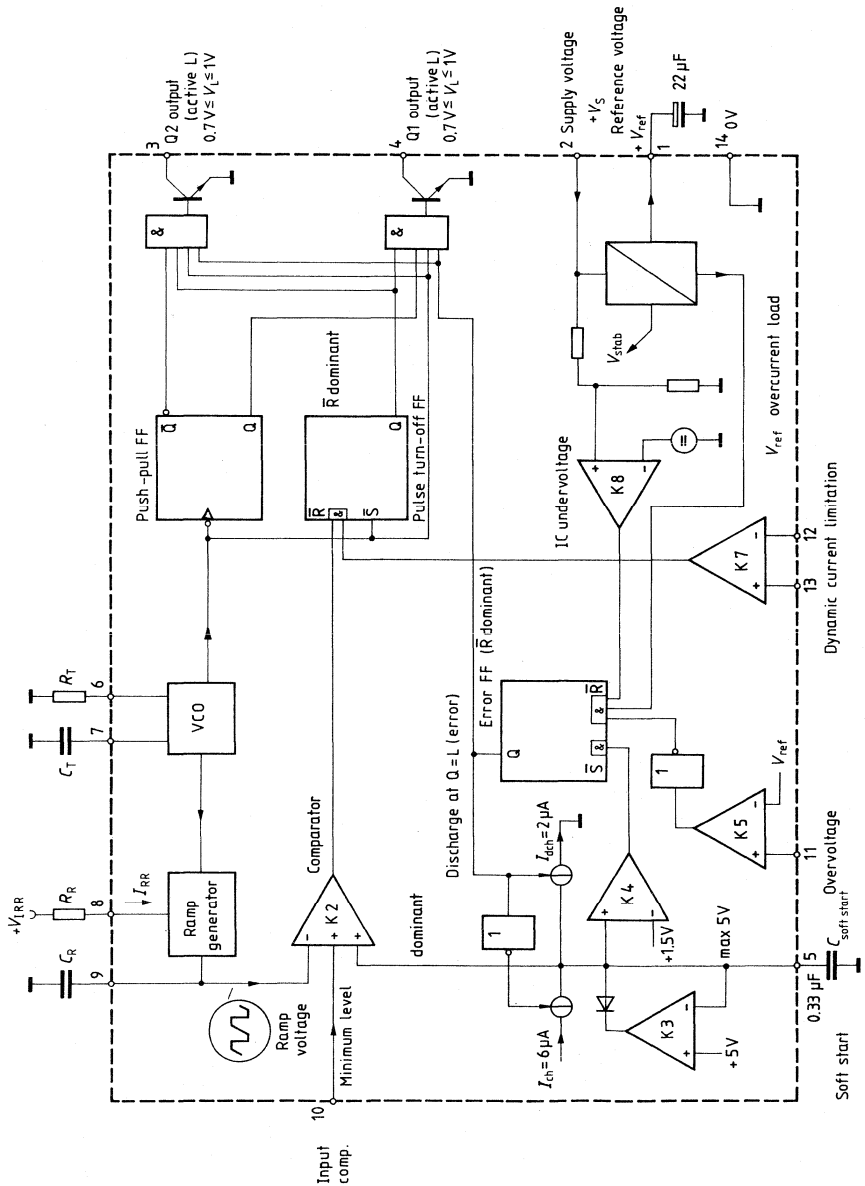
1. Determination of the minimum time during which both outputs must be disabled
   → selection of C_T; selection of $C_R \leq C_T$.

2. Determination of the VCO frequency = 2 x output frequency
   → selection of R_T.

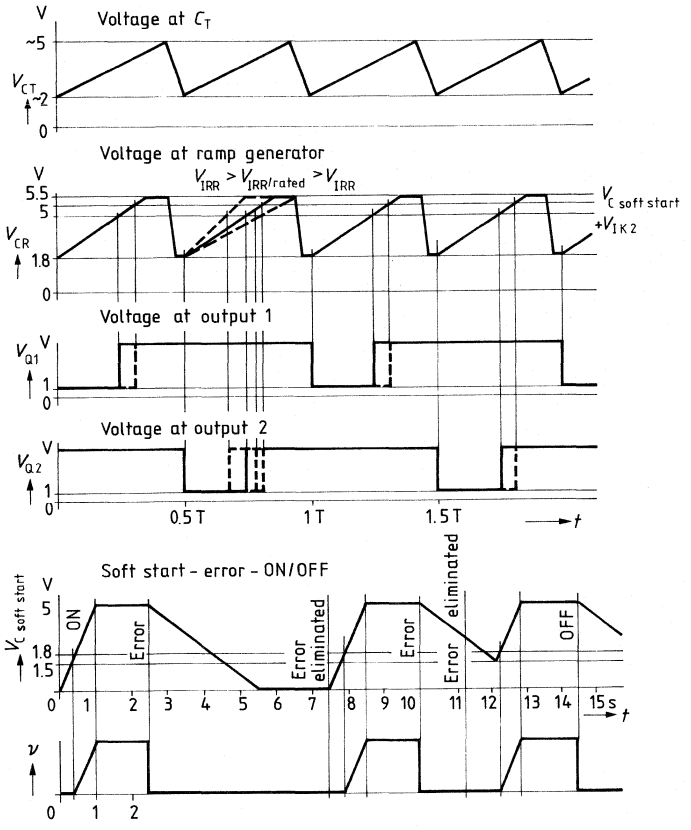
3. Determination of the rated slope of the rising ramp generator voltage, which the maximum possible turn-on period per half wave depends on
   → selection of R_R.

4. Duration of the soft start process
   → selection of $C_{soft\ start}$.

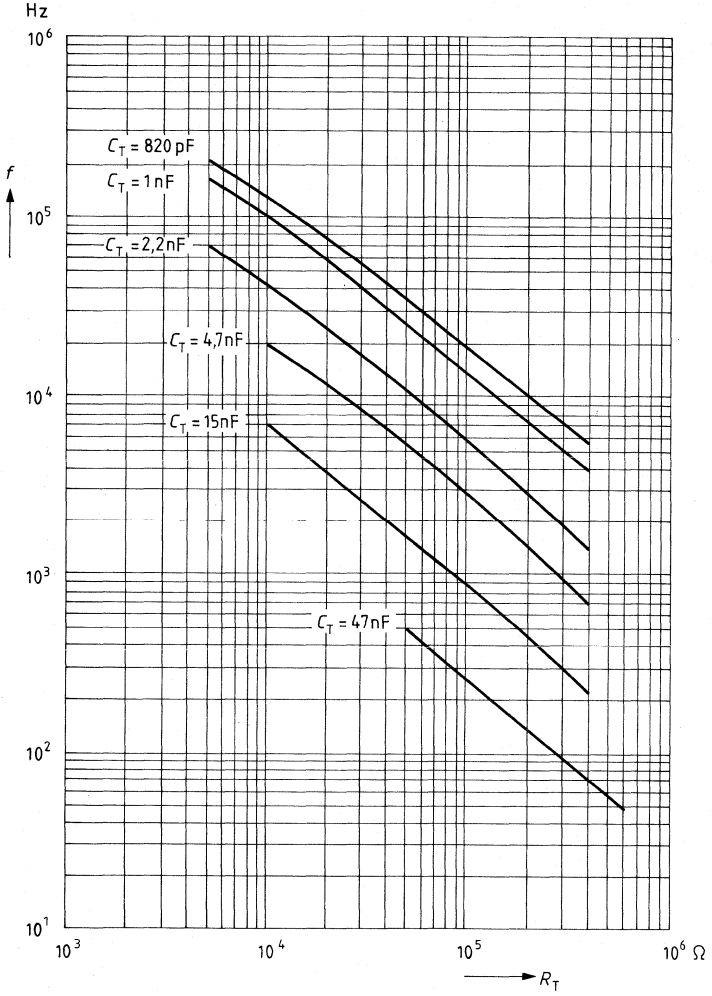
Block diagram



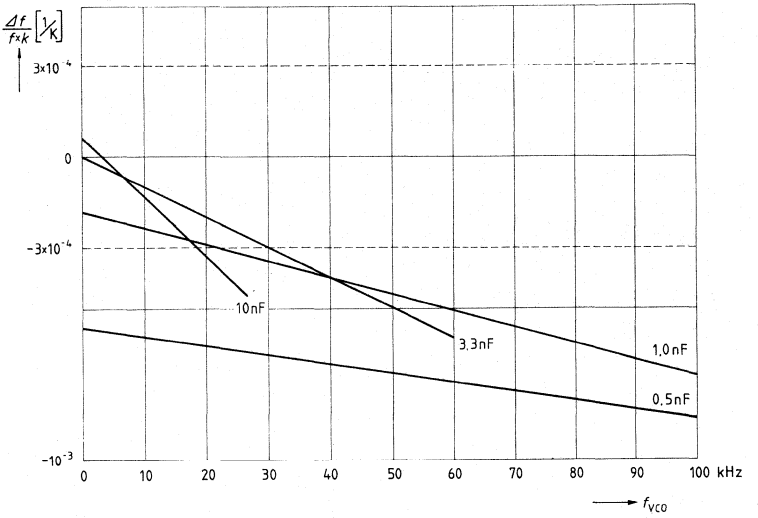
Pulse diagram



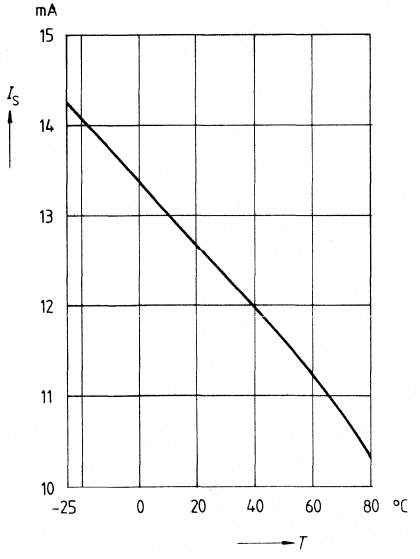
VCO frequency versus R_T and C_T



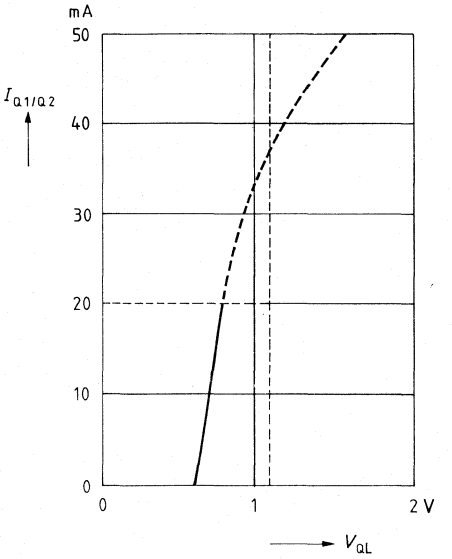
VCO temperature response
$V_S = 12$ V; ν = max.
$\frac{\Delta f_{VCO}}{f_K \times K}\left[\frac{1}{K}\right]$ with C_T as parameter



Supply current versus temperature



Output current versus L output voltage



Drivers and Interface Circuits, Driver Stages, Level Converters, LED Display Drivers, Transistor Arrays

Quad Drivers incl. Short-Circuit Signaling

FZL 4141 B FZL 4145 B

Preliminary data **Bipolar IC**

Type	Ordering code	Package	Fig. No.
FZL 4141 B	Q67000-H2357	DIP 18	11
FZL 4145 B	Q67000-H2358		

Functional description

The IC is comprised of four driver circuits capable of driving power transistors for high output currents. The output transistors are protected against short-circuit to ground and supply voltage. The input threshold can be adjusted between 1.5 V and 7 V. In the event of overloading or shorting of an output, a signaling process will respond.

Circuit description

Each driver circuit has one active H input DI and a common enable input ENA (active H) is provided for all stages. The Q outputs are designed to drive the output transistors. The load current is sampled via pin W. If the load current exceeds the preset value, the output stage switches off. Switching-on again is provided by the built-in clock generator. Its operation requires an external capacitor C_T at pin C. If C_T is bridged by a break-key, switching on can only be carried out by operating a key. The duty cycle of the clock generator is 1:50 (e.g. 40 µs/2 ms with $C_T = 33$ nF).

If one of the four output stages is shorted to ground or has overcurrent, the short-signaling output will go L. In clock-governed operation (i.e. when there is automatic switching on by the clock and not by a key), SQ switches on and off at the clock rate as long as a short circuit or overload exists. SQ is an open-collector output.

Unused W pins must be connected to V_S. Open W pins simulate a short circuit and activate the signaling output.

The switching threshold at inputs DI and ENA can be adjusted between 1.5 V and 7 V via connection TS:

$V_{TS} = 0$ V: input threshold = 1.5 V (for 5 V logic)
$V_{TS} = 0$ to 5 V: input threshold = $V_{TS} + 1.5$ V
$V_{TS} = V_S$: input threshold = 7 V (for 12/15 V and 24/28 V logic)

If the output is disabled due to the logic states of inputs DI or ENA this disable is effective over the total supply voltage range between $V_S = 0$ V and $V_S = 35$ V.

The inputs are protected with clamp diodes.

Maximum ratings

		Lower limit B	Upper limit A		Notes
Supply voltage	V_S	−0.3	35	V	
Supply voltage	V_S	−0.3	45	V	100 ms duration, 1 s interval
Input voltage at DI and ENA	$V_{DI, ENA}$	−0.3	35	V	1)
Voltage at TS and SQ	$V_{TS, SQ}$	−0.3	45	V	
Output voltage V_Q and voltage at C	V_Q, V_C	−0.3	V_S	V	
Voltage at W	V_W	V_S−5	V_S	V	3)
Input current at DI and ENA	$I_{DI, ENA}$	−3	1	mA	2)
	$I_{DI, ENA}$	−6	2	mA	2) 100 ms duration, 1 s interval
	$I_{DI, ENA}$	−6	5	mA	2) 100 µs duration, 1 ms interval
Output current at SQ	I_{SQ}		8	mA	
Power dissipation of all input diodes	P_{tot}		50	mW	

Operating range

Supply voltages for					
input threshold 1.5 V	V_S	4.5	35	V	$V_{TS} = 0$ V
input threshold 1.5 V to 6.5 V	V_S	V_{TS}+4.5	35	V	$V_{TS} = 0$ V to 5 V
input threshold 7 V	V_S	10	35	V	$V_{TS} = V_S$

Notes: 1) $V_{DI, ENA} > 35$ V requires a protective resistor before DI, ENA.
2) $V_{DI, ENA}$ may increase to more than 35 V during current nodes.
3) Unused W connections must be connected to V_S.

Characteristics

Supply voltage 4.5 V ≤ V_S ≤ 30 V

Temperature range 1 and 5

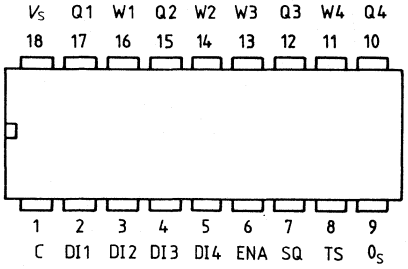
		Test conditions	Lower limit B	typ	Upper limit A	
Supply current	I_S	$V_{ENA} = 0$ V, $V_W = V_S$		6	8.5	mA
H input voltage at DI, ENA	V_{IH}	$V_{TS} = 0$ V	2			V
H input voltage at DI, ENA	V_{IH}	$V_{TS} = V_S$	8			V
L input voltage at DI, ENA	V_{IL}	$V_{TS} = 0$ V			0.7	V
L input voltage at DI, ENA	V_{IL}	$V_{TS} = V_S$			6	V
Input current at DI, ENA	$I_{DI, ENA}$	$0.5\,V \leq V_{DI, ENA} \leq 30$V	50		200	µA
L output voltage at SQ	V_{SQL}	$I_{SQ} = 5$ mA			0.5	V
Output current available[1]	I_Q	$V_Q = V_S - 1.5$ V	1.5	2.5		mA
	I_Q	$T_{amb} = 0$ °C, $V_Q = V_S - 1.5$ V	1.7			mA
Current from TS	$-I_{TS}$	$V_{TS} = 0$ V		2	10	µA
Switching threshold at W	V_W		$V_S - 0.6$	$V_S - 0.5$	$V_S - 0.4$	V
Current in W	I_W				100	µA
Current from C	$-I_C$	$T_{amb} = 20$ °C	12	20	34	µA
Current in C	I_C	$T_{amb} = 20$ °C	0.6	1	1.7	mA
Upper switching threshold at C	V_{CU}	$T_{amb} = 20$ °C	1.6	2.1	1.7	V
Lower switching threshold at C	V_{CL}	$T_{amb} = 20$ °C	0.6	0.9	1.2	V
Saturation voltage at T[2]	V_{QR}	$V_W = V_S - 2$ V, $I_Q = 0$		$V_S - 0.3$		V
H output voltage	V_{QH}	$V_{ENA} = 0$ V	$V_S - 0.25$	$V_S - 0.02$		V

1) The actual output current is typically 0.5 mA higher, a value which is required as current for the short-circuit protection. However, only the value specified above is available to drive the external output transistors.

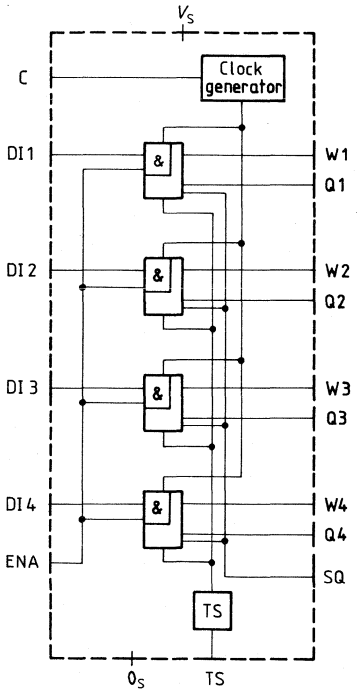
2) See block diagram

Pin configuration

top view

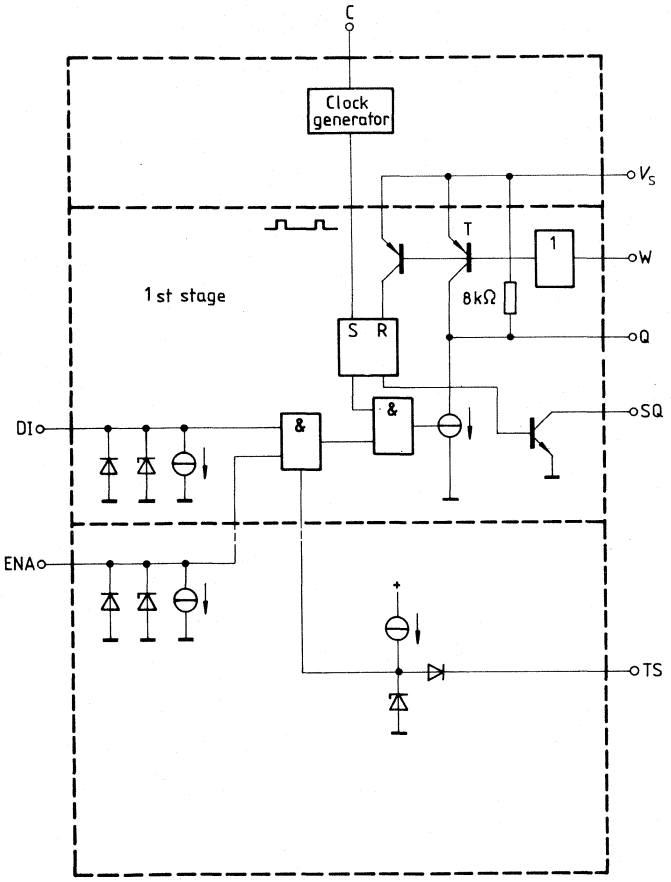


Block diagram



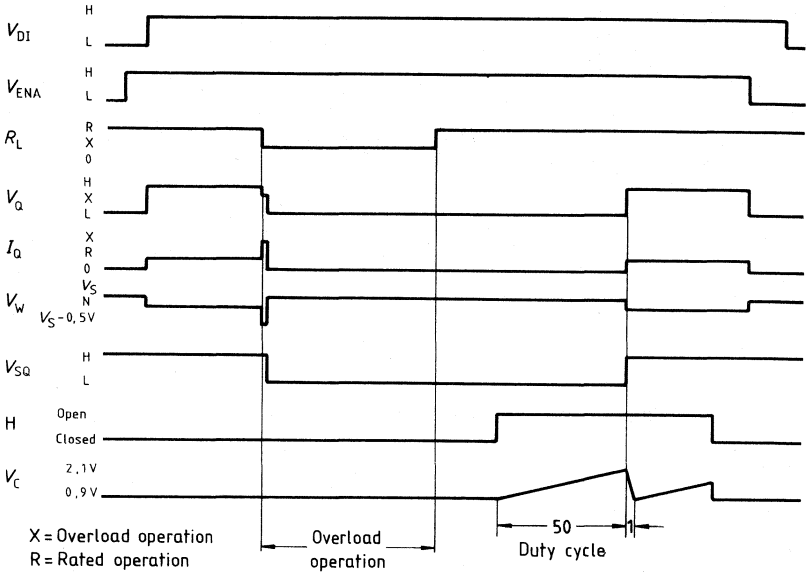
DI Driver input
ENA Enable input
C Clock capacitor
Q Output
TS Input for threshold switching
W Input for output current limiter
SQ Signaling output

Schematic circuit diagram of a stage

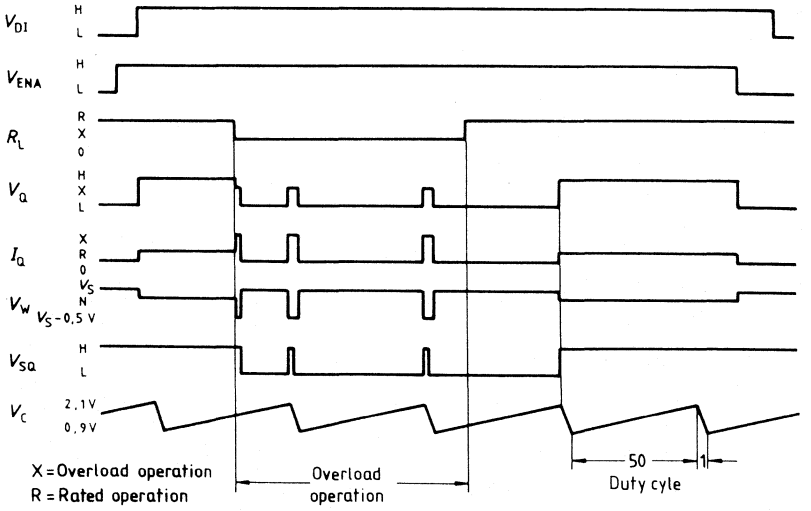


DI Driver input
ENA Enable input
C Clock capacitor
SQ Signaling output
Q Output
TS Input for threshold switching
W Input for output current limiter

Mode of operation: switching-on again after overload with key H



Mode of operation: automatic switching-on again after overload



Typical application circuits

The load conditions at Q depend on the permissible power dissipation of the power transistors used. The pulsed power dissipation in case of a short circuit must be observed.

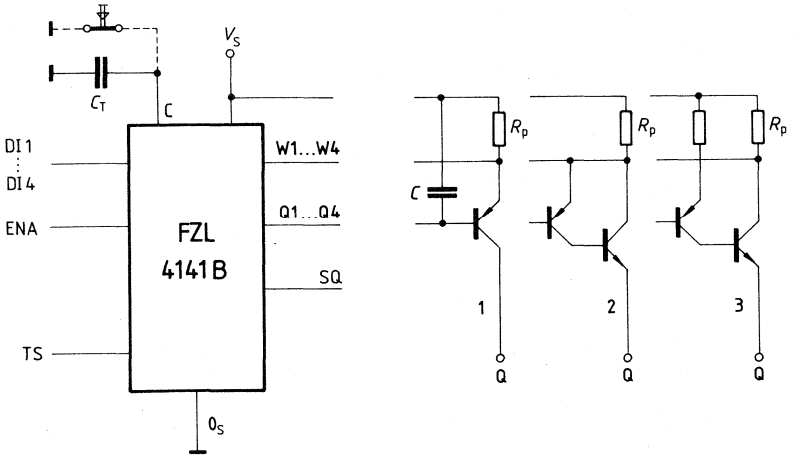
In order to suppress oscillations of the power stage in case of a short circuit, a capacitor C at Q1 to Q4 is necessary if e.g., fast switching transistors are used.

Typical value C approx. 20 nF.

The output circuit 1 is suited for currents up to approx. $I_Q = 100$ mA.

The output circuits 2 and 3 are suited for currents up to approx. $I_Q = 2$ A. A minimum power dissipation can be achieved with circuit 3.

A break key in parallel to C_T allows a manual switch-on in case of short circuit.



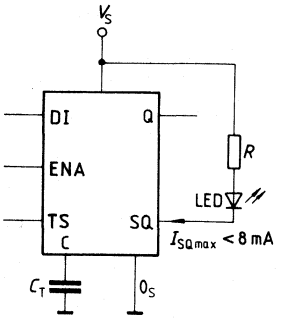
R_P = Precision resistor (current measurement)
$C_T = 0.8 \times t_p$ (nF, µs)
t_p = Short-circuit current pulse length

Note

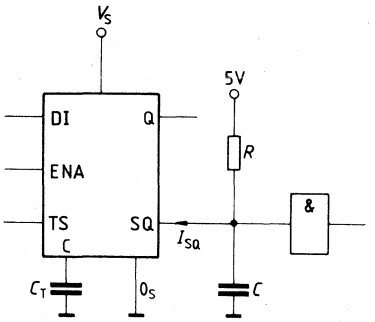
Circuit 1 does not permit a capacitor between Q1 and Q4 and the collector.
Circuit 2 does not permit a capacitor between Q1 and Q4 and base or emitter, respectively.
Otherwise too high current spikes would arise in case of a short circuit.

Typical application of short-circuit signaling output SQ

1. LED display



2. TTL/CMOS/LSL driving



If the pulses that appear at SQ during clocked operation disturb the remainder of the circuit, a lowpass filter will be necessary. For a load current of $I_{SQ} = 1$ mA a capacitor C of approx. 10 nF is necessary to limit the output pulses of up to 10 µs (depending on C_T) to 1 V. Signaling occurs after approx. 50 µs.

Type	Ordering code	Package	Fig. No.
FZH 211 S	Q67000-H639-S1	DIP 16	8
FZH 215 S	Q67000-H2431		

Four NAND drivers with open collector outputs, 2 inputs, and N inputs for delay circuits. The input threshold can be switched to LSL, TTL, or CMOS level, depending on the supply voltage used.

Typical application

Driver up to 30 V/150 mA, relay driver, and level converter.

Calculation of the load resistance for wired AND connection is carried out as described for FZH 161/181. In the case of wired AND connection and N wiring, the capacitors C_N must have identical vaules.

Additional maximum ratings

		Test conditions	Lower limit B	Upper limit A	Unit
Supply voltage	V_S		0	30	V
Input voltage	V_I		−0.5	30	V
Voltage between 2 inputs	V_{II}			30	V
Voltage at output, output transistor cut off	V_{QH}			30	V
Voltage at output, output transistor conducting	V_{QL}		0		V
Output current	I_{QL}			150	mA
Capacitance at Q	C_L			5	nF
Capacitance between N and Q	C_N			0.1	µF

Moreover, the maximum ratings defined for the LSL series FZ 100 apply (refer to LSL data book).

Functional range

Temperature range 1 and 5

Supply voltage range 1	V_S	TTL threshold at A, B	4	7	V
Supply voltage range 2	V_S	LSL threshold at A, B	9	30	V
Supply voltage	V_S	Switching of threshold at A, B at $V_S = 8$ V, typical	4	30	V

Characteristics in the 5 V range Temperature range 1 and 5		Test conditions	Lower limit B	typ	Upper limit A	
Supply voltage	V_S		4		7	V
H-input voltage	V_{IH}	$V_S = V_{SB}$	2			V
L-input voltage	V_{IL}	$V_S = V_{SA}$ and V_{SB}			0.8	V
Static noise immunity	V_{sn}		0.4	1.0		V
L-output voltage	V_{QL}	I_{QL} 1,6 mA | $V_{IH} = 2$ V		0.7	0.8	V
L-output voltage	V_{QL}	$I_{QL} = 100$ mA | $V_S = V_{SB}$			1.3	V
L-output voltage[1]	V_{QL}	$I_{QL} = 150$ mA			1.5	V
H-input current	I_{IH}	$V_{IH} = 30$ V | $V_S = V_{SA}$			1	µA
L-input current	$-I_{IL}$	$V_{IL} = 0$ V		5	50	µA
H-output current	I_{QL}	$V_{IL} = 0.8$ V, $V_{QH} = 30$ V, $V_S = V_{SB}$			50	µA
Supply current per package	I_S	$V_S = 7$ V, $V_I = 0$ V	1.5	3	5	mA

Characteristics in the 12 V, 15 V, 24 V ranges Temperature range 1 and 5						
Supply voltage	V_S		9		30	V
H-input voltage	V_{IH}	$V_S = V_{SB}$	8			V
L-input voltage	V_{IL}	$V_S = V_{SA}$ and V_{SB}			6	V
Static noise immunity	V_{sn}		2.5	5.0		V
L-output voltage	V_{QL}	$I_{QL} = 100$ mA | $V_{IH} = 8$ V		1	1.3	V
L-output voltage[1]	V_{QL}	$I_{QL} = 150$ mA | $V_S = V_{SB}$			1.5	V
H-input current	I_{IL}	$V_{IH} = 30$ V | $V_S = V_{SA}$			1	µA
L-input current	$-I_{IL}$	$V_{IL} = 0$ V		5	50	µA
H-output current	I_{QH}	$V_{IL} = 6$ V, $V_{QH} = 30$ V, $V_S = V_{SB}$			50	µA
Supply current per package	I_S	$V_S = 30$ V, $V_I = 0$ V	1.5	3	5	mA

Switching characteristics at $V_S = 12$ V, $T_{amb} = 25$ °C,

Signal propagation time	t_{PLH}	$V_{SC} = 12$ V $R_C = 760\ \Omega$ $C_L = 15$ pF		550		ns
	t_{PHL}			200		ns
Signal transition time	t_{TLH}			90		ns
	t_{THL}			25		ns

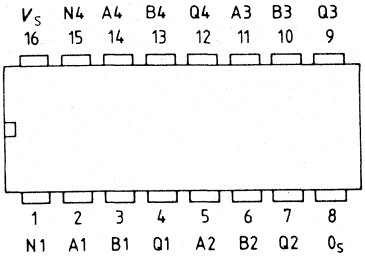
Signal transition times at Q
with C_N wiring between N and Q:

$$\left.\begin{aligned} t_{THL} &= 6 \cdot C_R \cdot (V_{QH} - V_{QL}) \\ t_{TLH} &= 15 \cdot C_R \cdot (V_{QH} - V_{QL}) \end{aligned}\right\} \text{(µs, µF, V)}$$

typical values for $C_R > 0.02$ µF

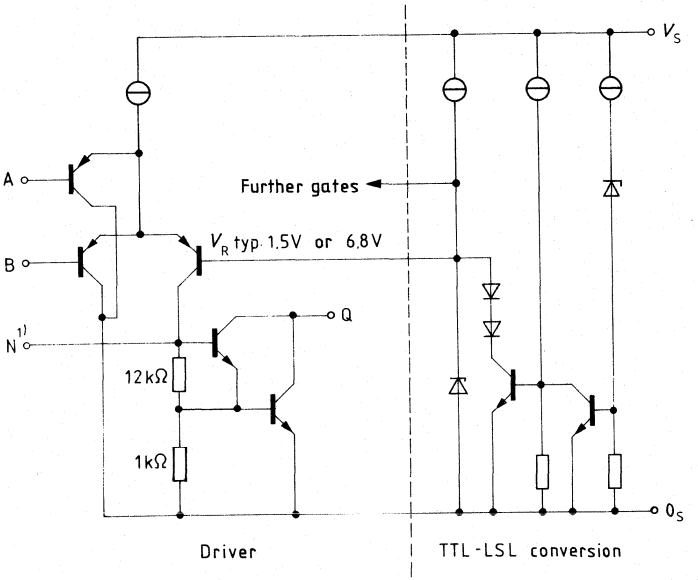
1) The sum of all output currents per package may not exceed 400 mA for the FZH 211 S and 350 mA for the FZH 215 S.

Pin configuration
top view



A, B = inputs
Q = output

Schematic (one gate)



Logic function $Q = \overline{A \wedge B}$

1) only in case of gate 1 and 4

Bipolar IC

Type	Ordering code	Package	Fig. No.
UAA 170	Q67000-A940	DIP 16	8

IC for driving 16 light emitting diodes. Depending on the input voltage, the individual LEDs are driven within one row in form of a light spot. The UAA 170 provides a linear relation between control voltage and the driven LED.

By using an appropriate circuitry, the brightness of the LEDs can be varied and the crossing over of the light spot can be set between "smooth" and "abrupt". By connecting two ICs in parallel, up to 30 LEDs can be driven.

Maximum ratings

Supply voltage	V_S	18	V
Input voltages	V_{11}, V_{12}, V_{13}	6	V
Load current	I_{14}	5	mA
Junction temperature	T_j	125	°C
Storage temperature range	T_{stg}	−40 to 125	°C
Thermal resistance (system-air)	$R_{th\,SA}$	90	K/W

Operating range

Supply voltage range (LED red)[1]	V_S	11 to 18	V
Ambient temperature range	T_{amb}	−25 to 85	°C

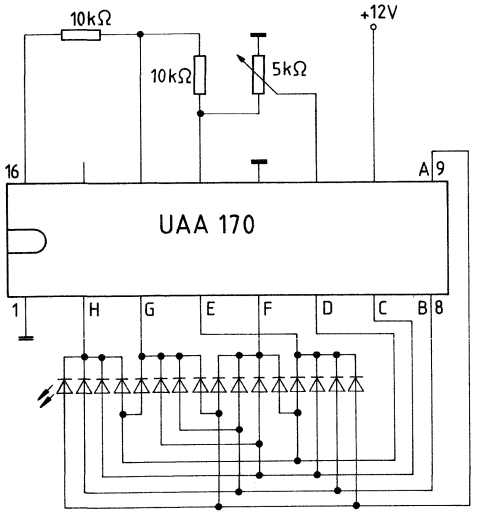
1) The lower limit only applies to a forward voltage of the LEDs of approx. 1.5 V (red LEDs); the lower limit increases with higher forward voltage

Characteristics

$V_S = 12$ V; $T_{amb} = 25$ °C

		min	typ	max	
Current consumption ($I_{14} = 0$; $I_{16} = 0$)	I_S	2	4	10	mA
Control input current	I_{11}	−2			µA
Reference input current	I_{12}, I_{13}	−2			µA
Voltage difference	$\Delta V_{12/13}$	1.4		6.0	V
Voltage difference for smooth light transition	$\Delta V_{12/13}$	1.4			V
Voltage difference for abrupt light transition	$\Delta V_{12/13}$	4			V
Voltage difference	$\Delta V_{12/13}$	4			V
Stabilized voltage $I_{14} = 300$ µA	V_{14}		5.0	6.0	V
$I_{14} = 5$ mA	V_{14}	4.5			V
Reference input voltage	$V_{ref\,max}$	1.4		6.0	V
	$V_{ref\,min}$	0		4.6	V
Tolerance of forward voltages of LEDs, mutually	ΔV_D			0.5	V
Output current for LEDs	ΣI_D		25		mA

Test circuit



16 LEDs.

Scale display with light emitting diodes

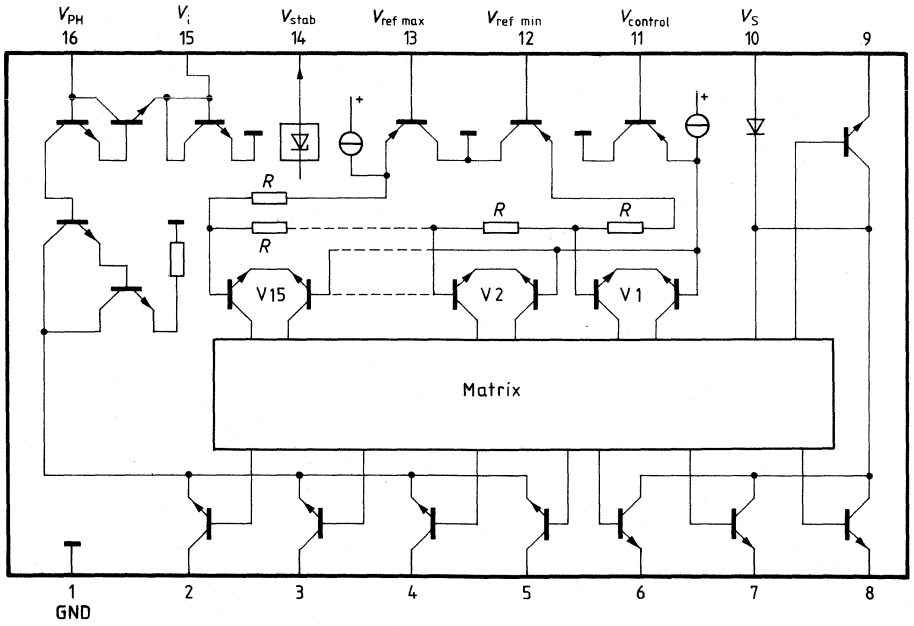
Scale displays by means of a wandering light spot are particularly suitable for indicating approximate values. Applications of this kind are level sensors, VU meters, tachometers, radio scales etc. When applying the displays in measuring equipment, multicolored light emitting diodes can be used as range limitation. Ring scales are obtained by a circular arrangement of the diodes. The UAA 170 IC has especially been developed for driving a scale of 16 LEDs.

The input voltages at pins 11, 12 and 13 are freely selectable between 0 V and 6 V. Any kind of adjustment becomes possible by suitable voltage drivers. The DC value $V_{control}$ is always assigned to a certain spot of the diode chain.

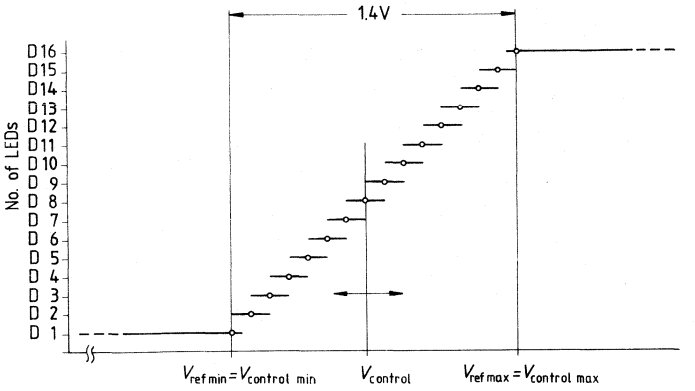
The voltage difference between pins 12 and 13 thereby corresponds to the possible indication range. At the same time $\Delta V_{12/13}$ defines the light transition between two diodes. With $\Delta V_{12/13}$ approx. 1.4 V, the light point glides smoothly along the scale. With increasing voltage difference, the passage becomes more abrupt. With $\Delta V_{12/13}$ approx. 4 V, the light point jumps from diode to diode.

Input voltages beyond the selected indication range cause the diodes D1 or D16 respectively, to light up, identifying only that the range has been exceeded.

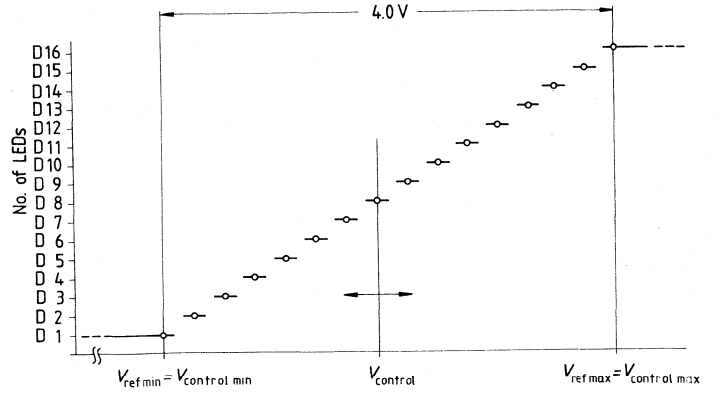
Block diagram



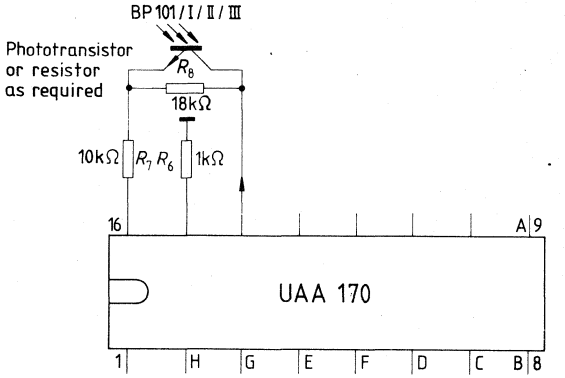
Indication for smooth transition UAA 170



Indication for abrupt transition UAA 170



Brightness control

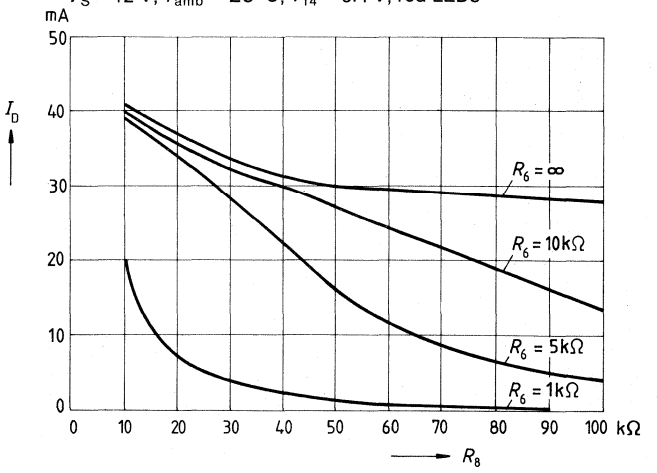


Pins 14, 15, and 16 are intended to determine the diode current. Corresponding to the desired light intensity, the forward current of the diodes is linearly variable in the range I_f approx. 0 mA to 50 mA. The resistance at pin 15 defines the adjusting range. The resistances between pin 14 and 16 determine the current.

With the aid of a phototransistor, such as BP 101, the light intensity of the LEDs can be adjusted to the light fluctuations of the environment.

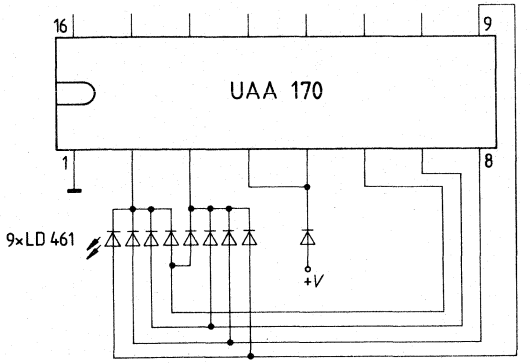
Diode current versus base emitter resistance

$V_S = 12$ V; $T_{amb} = 25$ °C; $V_{14} = 5.4$ V; red LEDs

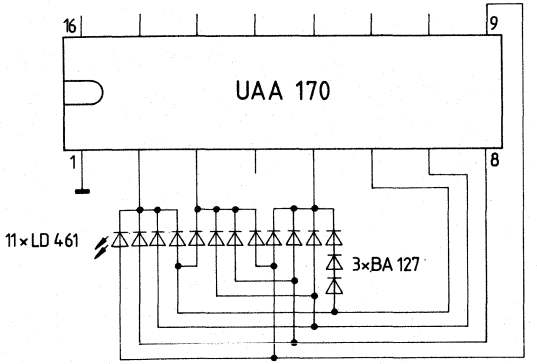


Operation of less than 16 LEDs

Control of 9 LEDs

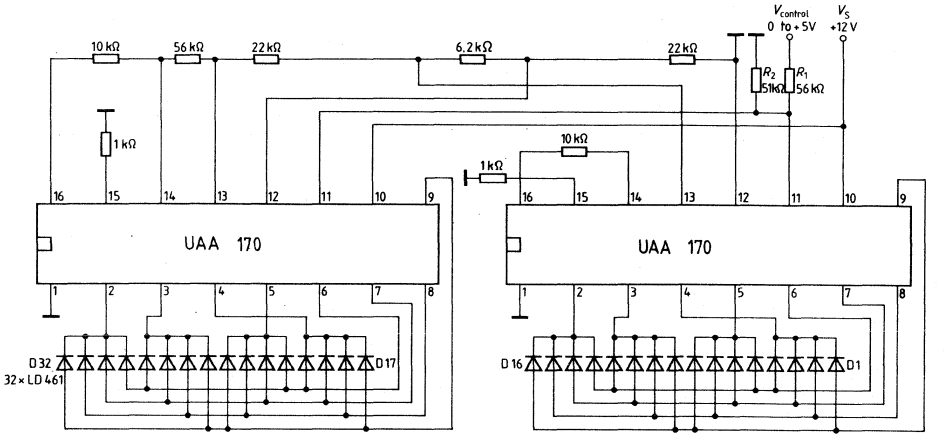


Control of 11 LEDs



Application circuit for the control of 30 LEDs with 2 x UAA 170

Range of control voltage $V_{control} = 0$ to 5 V
Voltage difference $V_{12/13} = 2 \times 1.2\ V = 2.4\ V$
Since the diodes D16 or D17 are permanently lit when the maximum or minimum voltages V_{13} or V_{12} adjusted by R_3, R_4, R_5, are exceeded or fall short the diodes should be covered, if necessary.



The figure shows an expansion of the circuit to 30 diodes with 2 ICs UAA 170. The diodes D16 or D17 light permanently, when the reciprocal absolute ratings are exceeded. They should be covered. The reference voltage $\Delta V_{12/13} = 2 \times 1.2\ V = 2.4\ V$ is derived from a stabilized dc voltage of typ. 5 V available at pin 14. A resistance of 6.2 kΩ provides an overlapping of the ranges in order to ensure a smooth transition from D15 to D18. The control voltage $V_{control}$ is forwarded in a parallel mode to pins 11 via a divider $R_1 : R_2$. The voltage divider is to be dimensioned according to the desired input voltage. With a divider current of $I = 100\ \mu A$ and a control voltage of $V_{control} = 10\ V$, the following is valid:

$$R_2 = \frac{\Delta V_{12/13}}{I} = \frac{2.4}{0.1} = 24\ k\Omega \text{ and}$$

$$R_1 = \frac{V_{control} - \Delta V_{12/13}}{I} = \frac{7.6}{0.1} = 76\ k\Omega$$

The nearest standard value is $R_1 = 75\ k\Omega$. The voltage difference for switching an incremental step is then $\Delta V_{control} = \frac{10\ V}{30} = 0.16\ V$.

Bipolar IC

Type	Ordering code	Package	Fig. No.
UAA 180	Q67000-A1104	DIP 18	11

Integrated circuit for driving 12 light emitting diodes. Corresponding to the input voltage the LEDs, forming a light band, are controlled similar to a thermometer scale.

By using an appropriate circuitry the brightness of the LEDs can be varied and the light passage between two adjacent LEDs can be arranged between "smooth" and "abrupt".

Maximum ratings

Supply voltage	V_S	18	V
Input voltage	V_3	6	V
	V_{16}	6	V
	V_{17}	6	V
Junction temperature	T_j	150	°C
Storage temperature range	T_{stg}	−40 to 125	°C
Thermal resistance (system-air)	$R_{th\,SA}$	78	K/W

Operating range

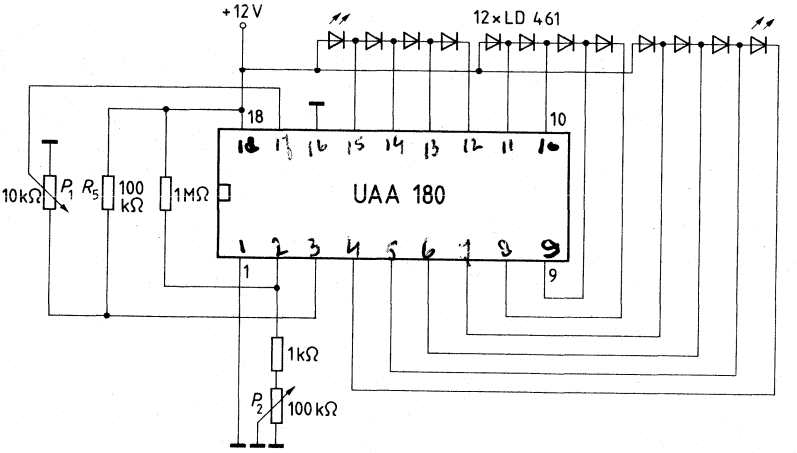
Supply voltage range	V_S	10 to 18	V
Ambient temperature range	T_{amb}	−25 to 85	°C

Characteristics

$V_S = 12$ V, $T_{amb} = 25$ °C

		min	typ	max	
Current consumption ($I_2 = 0$) (without LED current)	I_{18}		5.5	8.2	mA
Input currents ($V_3 - V_{16} < 2$ V)	I_3		0.3	1	µA
	I_{16}		0.3	1	µA
	I_{17}		0.3	1	µA
Voltage difference for smooth light transition	$V_{16/3}$	1.0			V
Voltage difference for abrupt light transition	$V_{16/3}$	4.0			V
Diode current per diode	I_D		10		mA
Tolerance of LED forward voltages	ΔV_D			1.0	V

Measurement circuit



P_1 light band test
P_2 brightness test

Scale display with light emitting diodes

Scale displays by means of a growing light band are particularly suitable for the measuring of approximate values. Applications of this kind are level sensors, VU meters, tachometers, field strength indicators etc. When applying the displays in measuring equipment, multi-colored LEDs can be used as range limitation.

The voltage difference between pins 16 and 3 thereby corresponds to the possible indication range. At the same time $\Delta V_{16/3}$ defines the light passage between two diodes. With $\Delta V_{16/3} \geq 1$ V, the light band glides smoothly along the scale. With increasing voltage difference, the passage becomes more abrupt. With $\Delta V_{16/3}$ approx. 4 V, the light band jumps from diode to diode.

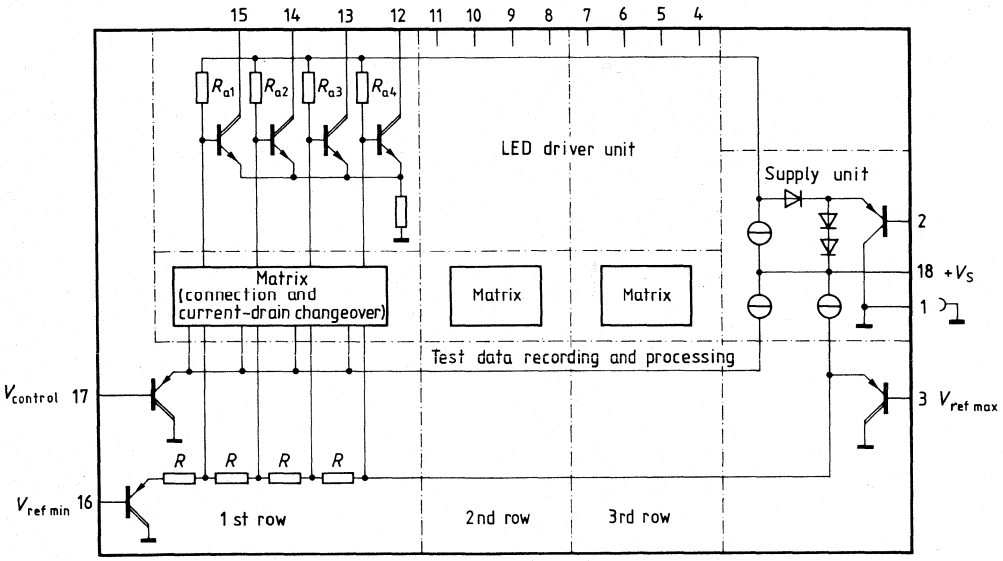
Each quartet must consist of identical diodes in order to maintain its functional characteristics.

It is therefore possible to design the first and third quartet as diodes emitting the color red and the second quartet as diodes emitting the color green to delineate a certain operational area.

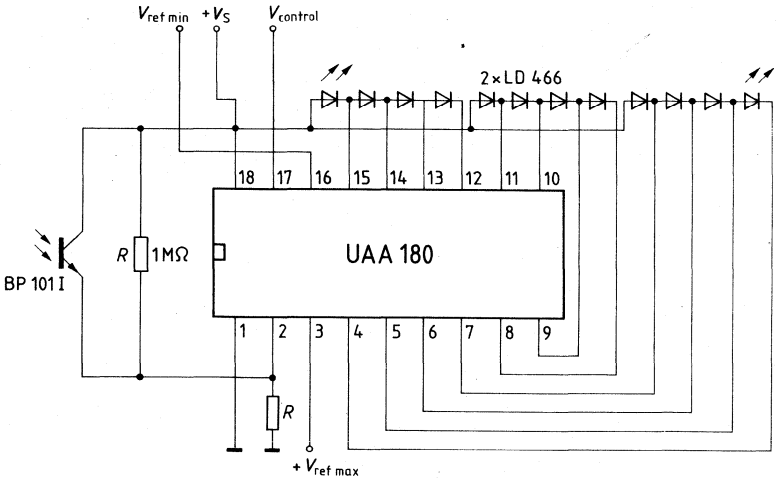
Pin 2 serves to determine the diode current. Corresponding to the desired light intensity, the forward current of the diodes is variably linear in the range I_f approx. 0 mA to 10 mA.

Application circuit 1 shows the possibility of designing this resistance, adjustable by means of a phototransistor BP 101, in order to adapt the light intensity to changing ambient brightness. The adjusting range of the diode current lies between I_f approx. 5 mA (BP 101 not lit) and I_f approx. 10 mA (BP 101 fully lit). If pin 2 is open the diode current is 10 mA.

Block diagram



Application circuit 1



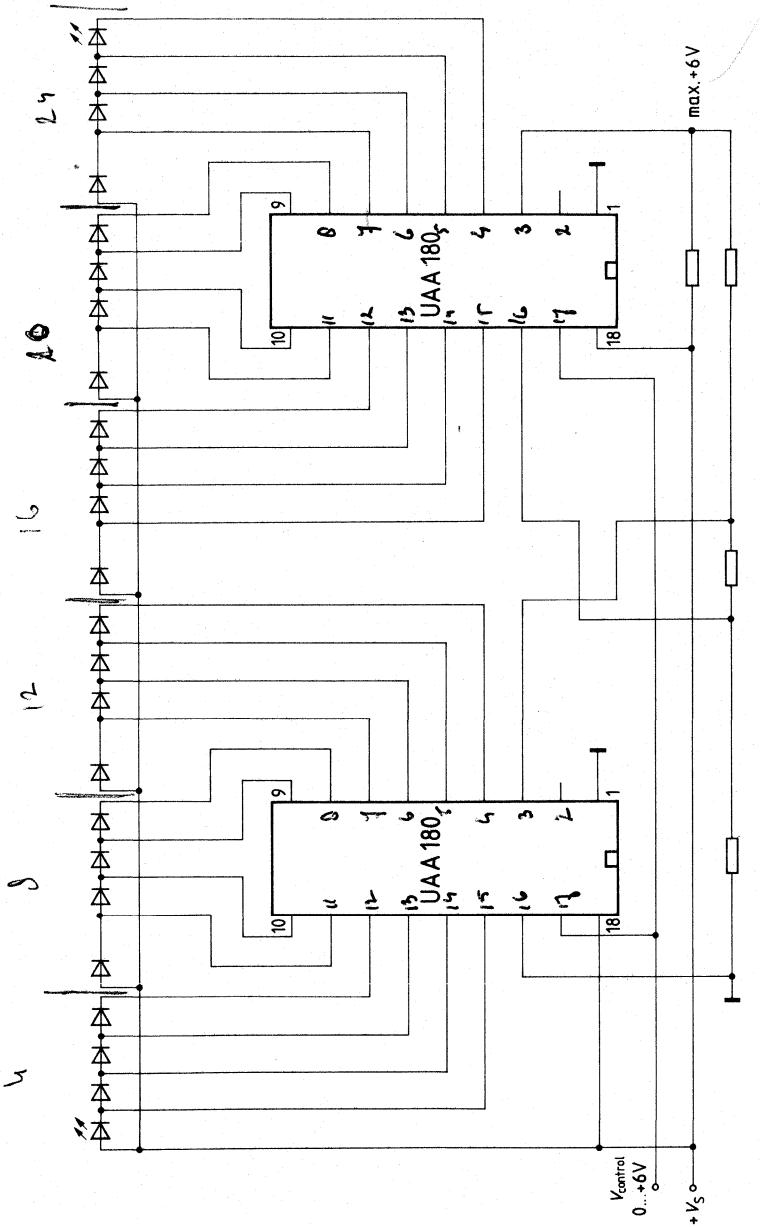
Depending on the actual maximum ratings, the resistances R_1 to R_7 can be varied widely as follows:

Proposal for smooth light transition:

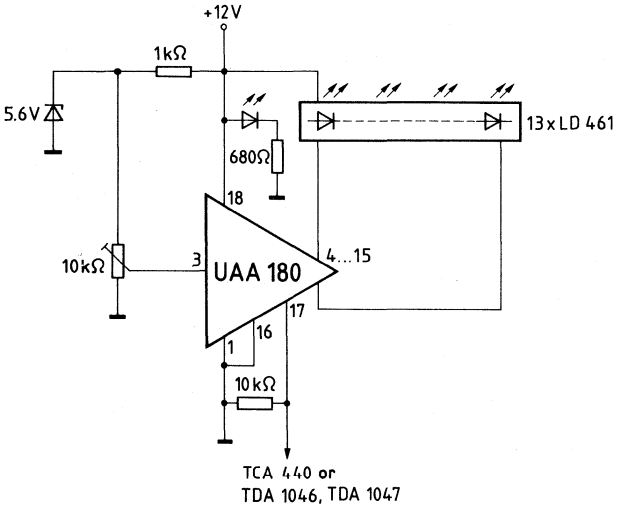
$R_3 = 820\ \Omega$
$R_4 = 56\ k\Omega$
$R_5 = 220\ k\Omega$
$R_6 = 2.2\ k\Omega \ldots 100\ k\Omega$

If a quartet does not need the full number of display diodes and if the first wired diodes shall be left luminous at full driving, bridges have to be inserted replacing the missing LEDs. Otherwise the first diodes of the quartet switch off when their display range is exceeded.

Application circuit 2
for cascading several UAA 180 ICs (up to 7)



Application circuit 3
for field strength indication



Bipolar IC

Type	Ordering code	Package	Fig. No.
SDA 2131	Q67000-A2044	DIP 22	13

The SDA 2131 includes a static display driver for 16 LEDs featuring a 10 mA output current, each. The serial data interface enables a simple connection to the microcomputer.

Features

- Integrated load resistances, thus few external components are required
- Number of LEDs software-selectable
- Blanking capability through DC-controlled input
- Simple connection to a microcomputer

Maximum ratings

Supply voltage range	V_{S7}	−0.3 to 7	V
Input voltage range	$V_{i4,5,6}$	−0.3 to 7	V
Output voltage range (outputs blocked) (pins 1 to 3, 9 to 16, 18 to 22)	V_{qH}	−0.3 to 7	V
Input voltage C range	V_{C8}	−0.3 to V_S	V
Junction temperature	T_j	150	°C
Storage temperature range	T_{stg}	−40 to 125	°C
Thermal resistance (system-air)	R_{thSA}	65	K/W

The anode voltage of the LEDs and the number of simultaneously active outputs should be selected so that a total power dissipation of 800 mW in the IC is not exceeded.

Operating range

Supply voltage range	V_{S7}	4.5 to 5.5	V
Ambient temperature range	T_{amb}	0 to 70	°C

Characteristics

$V_S = 5$ V; $T_{amb} = 25$ °C

		min.	typ.	max.	
Supply current (all LEDs ON) ($I_q = 10$ mA)	I_{S7}		10	15	mA
Quiescent current ($I_q = 0$; C = "L")	I_{S7}		2.5	3.5	mA
Switching voltage	$V_{S4,5,6}$	0.8	1.4	2.0	V
H input current ($V_H = 5.5$ V)	$I_{H4,5,6}$			1	µA
L input current ($V_L = 0.4$ V)	$-I_{L4,5,6}$			10	µA
Output current ($V_q = 2.9$ V) (pins 1 to 3, 9 to 16, 18 to 22)	I_q	8	10	12.5	mA
Output leakage current ($V_q = V_S$) (pins 1 to 3, 9 to 16, 18 to 22)	I_{ql}			10	µA
Switching voltage C	V_{S8}	1.5	2.1	2.7	V
H input current C ($V_{H8} = 5$ V)	I_{H8}		0.6	0.9	mA
L input current C ($V_{L8} = 0$ V)	$-I_{L8}$			1	µA
H input current C (at switching voltage)	I_{H8}			15	µA

Switching times

CLK (pin 5)	H pulse width	t_{HCLK}	1			µs
	L pulse width	t_{LCLK}	2			µs
	Set-up time	t_{SCLK}	0			µs
	Hold time	t_{hCLK}	0			µs
D (pin 4)	Set-up time	t_{SD}	0.5			µs
	Hold time	t_{hD}	0.5			µs
E (pin 6)	H pulse width	t_{HE}	50			µs
	L pulse width	t_{LE}	0.5			µs
	Set-up time	t_{SE}	1.5			µs
	Hold time	t_{hE}	1			µs
A	Delay time	t_A	10			µs

Circuit description

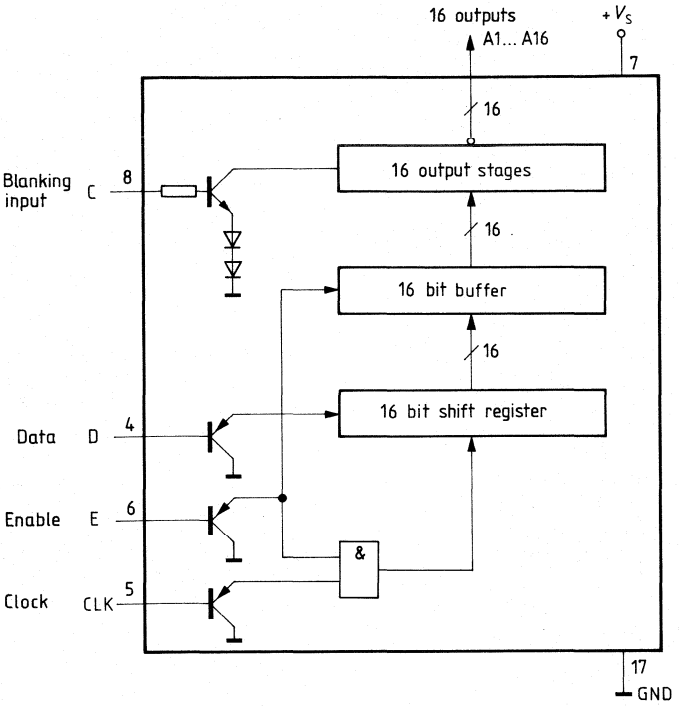
A serial interface consisting of data input D, enable input E, and clock input CLK, to connect the IC to a microprocessor. The 16 bit information ("H" at input D corresponds to the current flow at outputs A1 to A16) is loaded into a 16 bit shift register via the serial data input, beginning with LSB. Data transfer is initiated by the HL slope of the clock pulse at CLK. The data transfer D can take place only during the H state of the enable input E. A buffer accepts the data from the shift register during the HL slope of the enable input. The buffer directly drives the outputs A1 to A16.

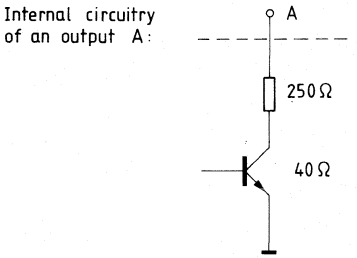
The output is limited by an internal resistor of 290 Ω.

Through input C the outputs can be switched off ($V_{C8} = 0$ V).

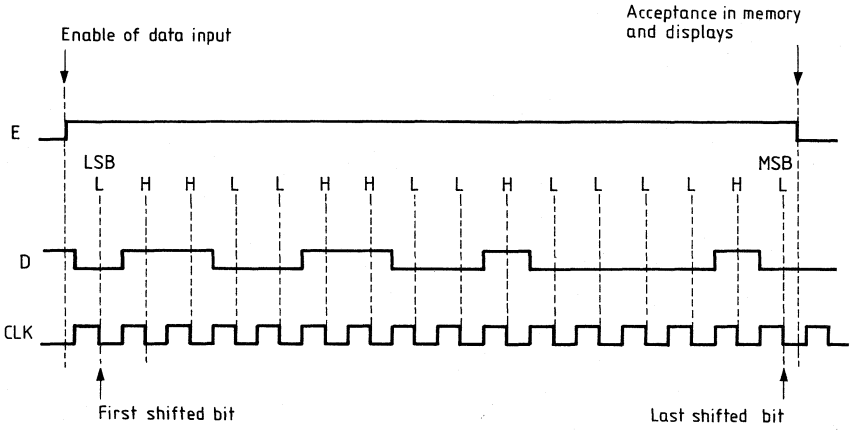
The inputs D, E, and CLK, and the input C are TTL-compatible.

Block diagram





Pulse diagram

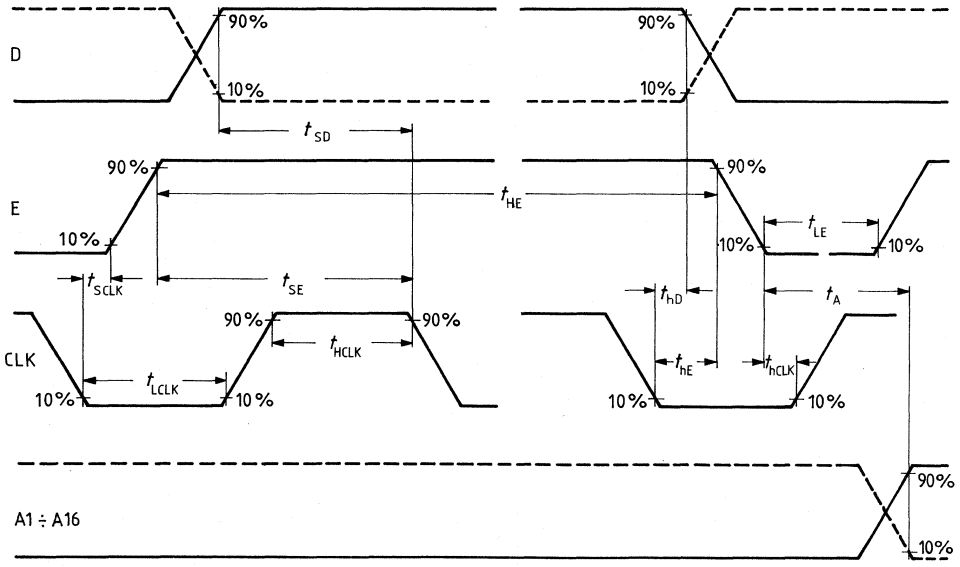


Memory contents after the falling edge of E

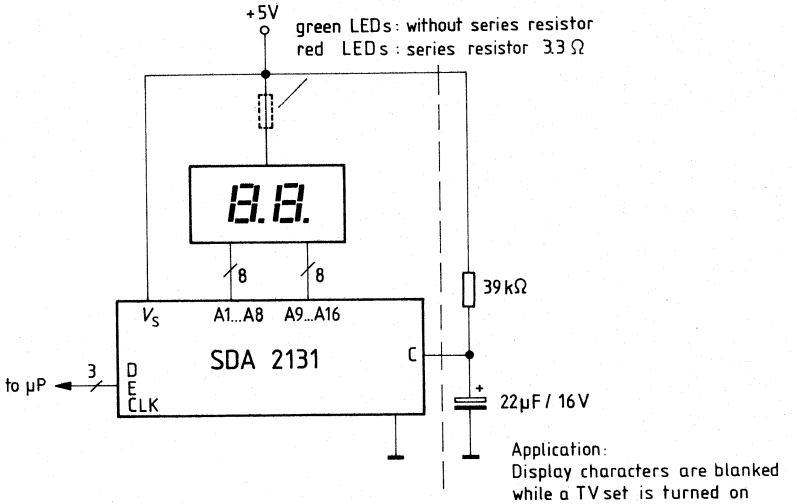
LSB MSB
L H H L L H H L L H L L L L H L

The first information shifted to D with CLK is displayed at A1.

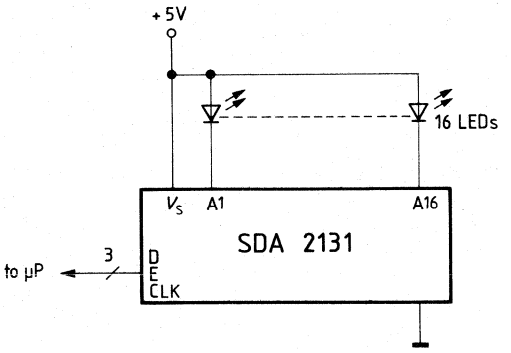
Pulse diagram



Application circuit 1
2 digit 7-segment display



Application circuit 2
Point display (1 of 16 diodes illuminated)



Pin configuration

Pin No.	Symbol	Function
1	A14	Output 14 for LED cathode
2	A15	Output 15 for LED cathode
3	A16	Output 16 for LED cathode
4	D	Input for data
5	CLK	Input for clock
6	E	Input for enable
7	V_S	Supply voltage
8	C	Input for blanking
9	A1	Output 1 for LED cathode
10	A2	Output 2 for LED cathode
11	A3	Output 3 for LED cathode
12	A4	Output 4 for LED cathode
13	A5	Output 5 for LED cathode
14	A6	Output 6 for LED cathode
15	A7	Output 7 for LED cathode
16	A8	Output 8 for LED cathode
17	GND	Ground
18	A9	Output 9 for LED cathode
19	A10	Output 10 for LED cathode
20	A11	Output 11 for LED cathode
21	A12	Output 12 for LED cathode
22	A13	Output 13 for LED cathode

Bipolar IC

Type	Ordering code	Package	Fig. No.
SDA 2014	Q 67000-Y 538	DIP 18	10

The SDA 2014 LED display driver enables cascade connection, decodes a serial BCD code and drives in multiplex operation 2 or 4 digits, as required. An output with serial data output permits cascade connections of the display drivers for more than 4 digits (6, 8, 10, etc.).

Features

- Serially read-in BCD code
- Enable input
- Any number of ICs permitted for cascade connection
- Optional 2- or 4-digit operation

Maximum ratings

Supply voltage	V_S	8.5	V
Supply current	I_S	400	mA
Input voltage (pins 7, 8, 9)	V_i	5.5	V
Output voltage (pin 10)	$V_{q\,H}$	8.5	V
H output current (pins 11, 12, 13, 15, 16, 17, 18)	$I_{q\,H}$	−60	mA
L output current (pins 2, 3, 4, 5)	$I_{q\,L}$	380	mA
Junction temperature	T_j	150	°C
Storage temperature range	T_{stg}	−65 to 150	°C
Thermal resistance (system-air)	$R_{th\,SA}$	80	K/W

Operating range

Supply voltage range	V_S	4.5 to 8	V
Ambient temperature range	T_{amb}	0 to 70	°C

Characteristics

$V_S = 5.0$ V, $T_{amb} = 25$ °C, unless otherwise specified

		min	typ	max	
Internal current consumption (without load) ($V_S = 8$ V)	I_S		20	31	mA
Current consumption ($V_S = 8$ V)	I_S			380	mA
Upper threshold voltage (pins 7, 8, 9)	V_{thu}		1.3		V
Lower threshold voltage (pins 7, 8, 9)	V_{thl}		0.7		V
Hysteresis (pins 7, 8, 9)			0.6		V
H output voltage (pins 11, 12, 13, 15, 16, 17, 18) ($V_S = 8$ V, $I_{qH} = -40$ mA)	V_{qH}			7.35	V
H output voltage (pins 11, 12, 13, 15, 16, 17, 18) ($V_S = 4.5$ V, $I_{qH} = -40$ mA)	V_{qH}	3.2			V
L output voltage (pins 2, 3, 4, 5) ($V_S = 4.5$ V, $I_{qL} = 280$ mA)	V_{qL}		0.6	0.8	V
H input current (pins 7, 8, 9) ($V_i = 5$ V)	I_{iH}			8	µA
L input current (pins 6, 7, 8, 9) ($V_S = 8$ V, $V_{iL} = 0.4$ V)	I_{iL}			−50	µA
H output current (pins 11, 12, 13, 15, 16, 17, 18) ($V_S = 8$ V)	I_{qH}			−48[1]	mA
H output current (pins 2, 3, 4, 5) ($V_S = 8$ V)	I_{qH}			50	µA
L output current (pins 2, 3, 4, 5) ($V_S = 8$ V)	I_{qL}			336	mA
H output voltage (pin 10) ($-I_{qH} = 200$ µA)	V_{qH}	V_S-2	$V_S-1.5$	V_S-1	V
L output voltage (pin 10) ($I_{qL} = 3$ mA, $V_S = 4.5$ V)	V_{qL}			0.4	V
Short-circuit output current (pin 10) ($V_S = 8$ V, max. duration: 1 sec)	I_q	−20		−50	mA

1) 48 mA = 12 mA integral value at 4 digit operation or 24 mA at 2 digit operation, respectively

Switching characteristics

		min	typ	max	
H pulse width (level = 2 V)	t_{WH8}	0.5	0.1		µs
L pulse width (level = 0.6 V)	t_{WL8}	3	1.5		µs
Hold time	t_{H8}	0.3	0		µs
Set-up time	t_{S9}	0	−0.4		µs
Hold time	t_{H9}	3	1.5		µs
Set-up time	t_{S7}	0	−0.3		µs
Hold time	t_{H7}	3			µs
L pulse width (level = 0.6 V)	t_{WL7}	3	1.6		µs
H pulse width (level = 2 V)	t_{WH7}	70	50		µs
H pulse width (pins 2, 3, 4, 5)	t_{WH}		4.5		ms
4-digit operation					
L pulse width (pins 2, 3, 4, 5)	t_{WL}		1.5		ms
4-digit operation					
Set-up time (pins 2, 3, 4, 5)	t_S	0		2	µs
H pulse width	$t_{WH2.3}$		3		ms
2-digit operation					
L pulse width	$t_{WL2.3}$		3		ms
2-digit operation					
Set-up time	$t_{S2.3}$	0		2	µs

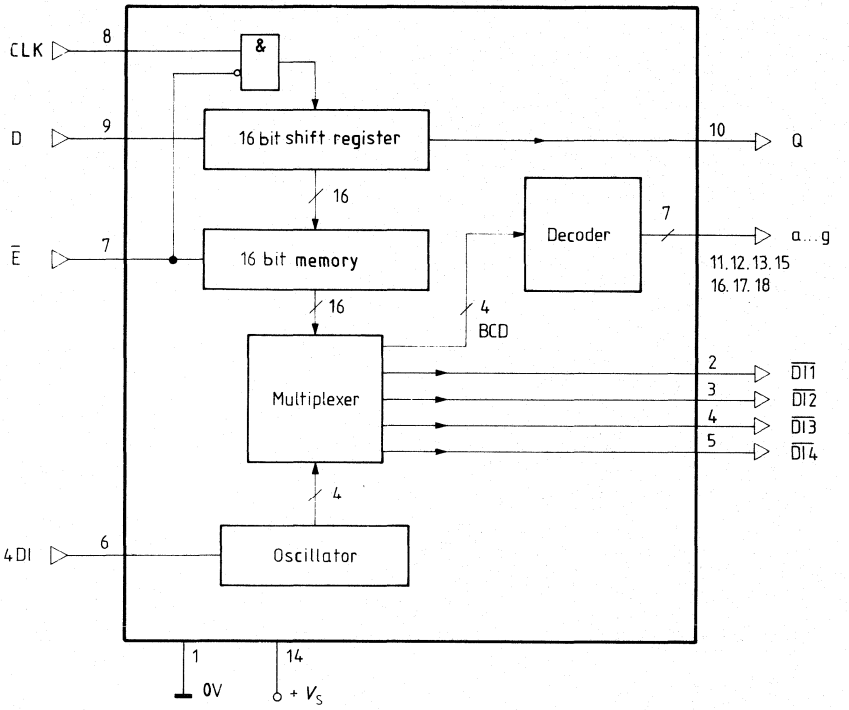
Truth table

Data D LSB...MSB[1]				Display	Segment driver (active H)						
					a	b	c	d	e	f	g
L	L	L	L	0	H	H	H	H	H	H	L
H	L	L	L	1	L	H	H	L	L	L	L
L	H	L	L	2	H	H	L	H	H	L	H
H	H	L	L	3	H	H	H	H	L	L	H
L	L	H	L	4	L	H	H	L	L	H	H
H	L	H	L	5	H	L	H	H	L	H	H
L	H	H	L	6	H	L	H	H	H	H	H
H	H	H	L	7	H	H	H	L	L	L	L
L	L	L	H	8	H	H	H	H	H	H	H
H	L	L	H	9	H	H	H	H	L	H	H
L	H	L	H	dark	L	L	L	L	L	L	L
H	H	L	H	dark	L	L	L	L	L	L	L
L	L	H	H	dark	L	L	L	L	L	L	L
H	L	H	H	dark	L	L	L	L	L	L	L
L	H	H	H	dark	L	L	L	L	L	L	L
H	H	H	H	dark	L	L	L	L	L	L	L

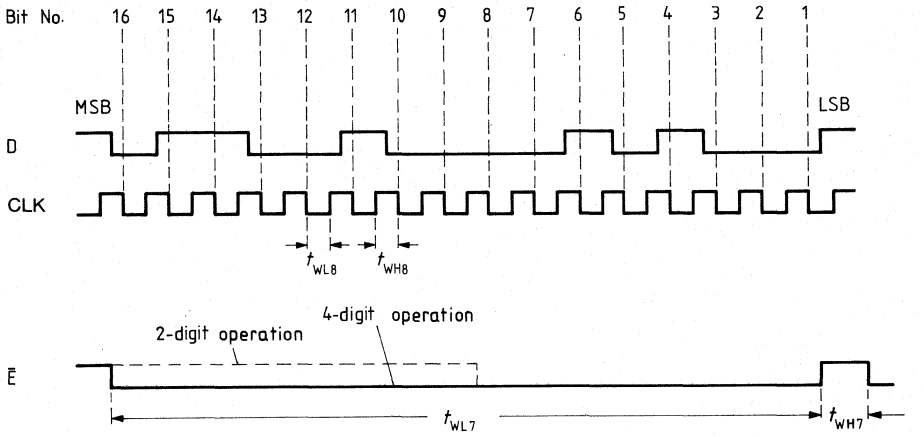
Segment designation

1) LSB = least significant bit
MSB = most significant bit

Block diagram



Pulse diagram



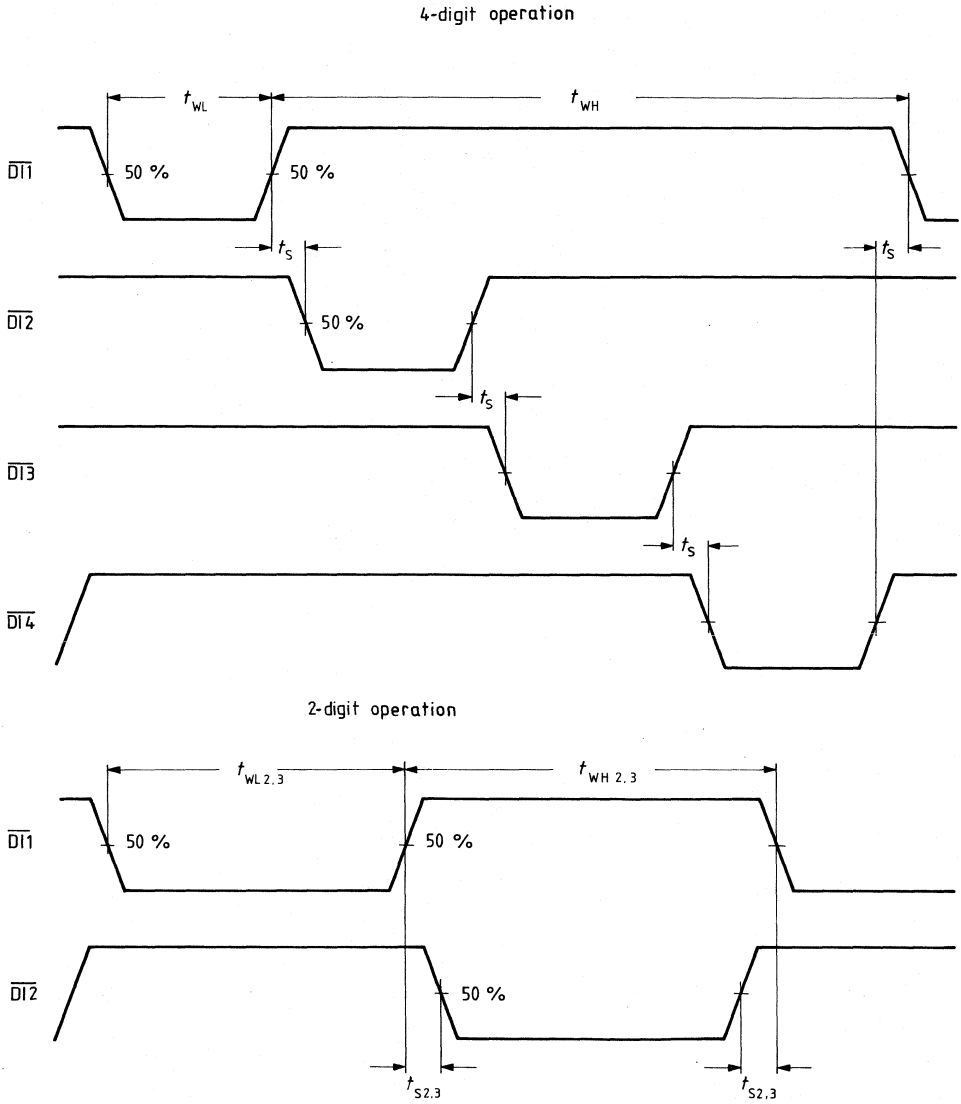
Memory contents after the rising edge of E: (4-digit operation)

	L	H	H	L	L	H	L	L	L	L	H	L	H	L	L	L
Display		6				4				2				8		
		Digit 4				Digit 3				Digit 2				Digit 1		

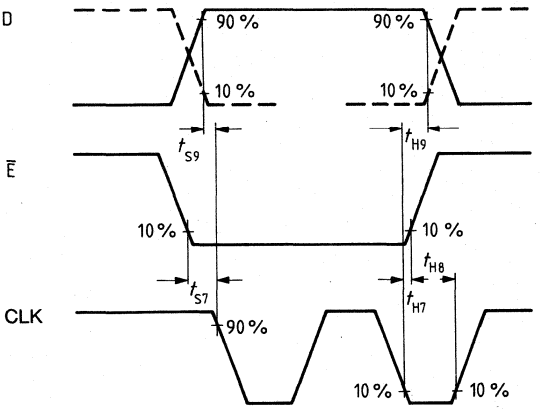
Memory contents and display at 2-digit operation

Remark: The information first shifted to D is displayed at digit 4; with digit 3, digit 2, and digit 1 following.
At every digit, MSB has to be shifted first.

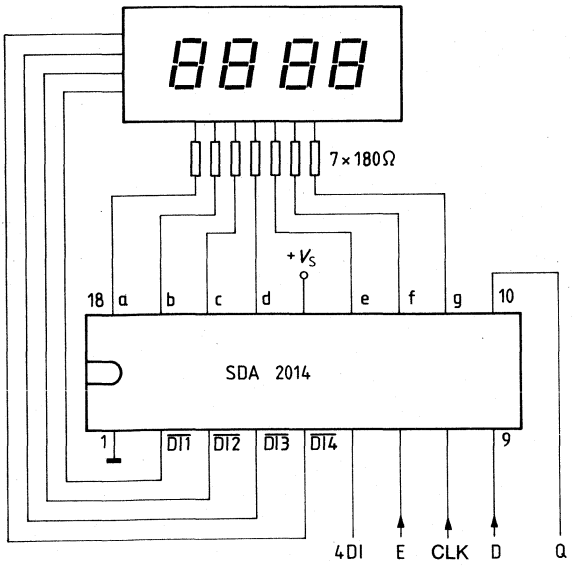
Timing diagram



Set-up and hold times



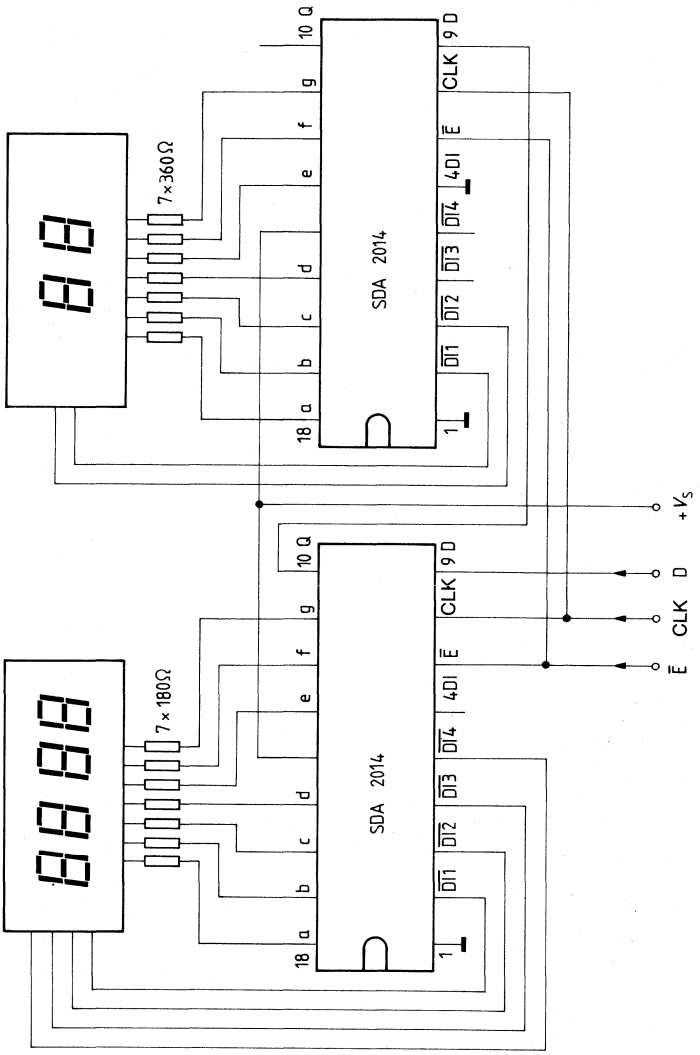
Application circuit 4-digit operation



At 2-digit operation ($\overline{DI1}$ and $\overline{DI12}$),4 DI is grounded

Application circuit

Example: Cascade connection to 6 digits



Transistor Array with 5 NPN Transistors

TCA 671; G
TCA 871; G
TCA 971
TCA 991

Bipolar IC

Type	Ordering code	Package	Fig. No.
TCA 671	Q67000-T1	DIP 14	7
TCA 671 G	Q67000-A2366	SO 14	27
TCA 871	Q67000-T2	DIP 14	7
TCA 871 G	Q67000-A2367	SO 14	27
TCA 971	Q67000-T11	DIP 14	7
TCA 991	Q67000-T12	DIP 14	7

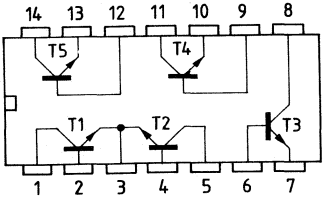
TCA 671, TCA 871, TCA 971, and TCA 991, are monolithic integrated transistor arrays each consisting of five NPN transistors. The arrays are well suited for switching and amplifying applications up to approx. 10 MHz. Due to a uniform design, the transistor characteristics show only slight deviations. The arrays are preferably intended for lamp drivers, amplifiers, pulse generators, and types TCA 971 and TCA 991 especially for discrete differential amplifiers.

Features

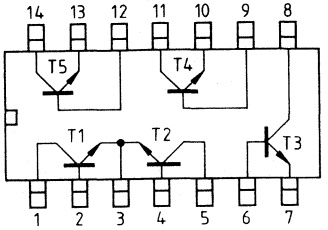
- Versatile use
- Slight V_{BE} and B deviation
- High output current
- Good thermal matching

Pin configuration

TCA 671, TCA 871 substrate = pin 3
TCA 971, TCA 991 substrate = pin 13
Substrate connection has to be on the most negative potential.



TCA 671 G, TCA 871 G



Maximum ratings

		TCA 671 TCA 971	TCA 871 TCA 991	
Collector-base breakdown voltage	V_{CB0}	45	35	V
Collector-emitter breakdown voltage	V_{CE0}	42	32	V
Emitter-base breakdown voltage	V_{EB0}	6	6	V
Collector-substrate voltage ($I_C = 100\ \mu A$)	V_{CS}	80	60	V
Collector current	I_C	200	200	mA
Base current	I_B	10	10	mA
Permissible power dissipation for a single transistor	P_{tot}	300	300	mW
Junction temperature	T_j	150	150	°C
Storage temperature range	T_{stg}	−40 to 125	−40 to 125	°C
Thermal resistance (system-air)	$R_{th\ SA}$	85	85	K/W
TCA 671 G, TCA 871 G	$R_{th\ SA}$	145	145	K/W

Operating range

Ambient temperature range	T_{amb}	−25 to 85	−25 to 85	°C

Characteristics

$T_{amb} = 25$ °C

		TCA 671 TCA 971			TCA 871 TCA 991			
		min	typ	max	min	typ	max	
Collector-base breakdown voltage at $I_C = 100\ \mu A$, $I_E = 0$	V_{CB0}	45			35			V
Collector-emitter breakdown voltage at $I_C = 100\ \mu A$, $I_B = 0$	V_{CE0}	42			32			V
Collector-substrate breakdown voltage at $I_C = 100\ \mu A$, $I_{CS} = 0$	V_{CS}	80			60			V
Emitter-base breakdown voltage at $I_E = 100\ \mu A$, $I_C = 0$	V_{EB0}	6			6			V
Collector-emitter saturation voltage at $I_C = 50$ mA, $I_B = 5$ mA	V_{CEsat}		200	350		200	350	mV
Collector-base cutoff current at $V_{CB} = 25$ V, $I_E = 0$	I_{CB0}		0.02	1		0.02	10	µA
Collector-emitter cutoff current at $V_{CE} = 25$ V, $I_B = 0$	I_{CE0}			10		1	100	µA
Static current gain	B							
at $V_{CE} = 3$ V, $I_C = 100\ \mu A$		40	80		40	80		
at $V_{CE} = 3$ V, $I_C = 1$ mA		100	140		100	140		
at $V_{CE} = 3$ V, $I_C = 10$ mA		100	160		100	160		
at $V_{CE} = 3$ V, $I_C = 100$ mA		40	100		40	100		

Characteristics

$T_{amb} = 25\,°C$

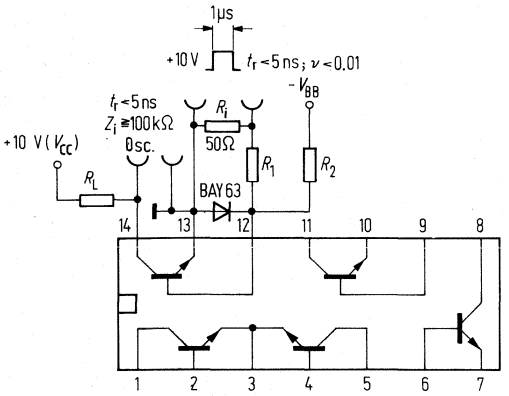
		TCA 671 TCA 971			TCA 871 TCA 991			
		min	typ	max	min	typ	max	
Differential base current for transistors T1 = T2 at $V_{CE} = 3$ V; $I_C = 1$ mA	I_{BD}		0.5	1		1		µA
Base-emitter voltage at $V_{CE} = 3$ V; $I_C = 1$ mA	V_{BE}		0.65			0.65		V
Differential base-emitter voltage for transistors T1 + T2 at $V_{CE} = 3$ V; $I_C = 1$ mA	V_{BED}		2	5		4		mV
Differential base-emitter voltage for transistors T3 to T5 at $V_{CE} = 3$ V; $I_C = 1$ mA	V_{BED}		4	10		6		mV
Temperature coefficient of base-emitter voltage at $V_{CE} = 3$ V; $I_C = 1$ mA	$\frac{\Delta V_{BE}}{\Delta T}$		−2			−2		mV/K
Transition frequency	f_T	300	550		300	550		MHz

Switching times

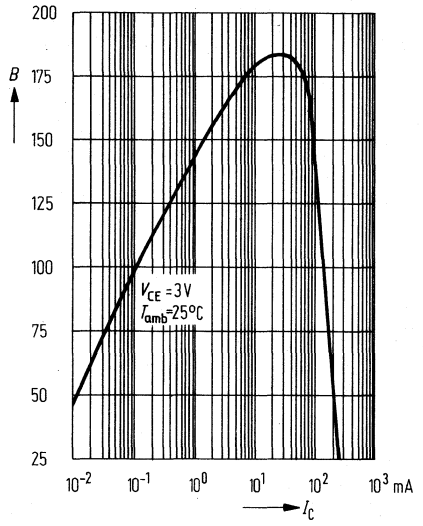
I_C: I_{B1}: $-I_{B2} \approx 10 : 1 : 1$ mA; $R_1 = 5$ kΩ; $R_2 = 5$ kΩ; $V_{BB} = 3.5$ V; $R_L = 990$ Ω
t_{on} 85 (< 150) ns t_{off} 480 (< 800) ns

I_C: I_{B1}: $-I_{B2} \approx 100 : 10 : 10$ mA; $R_1 = 500$ Ω; $R_2 = 700$ Ω; $V_{BB} = 5$ V; $R_L = 98$ Ω
t_{on} 55 (< 150) ns t_{off} 450 (< 800) ns

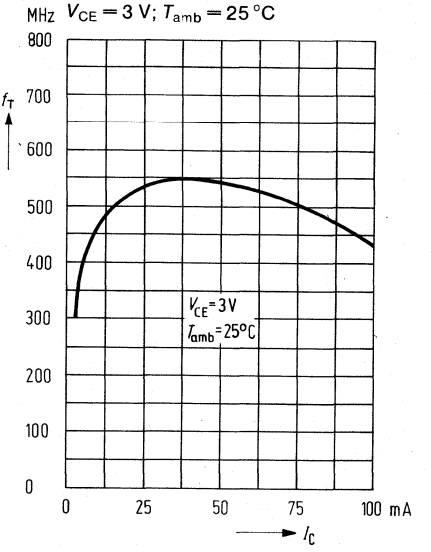
Test circuit for switching times



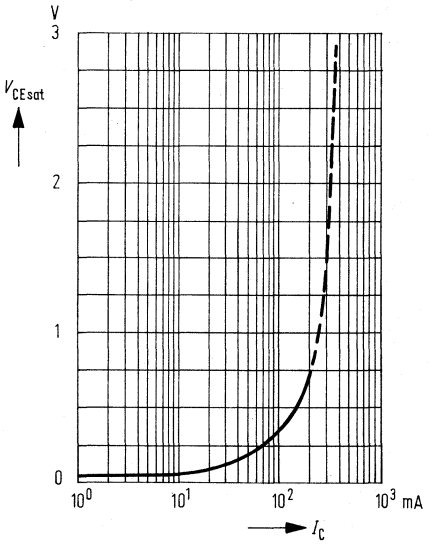
Current gain versus collector current
$V_{CE} = 3$ V; $T_{amb} = 25$ °C



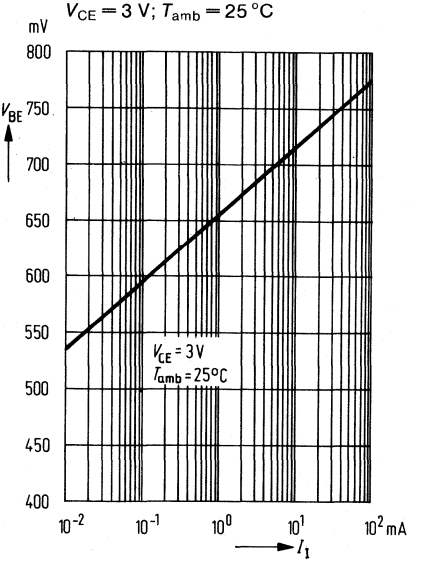
Transition frequency versus collector current
$V_{CE} = 3$ V; $T_{amb} = 25$ °C



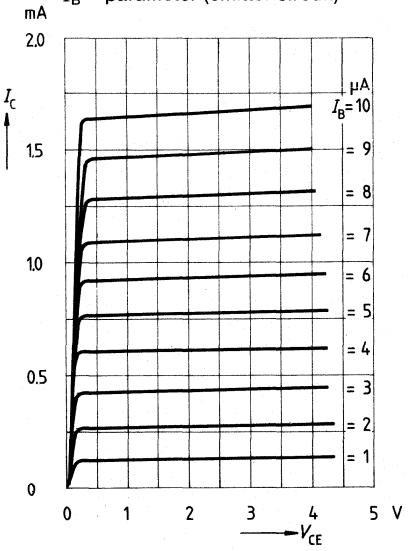
Collector-emitter saturation voltage versus collector current
$B = 20$



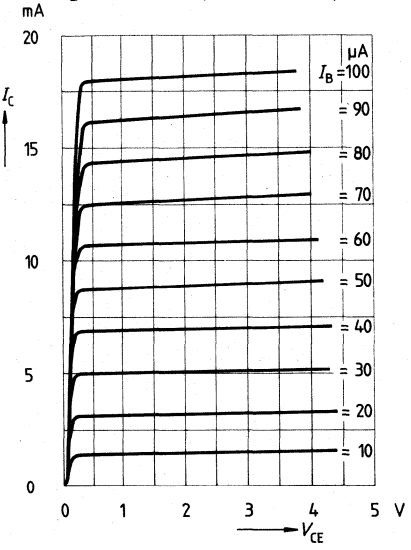
Base-emitter voltage versus input current
$V_{CE} = 3$ V; $T_{amb} = 25$ °C



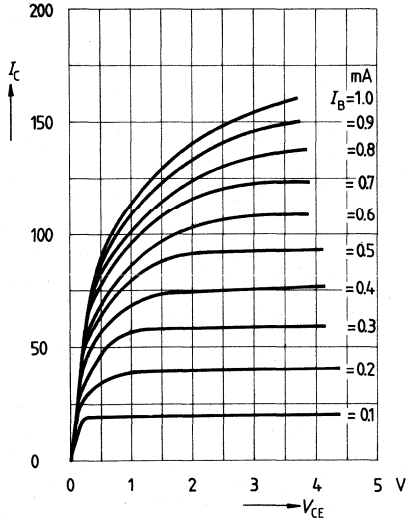
Output characteristics
Collector current versus
collector-emitter voltage
I_B = parameter (emitter circuit)



Output characteristics
Collector current versus
collector-emitter voltage
I_B = parameter (emitter circuit)



Output characteristics
Collector current versus
collector-emitter voltage
mA I_B = parameter (emitter circuit)



Control ICs for Thyristors and Triacs

Preliminary data **Bipolar IC**

Type	Ordering code	Package	Fig. No.
TCA 785	Q67000-A2321	DIP 16	8

This phase control IC is intended to control thyristors, triacs, and transistors. The trigger pulses can be shifted within a phase angle between 0° and 180°. Typical applications include converter circuits, AC controllers and three-phase current controllers.

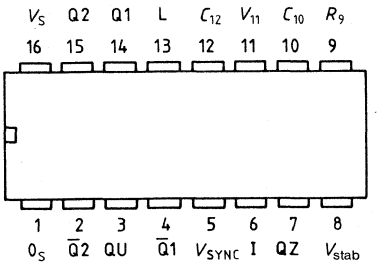
This IC replaces the previous types TCA 780 and TCA 780 D

Features

- Reliable recognition of zero passage
- Large application scope
- May be used as zero point switch
- LSL compatible
- Three-phase operation possible (3 ICs)
- Output current 250 mA
- Large ramp current range
- Large temperature range

Pin configuration

top view



Pin No.	Symbol	Function
1	0_S	Ground
2	$\overline{Q2}$	Output 2 inverted
3	QU	Output U
4	$\overline{Q1}$	Output 1 inverted
5	V_{SYNC}	Synchronous voltage
6	I	Inhibit
7	QZ	Output Z
8	V_{stab}	Reference voltage
9	R_9	Ramp resistance
10	C_{10}	Ramp capacitance
11	V_{11}	Control voltage
12	C_{12}	Pulse extension
13	L	Long pulse
14	Q1	Output 1
15	Q2	Output 2
16	V_S	Supply voltage

Functional description

The synchronization signal is obtained via a high-ohmic resistance from the line voltage (voltage V_5). A zero voltage detector evaluates the zero passages and transfers them to the synchronization register.

This synchronization register controls a ramp generator the capacitor C_{10} of which is charged by a constant current (determined by R_9). If the ramp voltage V_{10} exceeds the control voltage V_{11} (triggering angle φ), a signal is processed to the logic. Dependent on the magnitude of the control voltage V_{11}, the triggering angle φ can be shifted within a phase angle of 0° to 180°.

For every half wave, a positive pulse of approx. 30 µs duration appears at the outputs Q1 and Q2. The pulse duration can be prolonged up to 180° via a capacitor C_{12}. If pin 12 is connected to ground, pulses with a duration between φ and 180° will result.

Outputs $\overline{Q}1$ and $\overline{Q}2$ supply the inverse signals of Q1 and Q2.

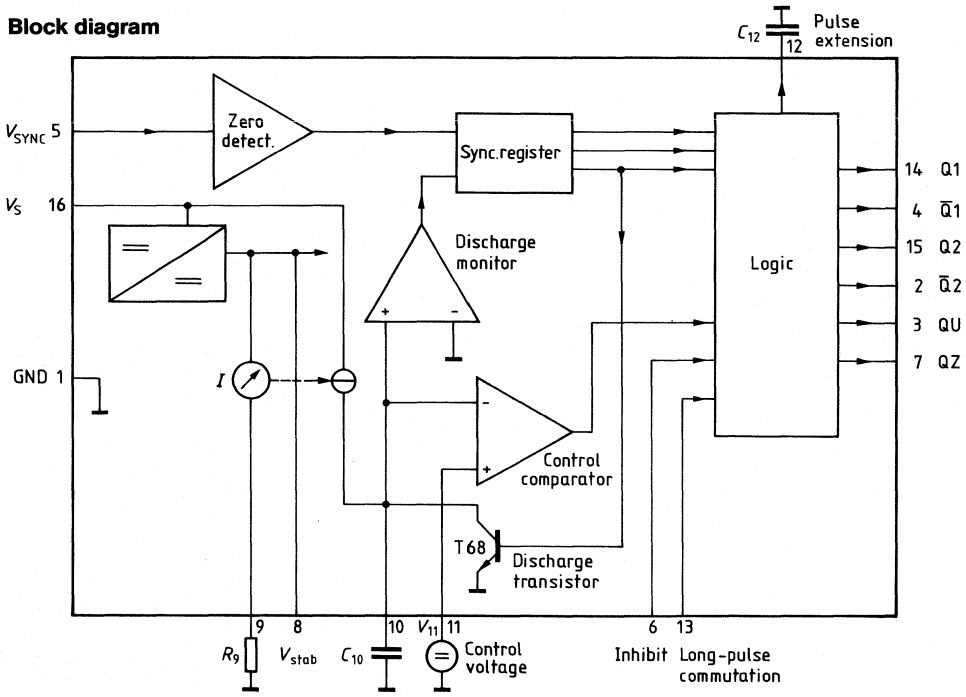
A signal of $\varphi + 180°$ which can be used for controlling an external logic, is available at pin 3.

A signal which corresponds to the NOR link of Q1 and Q2 is available at output QZ (pin 7).

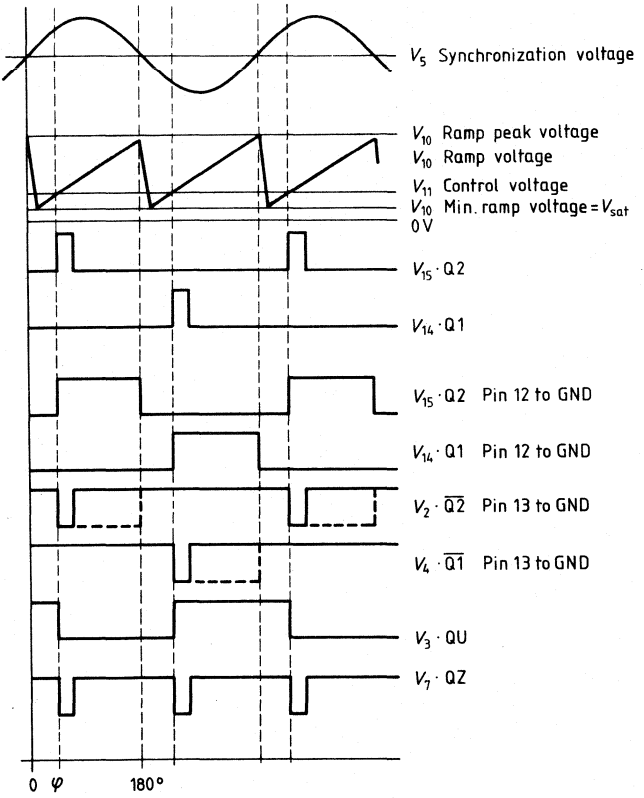
The inhibit input can be used to disable outputs Q1, Q2, $\overline{Q}1$, $\overline{Q}2$, QU.

Pin 13 can be used to extend the outputs $\overline{Q}1$ and $\overline{Q}2$ to full pulse length (180° – φ).

Block diagram



Pulse diagram



Maximum ratings

		Lower limit B	Upper limit A	
Supply voltage	V_S	−0.5	18	V
Output current at pin 14, 15	I_Q	−10	400	mA
Inhibit voltage	V_6	−0.5	V_S	V
Control voltage	V_{11}	−0.5	V_S	V
Voltage short-pulse circuit	V_{13}	−0.5	V_S	V
Synchronization input current	I_5	−200	± 200	µA
Output voltage at pin 14, 15	V_Q		V_S	V
Output current at pin 2, 3, 4, 7	I_Q		10	mA
Output voltage at pin 2, 3, 4, 7	V_Q		V_S	V
Junction temperature	T_j		125	°C
Storage temperature	T_{stg}	−55	125	°C
Thermal resistance (system-air)	$R_{th\,SA}$		80	K/W

Operating range

Supply voltage	V_S	8	18	V
Operating frequency	f	10	500	Hz
Ambient temperature range	T_{amb}	−25	85	°C

Characteristics
$8 \leq V_S \leq 18$ V; $-25\,°C \leq T_{amb} \leq 85\,°C$; $f = 50$ Hz

		Test circuit No.	Lower limit B	$f = 50$ Hz $V_S = 15$ V typ	Upper limit A	
Supply current consumption S 1...S 6 open $V_{11} = 0$ V $C_{10} = 47$ nF; $R_9 = 100$ kΩ	I_S	1	4.5	6.5	10	mA
Synchronization pin 5 Input current R_2 varied	$I_{5\,rms}$	1	30		200	µA
Offset voltage	ΔV_5	4		30	75	mV
Control input pin 11 Control voltage range Input resistance	V_{11} R_{11}	1 5	0.2	15	$V_{10\,peak}$	V kΩ
Ramp generator Load current	I_{10}		10		1000	µA
Max. ramp voltage	V_{10}	1			V_S-2	V
Saturation volt. at capacitor	V_{10}	1.6	100	225	350	mV
Ramp resistance	R_9	1	3		300	kΩ
Sawtooth return time	t_f	1		80		µs
Inhibit pin 6 switch-over of pin 7						
Outputs disabled	V_{6L}	1		3.3	2.5	V
Outputs enabled	V_{6H}	1	4	3.3		V
Signal transition time	t_r	1	1		5	µs
Input current $V_6 = 8$ V	I_{6H}	1		500	800	µA
Input current $V_6 = 1.7$ V	$-I_{6L}$	1	80	150	200	µA
Deviation of I_{10} $R_9 =$ const. $V_S = 12$ V; $C_{10} = 47$ nF	I_{10}	1	−5		5	%
Deviation of I_{10} $R_9 =$ const. $V_S = 8$ to 18 V	I_{10}	1	−20		20	%
Deviation of the ramp voltage between 2 following half-waves, $V_S =$ const.	$\Delta V_{10\,max}$			± 1		%

Characteristics

$8 \leq V_S \leq 18$ V; $-25\,°C \leq T_{amb} \leq 85\,°C$; $f = 50$ Hz

		Test circuit No.	Lower limit B	$f = 50$ Hz $V_S = 15$ V typ	Upper limit A	
Long pulse switch-over pin 13 switch-over of S 8						
Short pulse at output	$V_{13\,H}$	1	3.5	2.5		V
Long pulse at output	$V_{13\,L}$	1		2.5	2	V
Input current $V_{13} = 8$ V	$I_{13\,H}$	1			10	µA
Input current $V_{13} = 1.7$ V	$-I_{13\,L}$	1	45	65	100	µA
Outputs pin 2, 3, 4, 7						
Reverse current $V_Q = V_S$	I_{CE0}	2.6			10	µA
Saturation voltage $I_Q = 2$ mA	V_{sat}	2.6	0.1	0.4	2	V
Outputs pin 14, 15						
H output voltage $-I_Q = 250$ mA	$V_{14/15\,H}$	3.6	V_S–3	V_S–2.5	V_S–1.0	V
L output voltage $I_Q = 2$ mA	$V_{14/15\,L}$	2.6	0.3	0.8	2	V
Pulse width (short pulse) S 9 open	t_p	1	20	30	40	µs
Pulse width (short pulse) with C_{12}	t_p	1	530	620	760	µs/nF
Internal voltage control						
Reference voltage Parallel connection of 10 ICs possible	V_{ref}	1	2.8	3.1	3.4	V
TC of reference voltage	α_{ref}	1		2×10^{-4}	5×10^{-4}	1/K

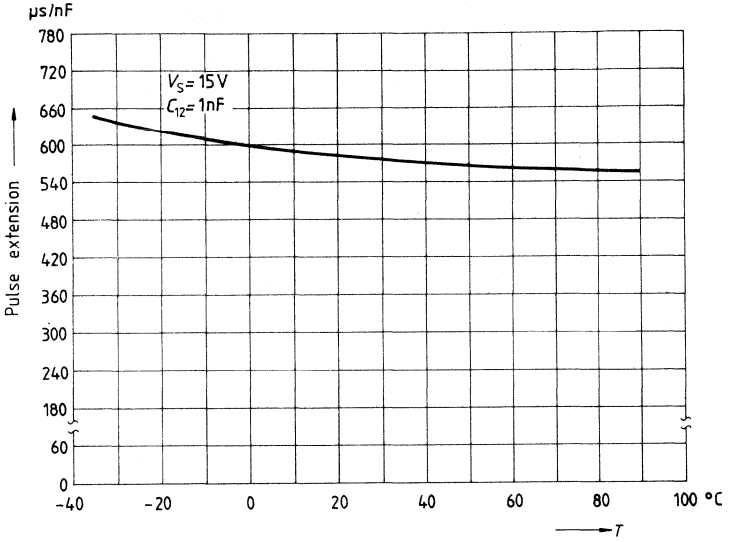
Application hints for external components

		min	max	
Ramp capacitance	C_{10}	500 pF	1 µF[1]	The minimum and maximum values of I_{10} are to be observed
Triggering point	$t_{Tr} = \frac{V_{11} \times R_9 \times C_{10}}{V_{ref} \times K}$		[2]	
Charging current	$I_{10} = \frac{V_{ref} \times K}{R_9}$		[2]	Ramp voltage $V_{10\,max} = V_S - 2$ V $V_{10} = \frac{V_{ref} \times K \times t}{R_9 \times C_{10}}$ [2]

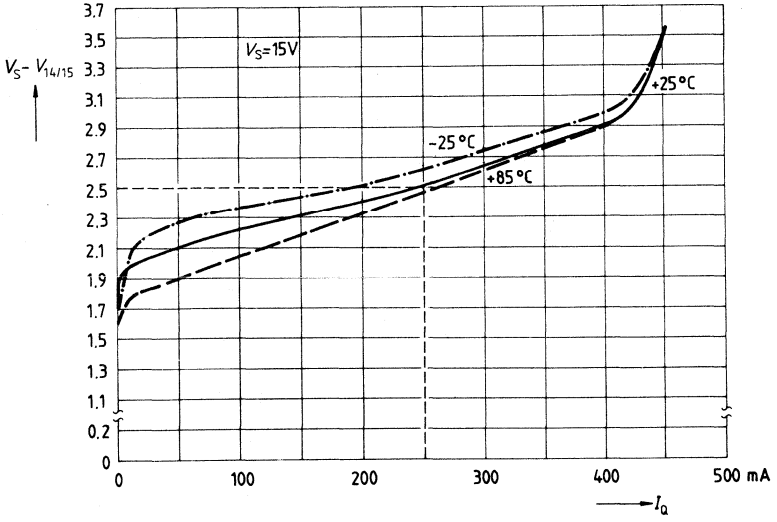
1) Attenuation to flyback times

2) $K = 1.10 \pm 20\%$

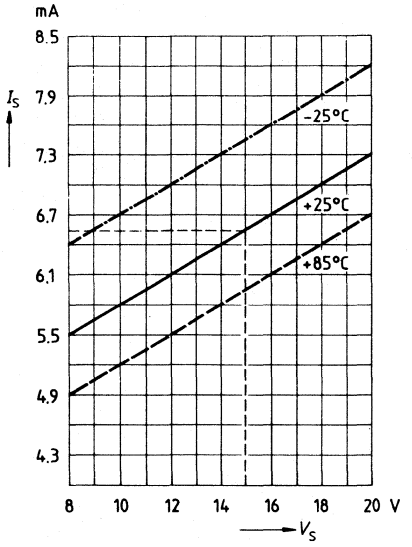
Pulse extension versus temperature



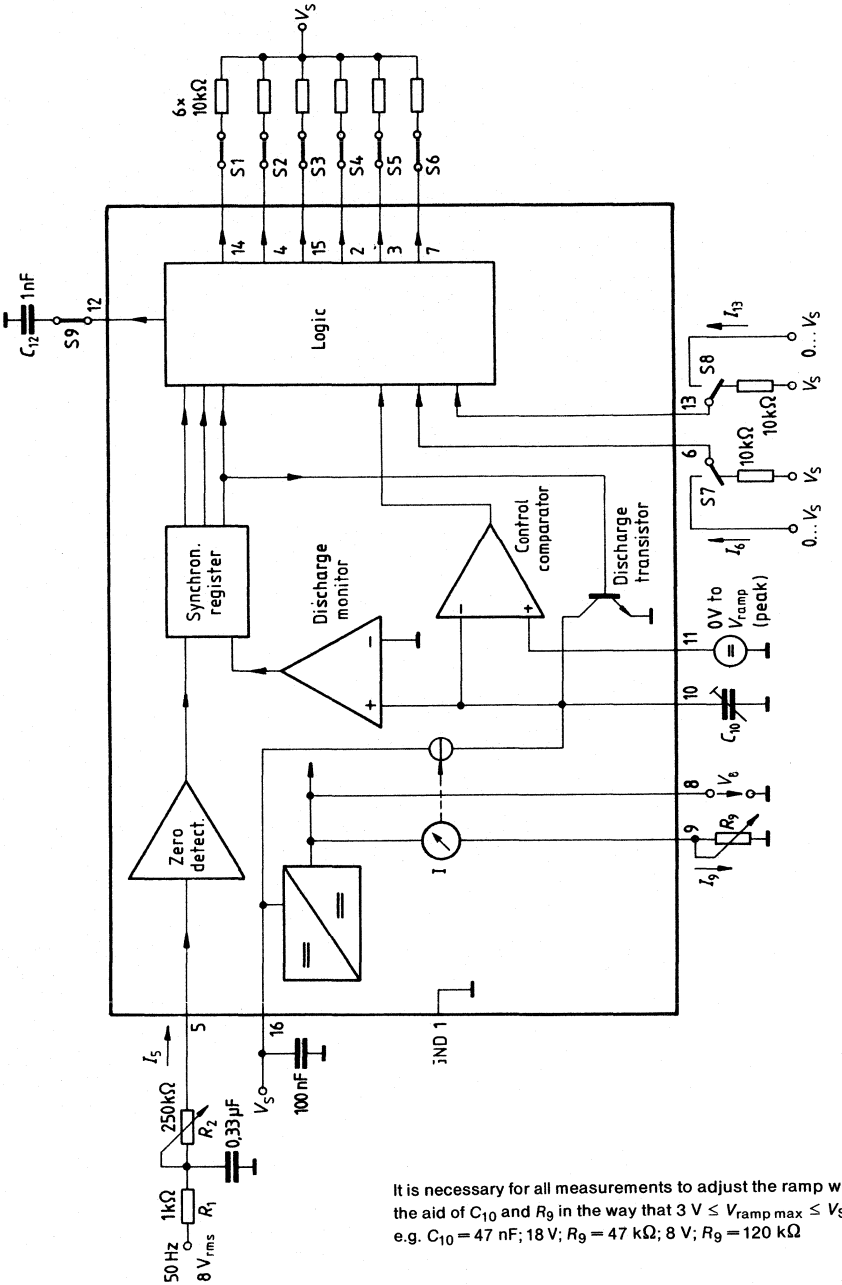
Output voltage measured to + V_S



Supply current versus supply voltage



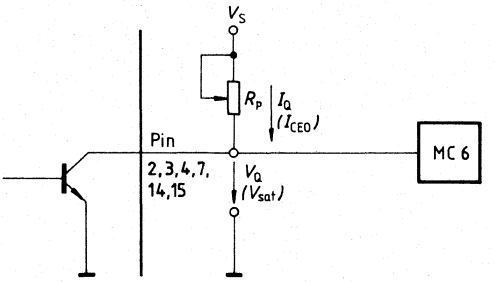
Test and measurement circuit 1



It is necessary for all measurements to adjust the ramp with the aid of C_{10} and R_9 in the way that $3\ V \leq V_{ramp\ max} \leq V_S - 2\ V$
e.g. $C_{10} = 47$ nF; 18 V; $R_9 = 47$ kΩ; 8 V; $R_9 = 120$ kΩ

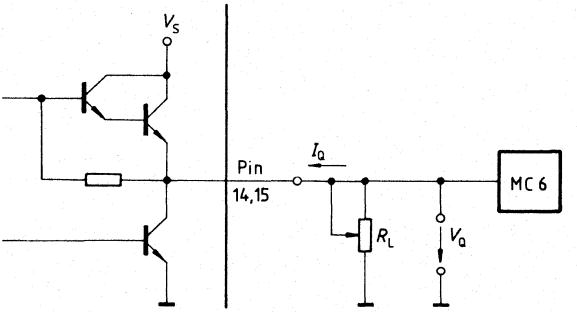
Test and measurement circuits

Measurement circuit 2



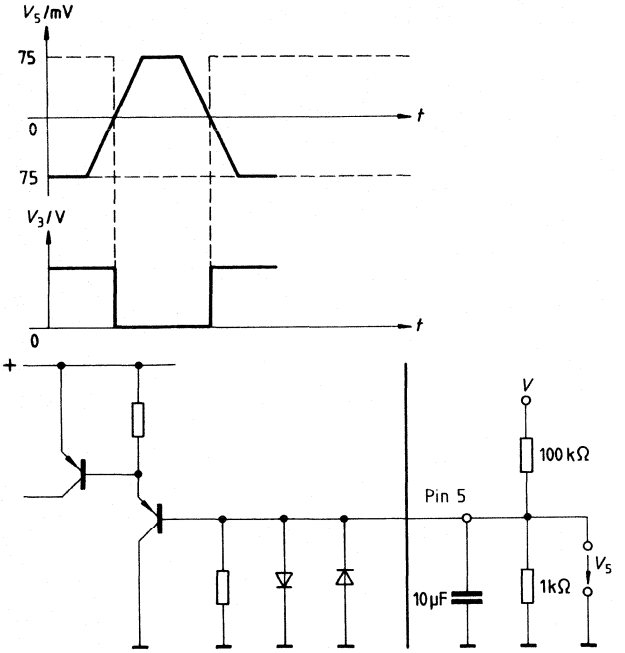
The residual pins are connected as in measurement circuit 1

Measurement circuit 3



The residual pins are connected as in measurement circuit 1

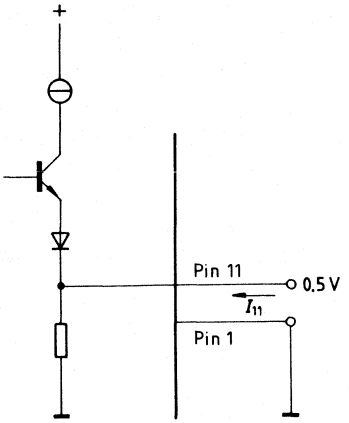
Measurement circuit 4



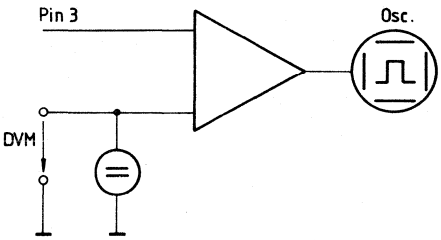
Residual pins are connected as in measurement circuit 1

The 10 µF capacitor at pin 5 serves only for test purposes

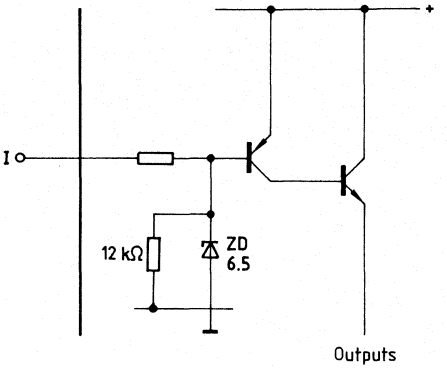
Measurement circuit 5



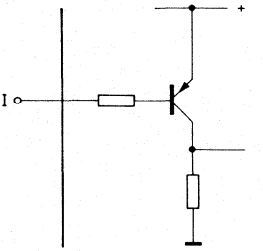
Measurement circuit 6



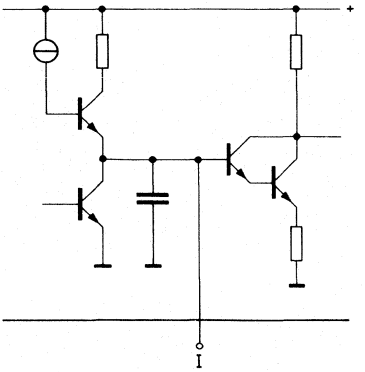
Inhibit 6



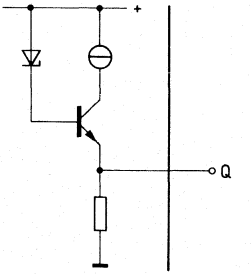
Long pulse 13



Pulse extension 12



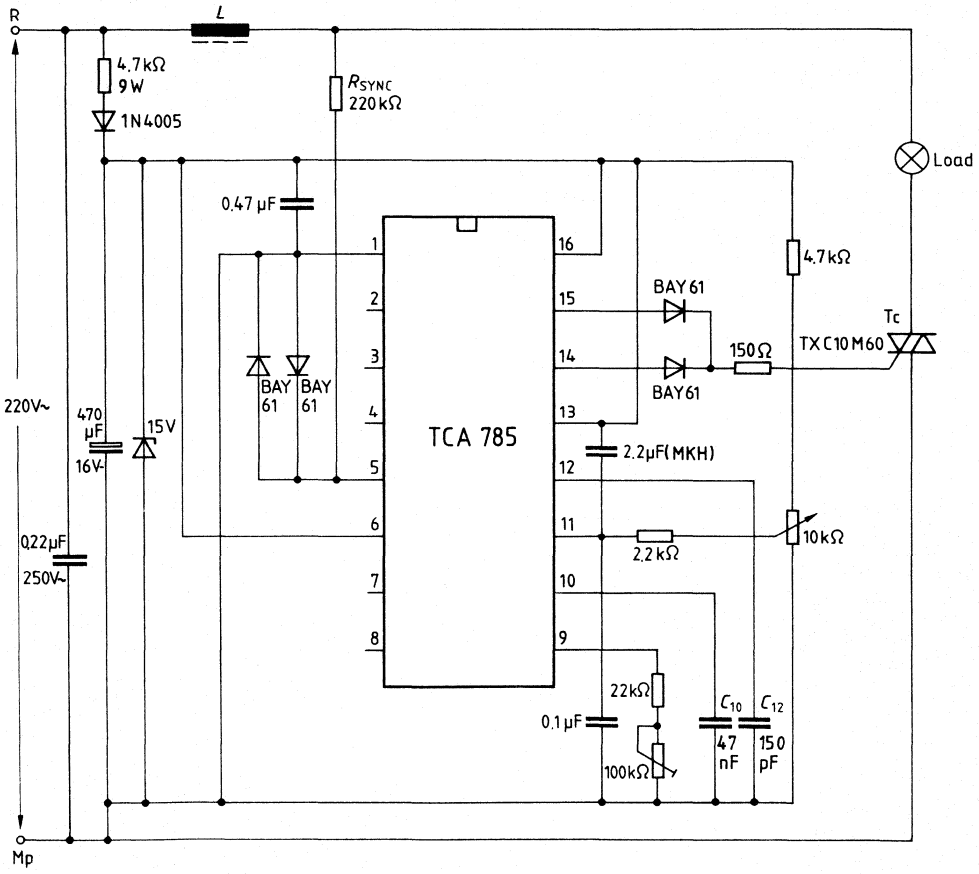
Reference voltage 8



Additional circuit description

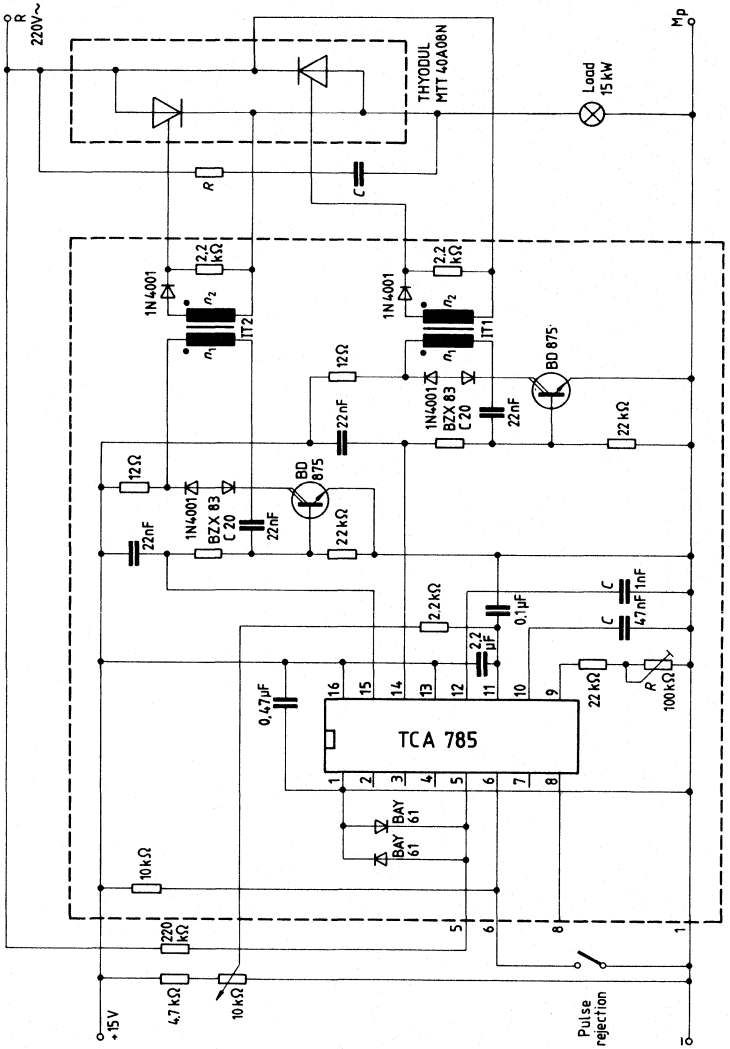
Application examples

Triac control for up to 50 mA gate trigger current



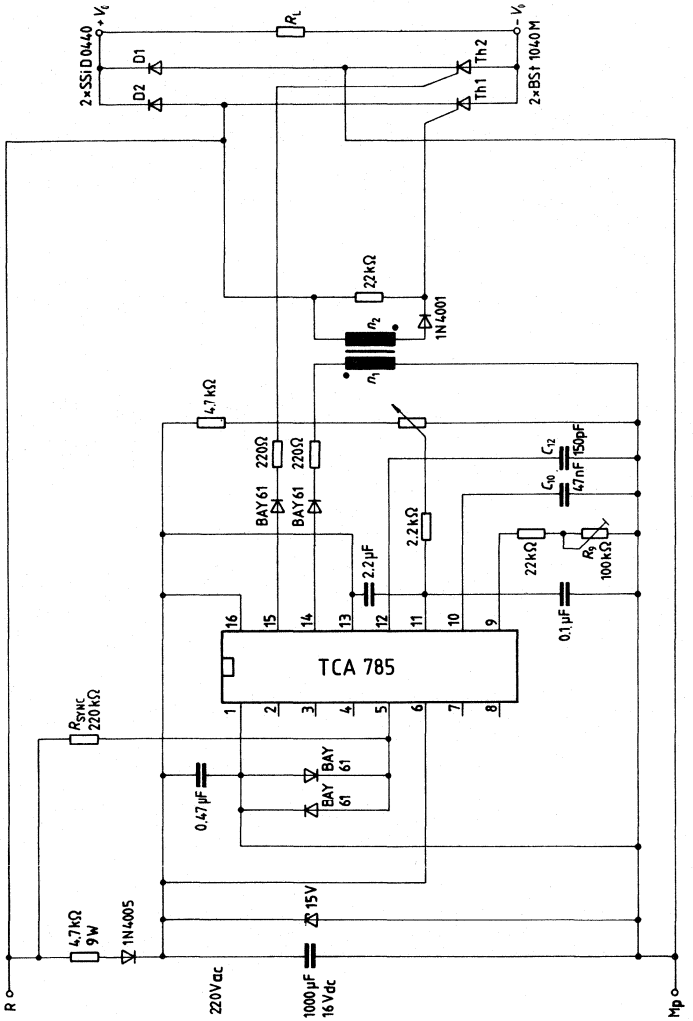
A phase control with a diretly controlled triac is shown in the figure. The triggering angle of the triac can be adjusted continuously between 0° and 180° with the aid of an external potentiometer. During the positive half wave of the line voltage, the triac receives a positive gate pulse from the IC output pin 15. During the negative half wave, it receives also a positive trigger pulse from pin 14. Trigger pulse width is approx. 100 µs.

Fully controlled AC power controller
Circuit for two high-power thyristors

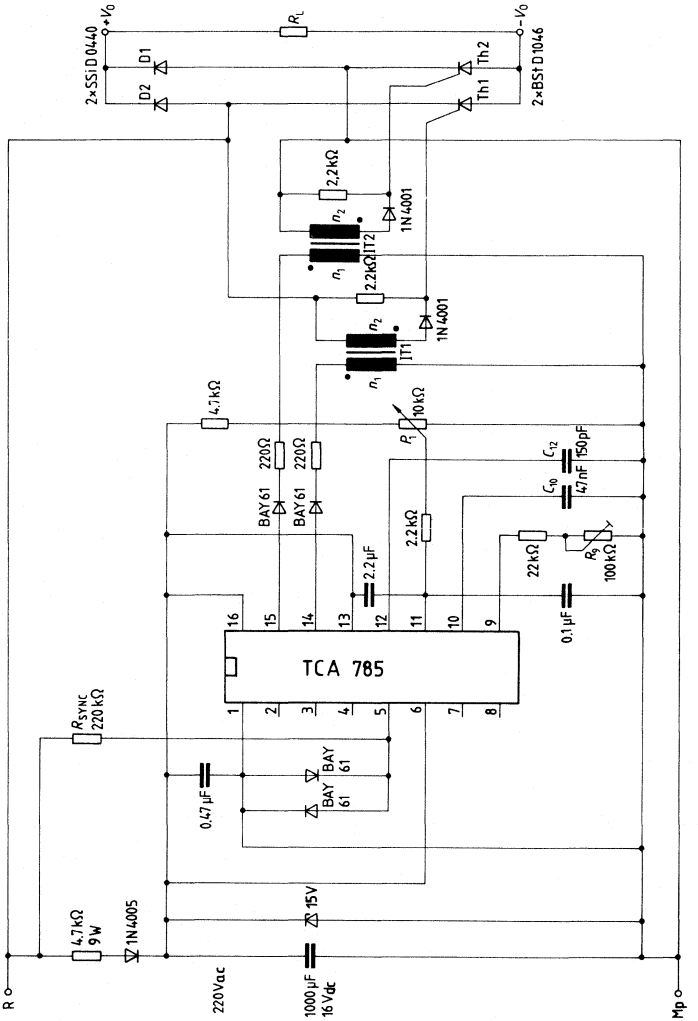


Shown is the possibility to trigger two antiparalleled thyristors with one IC TCA 785. The trigger pulses can be shifted continuously within a phase angle between 0° and 180° by means of a potentiometer. During the negative line half wave the trigger pulse of pin 14 is fed to the relevant thyristor via a trigger pulse transformer. During the positive line half wave, the gate of the second thyristor is triggered by a trigger pulse transformer at pin 15.

Half-controlled single-phase bridge circuit with trigger pulse transformer and direct control for low-power thyristors



Half-controlled single-phase bridge circuit with two trigger pulse transformers for low-power thyristors



TLE 3101
TLE 3102
TLE 3103
TLE 3104

Bipolar IC

Type	Ordering code	Package	Fig. No.
TLE 3101	Q67000-A2337	DIP 18	11
TLE 3102	Q67000-A2338	DIP 14	7
TLE 3103	Q67000-A2339		
TLE 3104	Q67000-A2340	DIP 8	6

These bipolar phase control ICs require, for most applications, only a minimum number of external components. Typical applications are motor control, brightness control, temperature control, cos φ optimization for squirrel-cage motors, and starting current limitation.

Thanks to their high efficiency, the TLE 310x ICs are particularly suitable for consumer goods, such as kitchen equipment and washing machines, vacuum cleaners, electric irons and hobbyist appliances.

A special feature is the soft start which requires only straightforward wiring, and is e.g. used in portable drills for center punching.

Features

- Direct supply from ac line possible
- Low power consumption, typically 2.4 mA
- Only one capacitor for trigger pulse width and phase angle
- Highly stabilized reference voltage
- Negative triac gate trigger current, 100 mA max.
- No triac drive pulses during supply undervoltage
- Optional voltage or current synchronization

- TLE 3101 with independent on-chip op amp OP and comparator K3

The following versions were produced from that basic IC:

- TLE 3102 without comparator K3
- TLE 3103 without op amp OP
- TLE 3104 without K3, enable input E/A, control input $V_{control}$, and without Z diode output.

These simplified versions are provided for less complex low cost applications.

Functional description

The following is a description of the individual functional units (refer to block diagram) and their interactions:

Operational amplifier OP

Two inputs and the output are available. The op amp is internally compensated and has a push-pull output. Should be op amp not be required, the +input is to be connected to ground (the TLE 3101 and TLE 3102 then consume minimum current).

Comparator K 3

Comparator K3 ist not frequency-compsensated. The output is an open NPN collector which may drive e.g. an LED in switching operation. Should the comparator not be required, the −input is to be connected to ground. K3 then has minimum current consumption.

Reference voltage source

A temperature-stabilized voltage source is available for control and regulating circuits.

Sawtooth generator

In this unit, a sawtooth synchronized to the line is generated by the external R_S and C_S. The phase angle of the triac is determined by comparison of the sawtooth voltage and the control voltage. The trigger pulse width for the driver is provided by the falling edge of the sawtooth generator. The charge of C_S determines the trigger pulse width. A special circuit ensures the release of only one trigger pulse per line half period.

Comparators K1, K2

Sawtooth voltage and control voltage are compared by means of comparators K1 and K2. Comparator K2 receives only half the sawtooth voltage. The phase angle limit can be adjusted within the complete phase angle range by applying a reduced reference voltage to input "$V_{\varphi max}$". Comparator K2 provides starting current limitation and/or phase angle limitation for inductive loads. Both comparator outputs are fed to the logic and driver unit.

The comparator with the smaller conduction angle is the dominating one. With $V_{\varphi max}$ dominating, the trigger pulse width is doubled – compared with the trigger pulse width in case of a dominating $V_{control}$.

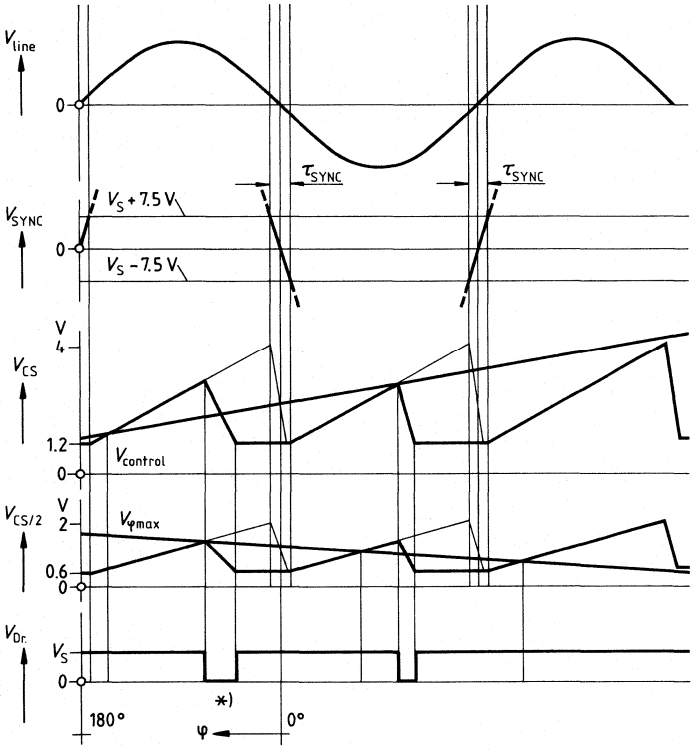
Logic + driver

The logic and driver unit for triac triggering is controlled by comparators K1, K2, and the enable input E/A. The E/A input is TTL-compatible and may disable or enable the trigger pulse. Logic +driver obtain information on the trigger pulse width from the sawtooth. The undervoltage monitoring enables the driver output only if the IC's supply voltage has reached the permissible minimum value. The driver output to the triac supplies negative pulses.

Synchronization

At the sync input, the phase angle is synchronized to the zero crossing point of the line voltage. The sync pulse width τ_{SYNC} has to be twice as large as the trigger pulse width.

Pulse diagram



Conduction angle (with resistive load)

*) With $V_{\varphi max}$ dominating, the trigger pulse width is doubled.

Maximum ratings

$T_{amb} = -25$ to 85 °C

		Lower limit B	Upper limit A	
Supply voltage	V_S	−0.3	33	V
Inputs op amp K3	V_I	−0.3	33	V
Output op amp	V_{Q1}	−0.3	V_S	V
	I_{Q1}	−5	3	mA
Output K3 (disabled)	V_{Q2}	−0.3	33	V
(enabled)	I_{Q2}	0	40	mA
Output V_{ref}	V_{ref}	−0.3	5	V
Z diode	I_Z	−35	35	mA
Input sync	I_{sync}	−10	10	mA
Input R_S	V_{RS}	−0.3	5	V
Input C_S	V_{CS}	−0.3	5	V
Input $V_{control}$	$V_{control}$	−0.3	V_S	V
Input $V_{\varphi max}$	$V_{\varphi max}$	−0.3	V_S	V
Enable input E/A	$V_{E/A}$	−0.3	33	V
Output driver (disabled)	$V_{Q dr}$	−0.3	33	V
(enabled)	$I_{Q dr}$	0	120	mA
Total power dissipation (time integral)	P_{tot}		700	mW
Junction temperature	T_j		125	°C
Storage temperature	T_{stg}	−55	125	°C
Thermal resistance (system-air)				
TLE 3104	$R_{th SA}$		100	K/W
TLE 3102, TLE 3103	$R_{th SA}$		70	K/W
TLE 3101	$R_{th SA}$		70	K/W

Operating range

Supply voltage	V_S	10	30	V
Ambient temperature	T_{amb}	−25	85	°C
Input sync	I_{SYNC}	−3.5	3.5	mA

Characteristics $V_S = 10$ to 30 V, $T_{amb} = -25$ to 85 °C		Test conditions	Lower limit B	typ	Upper limit A	
Current consumption						
without output load at op amp, K3, driver, V_{ref} without R_{SYNC} current	I_S	$V_S = 14.5$ V		2.4	3.2	mA
Reference voltage	V_{ref}		1.8	2.0	2.2	V
Load current	$-I_L$		0		3	mA
Stability $V_S = 10$ to 30 V	ΔV_{ref}				10	mV
$I_{ref} = 0$ to 3 mA	ΔV_{ref}				20	mV
Temperature coefficient	$\Delta V_{ref}/\Delta T$		−0.5		0.5	mV/K
Operational amplifier OP						
Open-loop voltage gain	G_{V0}		60	90		dB
Input offset voltage	V_{IO}		−10		10	mV
Input current	$-I_I$				2	µA
Common-mode input voltage range	V_{IC}		0		V_S-3	V
Output current	I_{Q1}		−3		1.5	mA
Transition frequency	f_T			2		MHz
Transition phase	φ_T			120		degrees
Output voltage	V_{Q1}		1.0		V_S-3	V
Comparator K3						
Input current	$-I_I$				2	µA
Input offset voltage	V_{IO}		−20		20	mV
Output enabled	V_{Q2}	$I_{Q2} = 20$mA		1.0	1.5	V
disabled	I_{Q2}	$V_{Q2} = 30$ V			5	µA
Common-mode input voltage range	V_{IC}		0		V_S-3	V
Input K1 ($V_{control}$)						
Input current	$-I_S$				2	µA
Control range:						
Conduction angle = 0°				4		V
(dependent on R_S and C_S)						
Conduction angle = 175°				1.2		V
Max. perm. conduction angle					SYNC pulse end −5	degrees
Input K2 ($V\varphi_{max}$)						
Input current	$-I_S$				2	µA
Control range:						
Conduction angle = 0°				2		V
(dependent on R_S and C_S)						
Conduction angle = 175°				0.6		V
Max. perm. conduction angle					SYNC pulse end −5	degrees

Characteriscs $V_S = 10$ to 30 V, $T_{amb} = -25$ to 85 °C		Test conditions	Lower limit B	typ	Upper limit A	
Z diode						
Z voltage	V_Z	$I_Z = 5$ mA	13	14.5	16	V
Enable input E/A						
Input current	$-I_I$				2	µA
H input voltage for driver output, active	V_{IH}		2.8			V
L driver output, disabled	V_{IL}				0.8	V
Triac trigger output						
Output, enabled	V_L	$I_Q = 10$ mA	1.4	2	2.5	V
		20 mA	1.4	2	2.5	V
		50 mA	1.4	2	3.0	V
		100 mA	1.4	4	6.0	V
Output, disabled	I_Q	$V_Q = 30$ V			10	µA
Input SYNC						
Switching current	I_{SYNC}			± 20		µA
Switching threshold	V_{SYNC}			V_S±7.5		V
Output disconnection at V_S undervoltage	V_S		7.5	8	10	V
Input R_S, C_S (refer to calculation formulae)						
Limit value C_S	C_S		5		100	nF
Limit value R_S	R_S		33			kΩ

Dimensioning notes and calculation formulae

1. Select trigger pulse width according to triac type and load.

2. **Calculate** C_S (for a $V_{control}$ domination)
   C_S (nF) = trigger pulse width (µs) x 0.2
   The formula yields the typical value
   e.g. T = 50 µs results in C_S = 10 nF

3. **Calculate** R_S (for 4 V max. sawtooth voltage)

$$R_S\ (k\Omega) = \frac{1}{\text{trigger pulse width } (\mu s)} \times 2 \times 10^4$$

   The formula yields the typical value
   e.g. T = 50 µs results in R_S = 400 kΩ

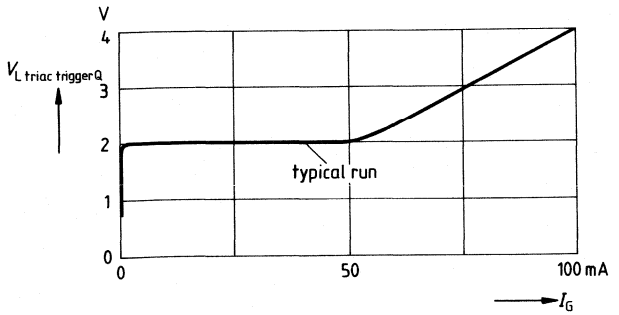
4. **Select R_{SYNC} resistance at SYNC input**
   The sync pulse width (from $V_S \pm 7.5$ V, $I_{SYNC} = \pm 20$ µA) has to be twice as large as the trigger pulse width.

4.1 Sync pulse width ≥ 2 x trigger pulse width x safety factor (according to component deviation and line voltage variation)

4.2 R_{SYNC} (kΩ) = [sync pulse width (µs) x line voltage (V rms) x 2.23×10^{-4} – 7.5] x 50.
e.g. 560 µs sync pulse width and 220 V rms result in R_{SYNC} = 1 MΩ.
With 220 V rms line voltage, the minimum permissible resistance R_{SYNC} is 100 kΩ corresponding to a pulse width of 195 µs.

5. **Calculate** R_G

$$R_G = \frac{V_S - \text{triac gate voltage} - \text{low-voltage triac trigger output}}{I_G}$$



6. **Calculate** R_S

6.1 Calculation of R_S requires first of all the determination of the total current consumption. Insert the arithmetic mean values of the currents for one line cycle.

6.2 $\bar{I}_{tot} = \bar{I}_S = 3.2\ mA + \bar{I}(V_{ref}) + \bar{I}_{Q1}\ (OP) + \bar{I}_{Q2}\ (K3) + \bar{I}$(driver output) $+ \bar{I}$ (additional external circuit currents) $+ |\bar{I}|\ (R_{SYNC})$.

6.3 $R_S\ (k\Omega) = \dfrac{\text{rms line voltage (V)}}{\bar{I}_{tot}\ (mA)} \times 0.455 \times \text{safety factor}$

(corresponding to component deviation and line voltage variation)

e.g. $\bar{I}_{tot} = 5$ mA und $V_{line} = 220$ V result in $R_S = 20\ k\Omega$.

Employing the internal Z diode reduces the IC's V_S voltage to 14.5 V.

7. **Calculate** C_G

7.1 Selection of the maximum permissible ripple at the V_S input, based on the desired functional quality and the special external components.

7.2 The ripple amplitude at the V_S input of the unit should not exceed $V_{pp} = 2$ V.

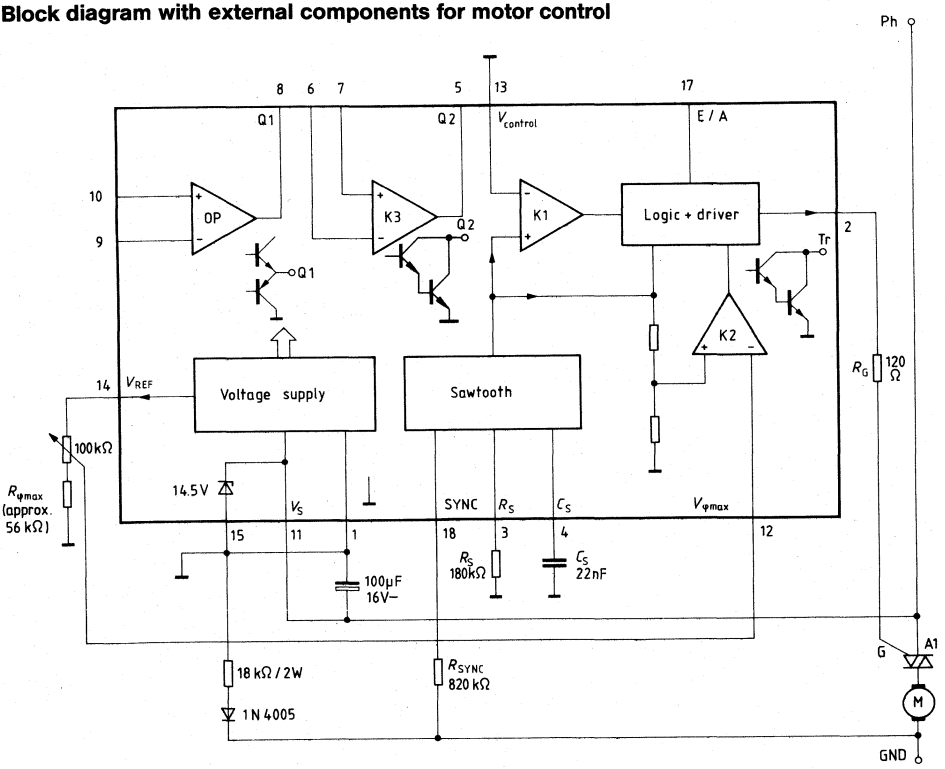
7.3 $C_G\ (\mu F) \geq \dfrac{\bar{I}_{tot}\ (mA)}{V_{pp}} \times 15$

e.g. ripple $V_{pp} = 0.75$ V; $\bar{I}_{tot} = 5$ mA results in $C_G = 100\ \mu F$

Pin configuration for TLE 3101

Pin No.	Function	Pin No.	Function
1	Ground	10	+ input op amp
2	Triac trigger output	11	V_S
3	R_S	12	$V_{\varphi max}$
4	C_S	13	$V_{control}$, K1
5	Output Q2, K3	14	V_{ref}
6	− input K3	15	Z diode
7	+ input K3	16	N.C.
8	Output Q1, op amp	17	Enable input E/A
9	− input op amp	18	Synchronization input (SYNC)

Block diagram with external components for motor control

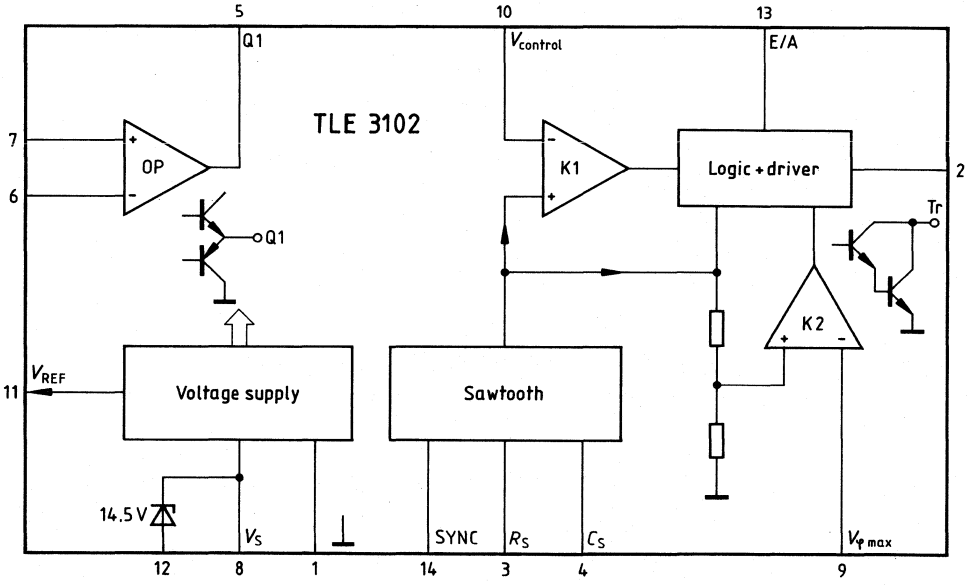


The **TLE 3102** with on-chip op amp for external use is particularly suitable as a speed controller with P, PI, or PID characteristic; the op amp serves as adjustable gain amplifier. An actual value which is proportional to speed can be formed by rectification of the tacho amplitude.

Pin configuration

Pin No.	Function	Pin No.	Function
1	Ground	8	V_S
2	Triac trigger output	9	$V_{\varphi max}$
3	R_S	10	$V_{control}$, K1
4	C_S	11	V_{ref}
5	Output Q1, op amp	12	Z diode
6	− input op amp	13	Enable input E/A
7	+ input op amp	14	Synchronization input (SYNC)

Block diagram

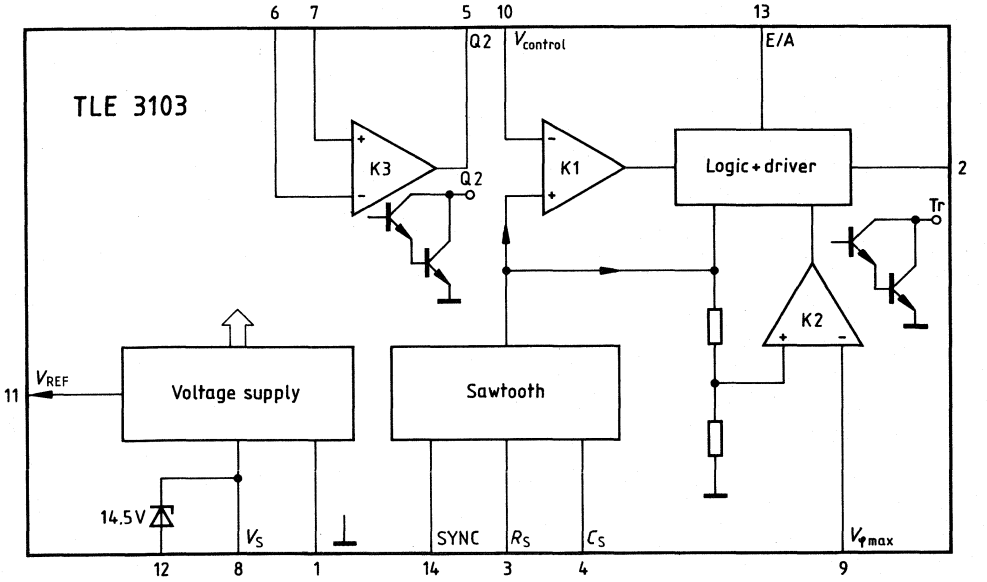


The **TLE 3103** with on-chip comparator for external use is particularly suitable for phase control systems in which special functions, such as blocking protection or overtemperature protection, are required.

Pin configuration

Pin No.	Function	Pin No.	Function
1	Ground	8	V_S
2	Triac trigger output	9	$V_{\varphi max}$
3	R_S	10	$V_{control}$, K1
4	C_S	11	V_{ref}
5	Output Q2, K3	12	Z diode
6	− input K3	13	Enable input E/A
7	+ input K3	14	Synchronization input (SYNC)

Block diagram

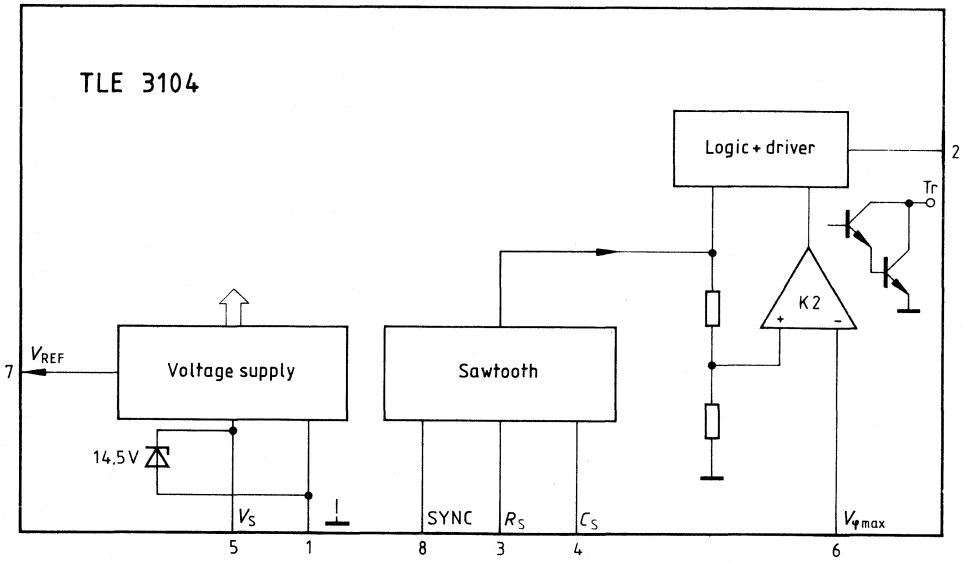


The **TLE 3104** is particularly suitable for simple, low-cost phase control and motor control systems, in which the actual value is formed by rectification of the tacho amplitude.

Pin configuration

Pin No.	Function	Pin No.	Function
1	Ground	5	V_S
2	Triac trigger output	6	$V_{\varphi\,max}$
3	R_S	7	V_{ref}
4	C_S	8	Synchronization input (SYNC)

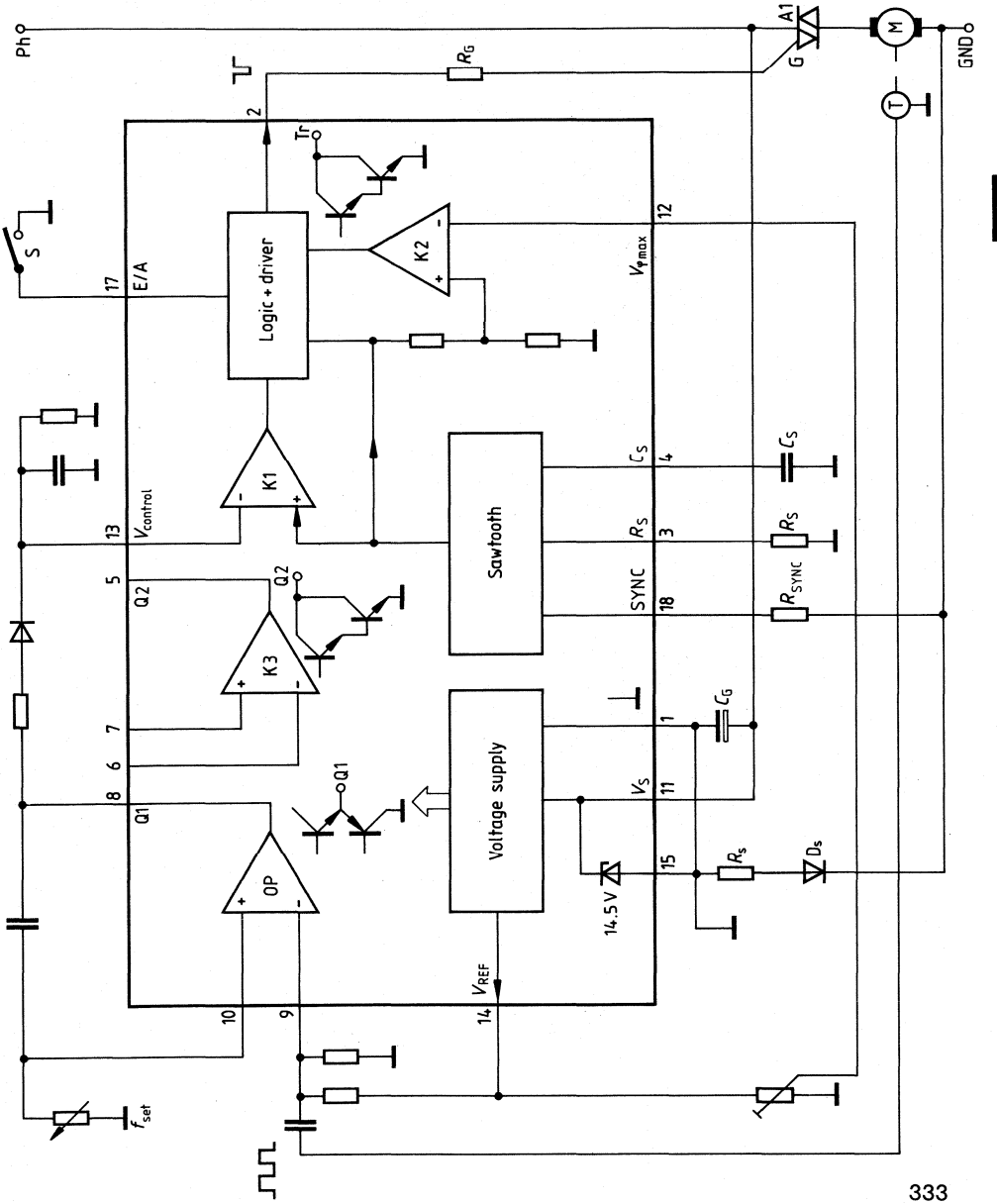
Block diagram



Application examples

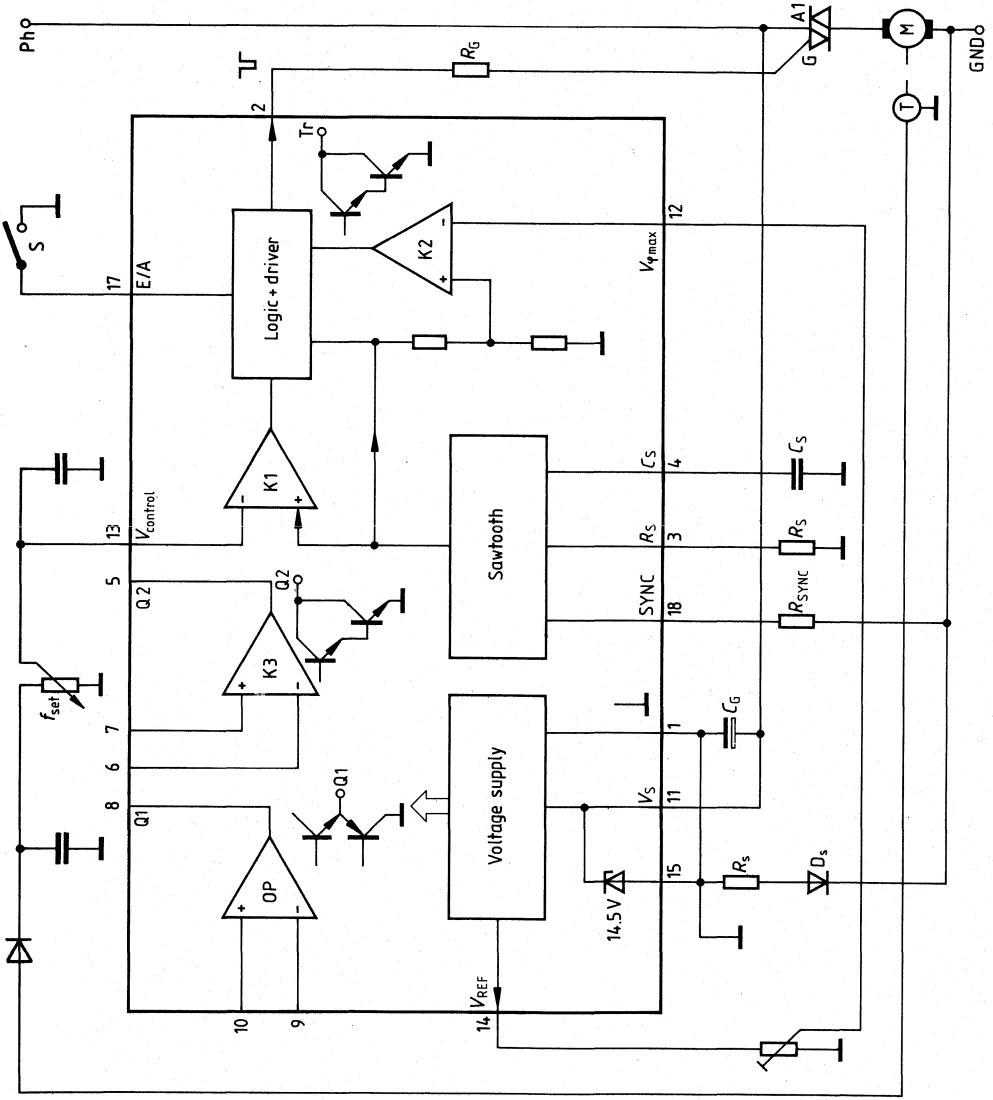
Schematic circuit diagram for motor control using TLE 3101

The tachogenerator provides a **frequency** being processed by the op amp (monoflop).

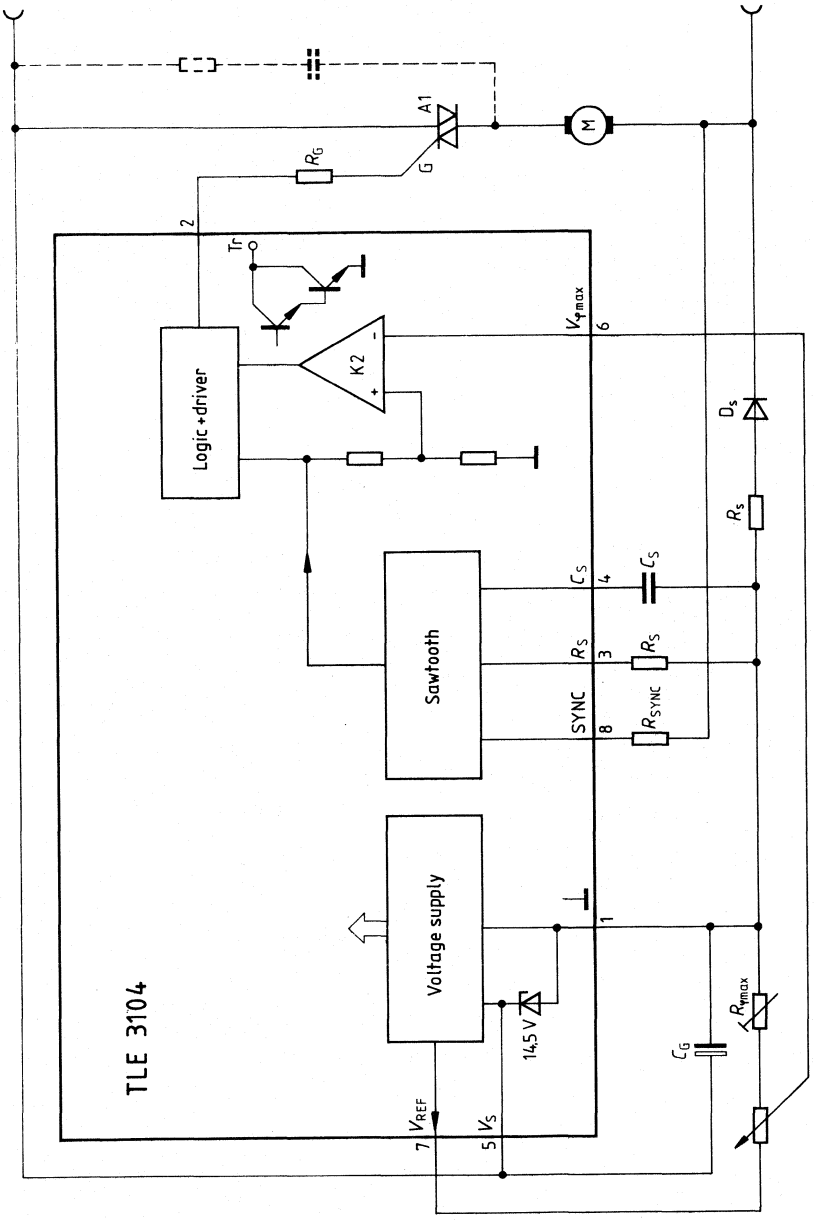


Schematic circuit diagram for motor control using TLE 3101

The tachogenerator provides a **voltage** which is rectified and stabilized, and then fed to input $V_{control}$.

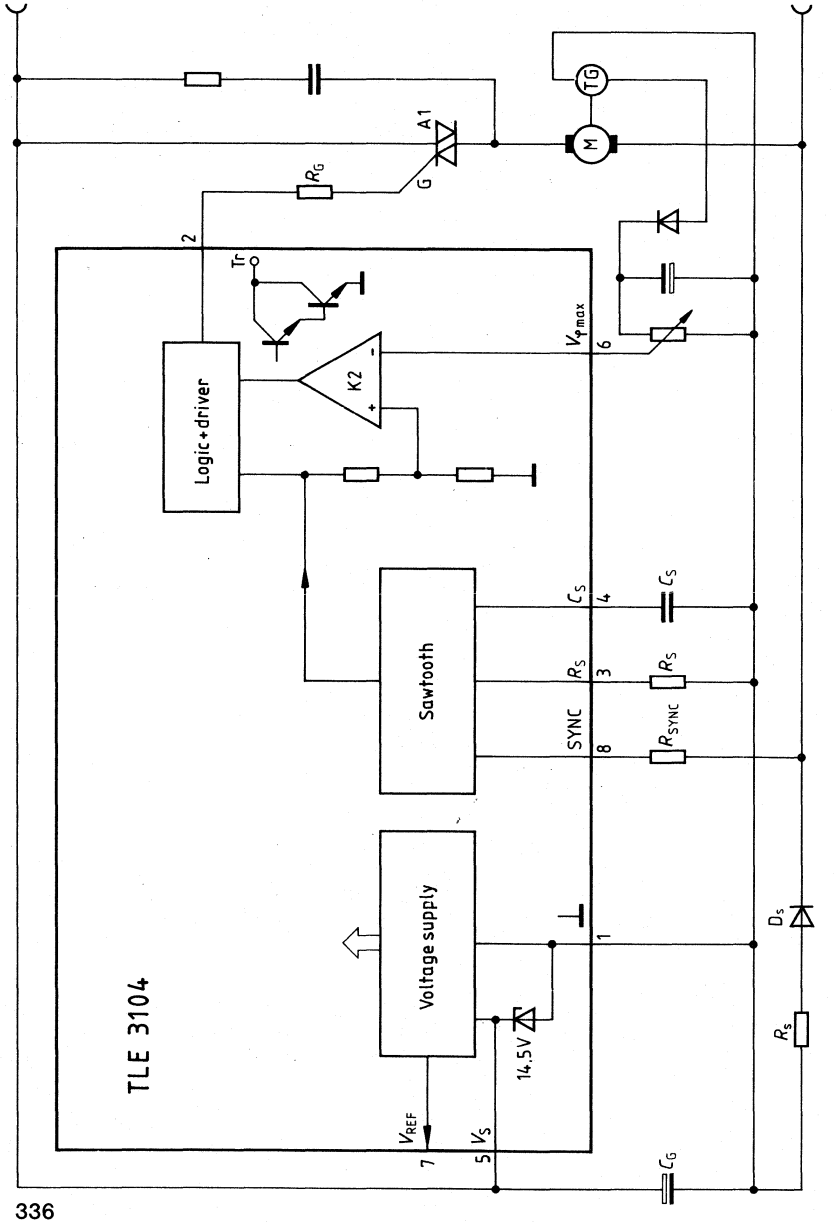


Schematic circuit diagram for motor control using TLE 3104



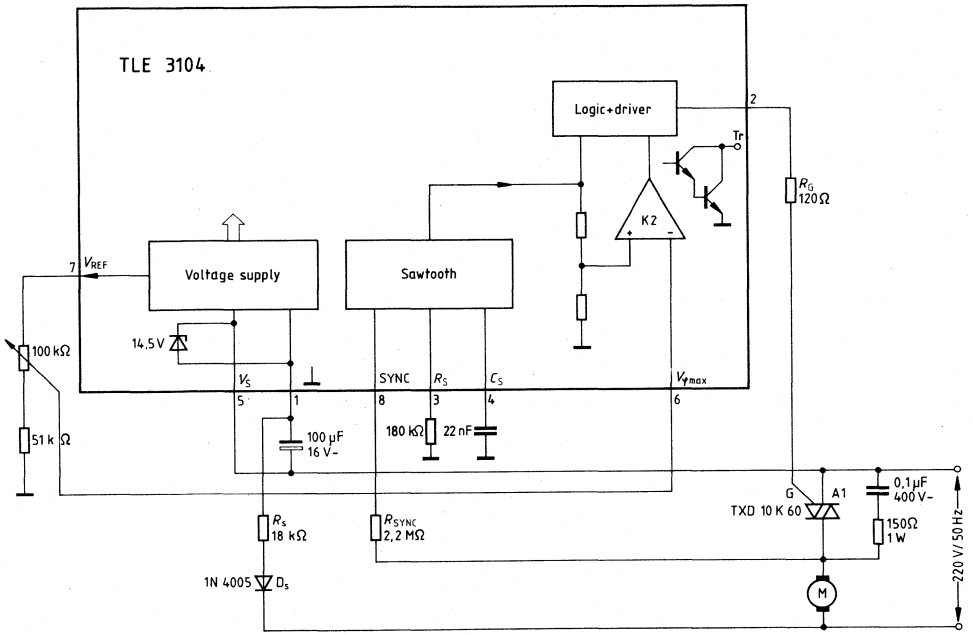
Schematic circuit diagram for motor control using TLE 3104

The tachogenerator supplies a **voltage,** which is rectified and stabilized and then fed to input $V_{control}$.



Current synchronization in case of inductive load control using TLE 3104

Particularly in case of phase control of inductive loads, such as transformers and shaded-pole motors, there is a risk of half-wave operation as a result of the phase shift between voltage and current. In order to avoid this condition, the synchronization resistor is connected to A 2 of the triac (this method cannot be applied in the event of severe brush sparking of the motor).



Notes:

The pulse width selected for the trigger pulse must be so great that the triac reaches its holding current, even with a great phase angle (critical: positive half-wave). For this reason, it may be necessary to select a lower value for the ac line series resistor.

The sync pulse must be at least twice as wide as the trigger pulse (see also page 323 and page 327/para. 4).

Electronic Dimmer
Electronic Light Switch

S 576 A, B, C
S 576 D

MOS IC

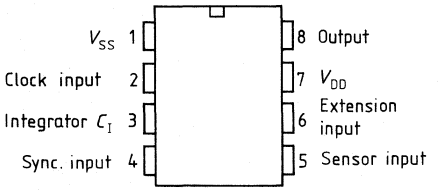
Type	Ordering code	Package	Fig. No.
S 576 A	Q67100-Y518	DIP 8	6
S 576 B	Q67100-Y519		
S 576 C	Q67100-Y506		
S 576 D	Q67100-Y520		

The IC S 576, constructed in PMOS depletion technology, permits the design of a digital electronic dimmer or light switch. Turning on and off as well as the setting of the required brightness are carried out via a single sensor or via an equivalent extension input, respectively.

Features

- Sensor operation – no mechanically moveable switching elements
- Operation is also possible from several extensions by means of sensors or push-buttons
- Can be interchanged with electromechanic wall switches in conventional light installations
- Easy connection to a wireless remote control
- Brightness control with a physiologically approximated linear characteristic
- Very high interference immunity
- The set brightness value remains stored during short line interruptions of < 1 s
- Low power dissipation
- Very few peripheral components
- Clock input provides for automatic dimming (slumber switch)

Pin configuration
top view



Maximum ratings
(without external protective circuitry)

		Lower limit B	Upper limit A	
Supply voltage	V_{DD}	−20	0.3	V
Input voltage	V_I	−20	0.3	V
Ambient temperature during operation	T_{amb}	0	80	°C
Junction temperature	T_j		125	°C
Storage temperature	T_{stg}	−55	125	°C
Thermal resistance (system-air)	$R_{th\,SA}$		135	K/W

Characteristics
$T_{amb} = 25$ °C, all voltage ratings are referred to $V_{SS} = 0$ V

		Test conditions	Lower limit B	typ	Upper limit A	
Supply voltage	V_{DD}		−18	−15	−13	V
Supply current	I_{DD}	$V_{DD} = -15$ V		1.0	1.4	mA
Supply current with missing sync signal	I_{DD}	$V_{DD} = -15$ V			0.85	mA
Input reverse current	I_I	$V_I = V_{SS} - 10$ V		< 0.1	3	µA
Input capacitance	C_I	$V_I = 0$ V, f=1MHz			5	pF
Sensor input						
H input voltage	V_{IH}	with series	$V_{SS}-2$			V
L input voltage	V_{IL}	resistor 10 MΩ			$V_{SS}-8$	V
Input current	I_{IH}	from 220 V line			35	µA
HL transition time (trigger transition)	t_{THL}			line sine wave		
LH transition time	t_{TLH}					
Frequency with active signal	f	synchronized with 50/60 Hz clock at sync input		50/60		Hz
Extension input						
H input voltage	V_{IH}		$V_{SS}-2$			V
L input voltage	V_{IL}				$V_{SS}-8$	V
Input current	I_{IH}				35	µA

Characteristics (cont'd)		Test conditions	Lower limit B	typ	Upper limit A	
Sync input (pin 4)						
H input voltage	V_{IH}	with series	1/2 V_{DD}+2			V
L input voltage	V_{IL}	resistor 1.5 MΩ			1/2 V_{DD}−2	V
Input current	I_{IH}	from 220 V line			240	µA
HL transition time (trigger transition)	t_{THL}			line sine wave		
LH transition time	t_{TLH}					
Frequency	f			50/60		Hz
Clock input (pin 2)						
H input voltage	V_{IH}		V_{SS}−2		V_S+0.3	V
L input voltage	V_{IL}		V_{DD}		V_{SS}−8	V
HL transition (trigger transition)	t_{THL}				100	µs
LH transition	t_{TLH}				100	µs
Clock frequency	f_{CLK}		0		500	Hz
Without clock	V_{IO}		V_{SS}		V_{SS}+0.3	V
Integrator (pin 3)						
External components	C_I	compare with fig.1		47		nF
Output						
L output current	I_Q	V_{DD} = −15 V, V_{QL} = −3 V	25			mA
L pulse width	t_{QL}	50 Hz line		40		µs
H output voltage	V_{QH}	compare with text	V_{SS}		V_{SS}+0.5	V
HL transition time	t_{HLQ}				20	µs
LH transition time	t_{LHQ}				20	µs

Operation of the control inputs

Input potential during both half waves of the line phase:

Function	Line half wave	Sensor input	Extension input		
operated	positive	L	H		
	negative	0	H		
not operated	positive	H	L	or	0
	negative	0	0		L

H: V_{IH}
L: V_{IL}
0: any

Functional description

The type series S 576 permits the design of fully electronic dimmers and light switches for light bulbs (resistive loads) which are operated in each case via a single sensor.

In conventional lighting circuit installations it is possible to interchange this component with mechanic wall switches as well as to operate all functions from several switching points (extensions).

The brightness is set by phase control. Its digital logic is sychronized with the line frequency. It is possible to supply the IC via a two-wire-connection as the conduction angle is limited to a maximum of 152° of the half wave.

Operation

1. Dimmers S 576 A, S 576 B, S 576 C (see figure 1)

The integrated circuit can distinguish the instructions "turning ON/OFF" and "dimming" due to the duration of the control input operation.

Turning ON/OFF

Short touch (50 to 400 ms) of the sensor area turns the lamp on or off, depending on its preceding state. The switching process is activated at the end of touching.

Setting of the brightness (dimming)

If the sensor is touched for a longer period (> 400 ms), the conduction angle will be varied continuously. It runs across its control loop in approximately 7 s (e.g. bright-dark-bright) and continues this sequence until the finger is removed from the sensor.

The following process is carried out to enable an easy operation also in the lower brightness range: the phase control angle is controlled such that during the run across the control loops, the lamp brightness varies approximately physiological-linearly with the operating time, and rests for a short period when a minimum brightness is reached.

The conduction angle can be controlled in the half wave range between 35° and 152° by means of the sync input circuitry (R_2, C_4) specified in the application example.

By increasing the *RC* time constant it is possible to shift the control range towards smaller conduction angles (effects the minimum brightness).

Control behavior

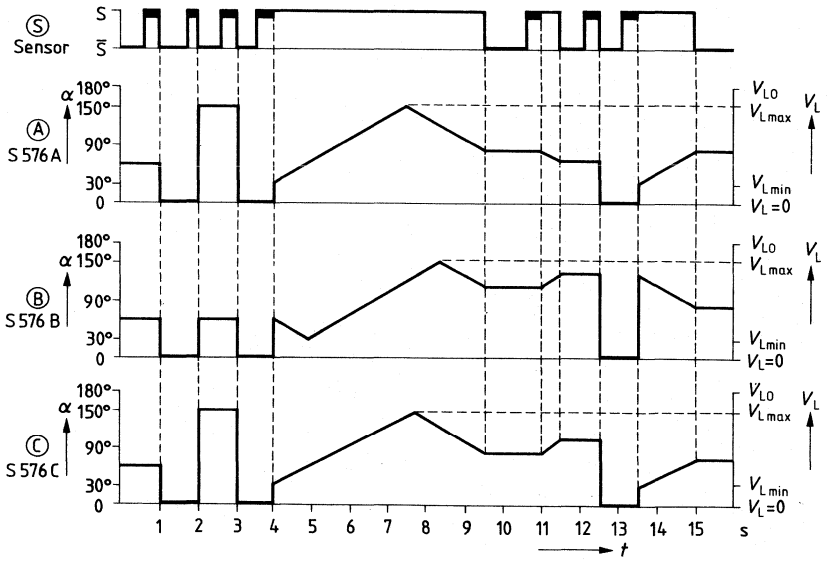
The three versions S 576 A, B, C, differ in their control behavior.

S 576 A With turning on, the maximum brightness is always set; with dimming, control is started from the minimum brightness. With repeated dimming, control is carried out in the same direction (e.g. "brighter").

S 576 B With turning off, the selected brightness is stored and again set when the switch is turned on. Dimming starts at that stored value and the control direction is reversed with repeated dimming.

S 576 C With turning on, the maximum brightness is always set; with dimming, control is started from the minimum brightness. The control direction is reversed with repeated dimming.

Control behavior of the electronic dimmers S 576 A, B, C (schematic)



α Conduction angle
V_L Lamp voltage
S Control signal: S Sensor touched (▬ <0,4s; ▬ >0,4s)
S̄ Sensor not touched
A S 576 A
B S 576 B
C S 576 C

Figure 1

2. Light switch S 576 D (see figure 2)

Upon touching the sensor area (> 50 ms) the lamp is turned on or off alternatively with maximum brightness. The switching process is activated at the start of touching.

Dimming or turning off the light via the clock input is also possible, as in the case with the dimmer.

Control behavior of the electronic light switch S 576 D (schematic)

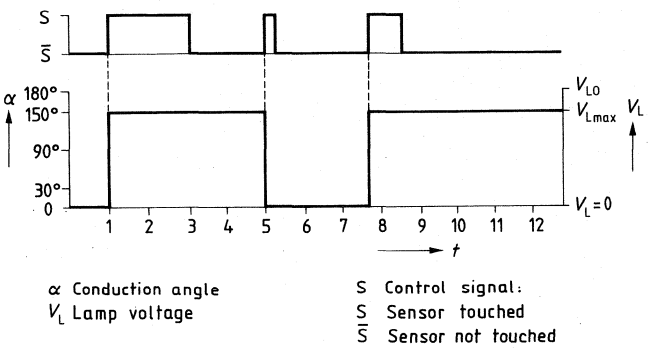


Figure 2

External circuitry (see figure 3)

The suggested circuit design of S 576 performs the following functions:

- current supply for the circuit (R_1, C_2, D 1, D 2, C_3)
- filtered signal for synchronization of the internal time base (PLL circuit) with line frequency (R_2, C_4)
- protection of the user (R_8, R_9)
- sensitivity setting of the sensor (R_7)
- current limitation in the case of incorrect polarization of the extension (R_5, R_6).

  Both resistors can be omitted if no extension is connected. In this case, pin 6 must be interconnected with V_{DD} (pin 7).
- D 3: reduction of positive voltages which may arise during the triggered state at the gate of some triacs, to values below $V_{SS}+0.5$ V (refer to characteristic data). If suitable triacs are used, diode D 3 can be omitted. (This feature of the triac depends on the anode current and on the internal resistance between G and A 1, and can be measured and specified by the manufacturer).

Application circuit S 576

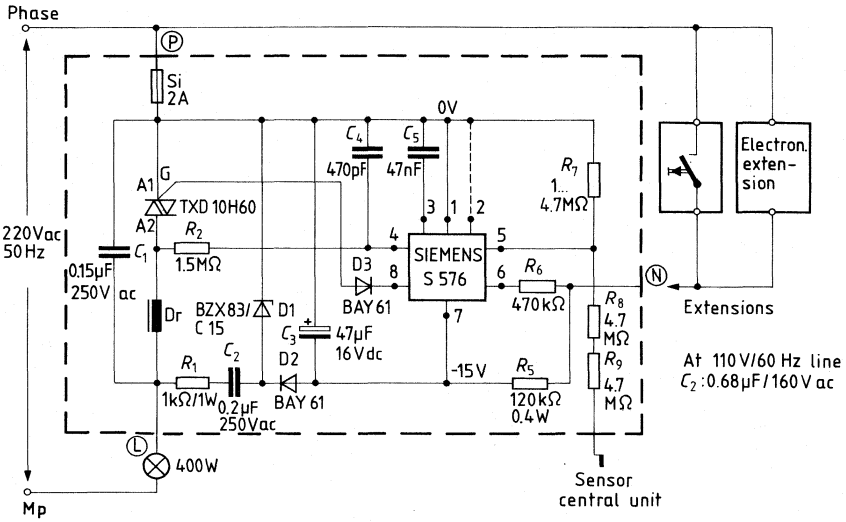


Figure 3

Extensions

All switching and control functions can also be performed from extensions which are connected to an extension input reserved for this purpose. The central unit and the extensions are equivalent. Electronic sensor switches or mechanical pushbutton switches can be connected to the extensions. During operation, H potential must be applied to the extension input for both line half waves.

An electronic circuit suitable for this purpose, is shown in the application example (figure 4). The circuit operates as return delay and takes over the triggering of the switching transistors during the negative line half wave.

- Response time approx. 2 ms
- Return delay time approx. 30 ms
- Protection against incorrect polarization (R_1, D 1, Si)

Application circuit: electronic extension

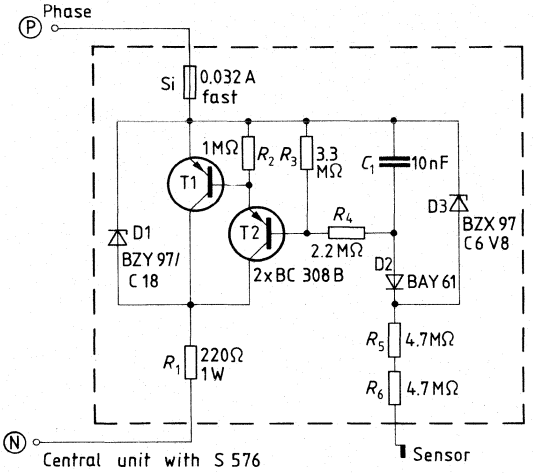


Figure 4

Wireless remote control

The connection of a wireless remote control to the extension is very easy. All functions of the S 576 can be performed with the aid of a single transmission channel.

Slumber switch (clock input)

In the unused state, the clock input is short-circuited to V_{SS}. A slumber switch can be obtained by applying an externally generated clock to this input. Each H L transition decrements the count of the internal brightness memory by one step. When the minimum brightness is reached, the clock turns the circuit to the OFF-state.

The application example (figure 5) shows an oscillator circuit which can also be connected to the power supply of the electronic dimmer or light switch by means of S 576.

The oscillator is enabled by touching the slumber switch sensor. Touching of the dimmer sensor disables the oscillator and, thereby, interrupts the automatic system.

Circuitry

- Oscillator with CMOS gates
- T1 and T2 provide a steep switching transition at the input of gate G3 in order to minimize current consumption (< 100 µA)
- Setting of the clock frequency and thus setting of the dimming time with the *RC* network (R_5, C_2)
- Sensitivity setting of the sensor area (R_1)

Application circuit: S 576 with a slumber switch

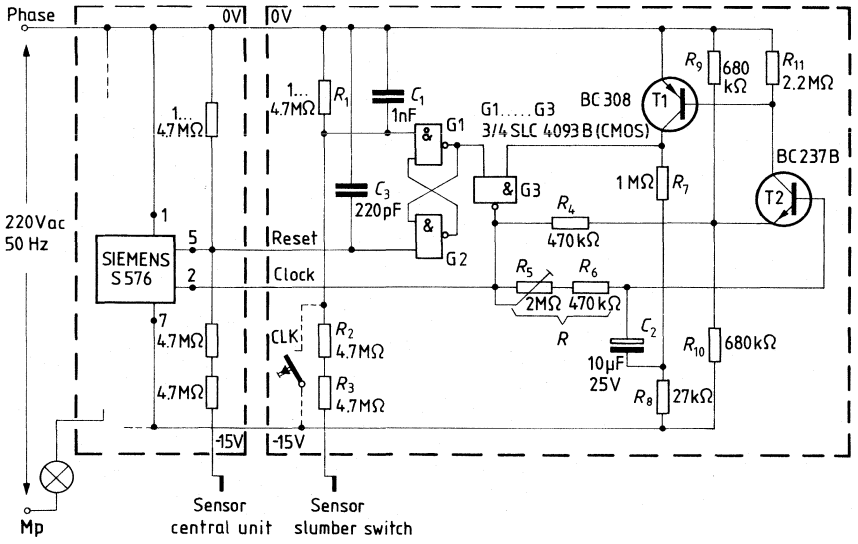


Figure 5

Interference immunity

A digitally determined immunity period of approximately 50 ms ensures a high interference immunity against electrical variations on the control inputs, and allows simultaneously an almost delay-free operation.

Due to the special logic of the extension input, even large ground capacitances of the control line will not lead to interference.

In the case of line interruption, the set switching state with the recommended external circuitry remains stored for about 1 s. After line interruptions for longer periods the circuit turns into the OFF-state.

General information

All stated time specifications refer to a line frequency of 50 Hz. In the case of a line frequency of 60 Hz, the periods are shortened accordingly.

A/D Converters

Bipolar IC

Type	Ordering code	Package	Fig. No.
■ SDA 5010	Q67000-Y621	DIC 16	9

The SDA 5010 is an ultra-fast A/D converter with 6 bit resolution. In addition to an exceptionally high strobe frequency of up to 100 MHz and excellent linearity, it offers the following features:

- Strobe frequency 100 MHz
- 6-bit resolution (1.6%)[1]
- ± 1/4 LSB linearity[2]
- No sample and hold required
- Dynamic driving of reference inputs for analog addition and multiplication
- ECL-compatible
- Low power dissipation of 450 mW
- Logic-compatible supply voltage +5 V; −5.2 V

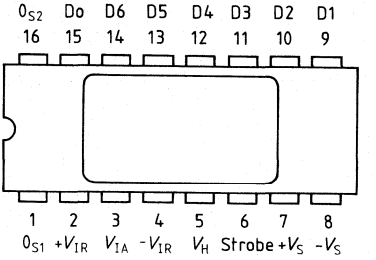
Maximum ratings

		Lower limit B	Upper limit A	
Supply voltage	$+V_S$	−0.3	6.0	V
Supply voltage	$-V_S$	−6.0	0.3	V
Input voltages	$V_{IA}, +V_{IR}, -V_{IR}$	−3.0	3.0	V
Strobe	V_{strobe}	$-V_S$	0	V
Hysteresis control	V_{Ihy}	0	3.0	V
Voltage difference	$0_{S1} - 0_{S2}$	−0.5	0.5	V
Operating temperature	T_{amb}	0	70	°C
Storage temperature	T_{stg}	−55	125	°C

1) A 7th bit (overflow output) enables extension of resolution
2) Measured at 50 MHz

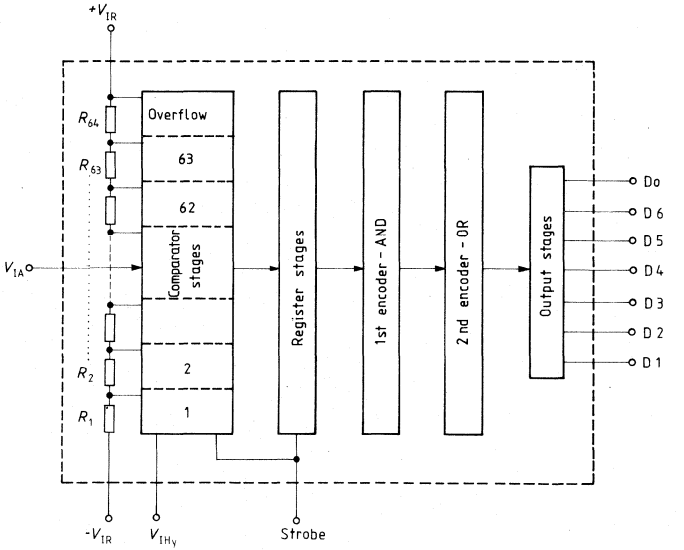
■ Not for new design

Pin configuration
top view



Pin No.	Symbol	Function
1	0_{S1}	Digital ground
2	$+V_{IR}$	Positive reference voltage (< +2.5 V)
3	V_{IA}	Analog signal input (max. ± 2.5 V)
4	$-V_{IR}$	Negative reference voltage (> −2.5 V)
5	V_{Ihy}	Hysteresis control (0 to +2.5 V)
6	Strobe	Strobe input (ECL)
7	$+V_S$	Positive supply voltage (+5 V)
8	$-V_S$	Negative supply voltage (−5.2 V)
9 to 14	D1 to D6	Data outputs bits 1 to 6 (ECL)
15	Do	Overflow
16	0_{S2}	Digital ground of output stages

Block diagram



Characteristics		Lower limit B	typ	Upper limit A	
Power supply					
Positive supply voltage	$+V_S$	4.5	5.0	5.5	V
Negative supply voltage	$-V_S$	−5.7	−5.2	−4.7	V
Current consumption					
at $+V_S = +5.0$ V; $V_{IA} \leq -V_{IR}$	I_S		30	60	mA
at $-V_S = -5.2$ V; $V_{IA} \leq -V_{IR}$	I_S		55	80	mA
Analog section					
Signal input					
Maximum input voltage	$V_{IA\,max}$	$-V_{IR\,min}$		$+V_{IR\,max}$	V
$V_{IA\,max} = \mid (+V_{IR\,max}) - (-V_{IR\,min}) \mid$				5	V
V_{IA} for 6-bit resolution	V_{IA}		0.3		V
V_{IA} for 1/2 LSB linearity	V_{IA}	1.2	0.6		V
V_{IA} for 1/4 LSB linearity	V_{IA}	2.4	1.2		V
Input current					
at $V_{IA} = +V_{IR}$ in sample mode	I_{IA}		150	500	µA
at $V_{IA} < -V_{IR}$ in sample mode	I_{IA}	−10		10	µA
$-V_{IR} < V_{IA} < +V_{IR}$ in hold mode	I_{IA}	−10		10	µA
Input capacitance					
at $V_{IA} < -V_{IR}$	C_{IA}		25		pF
Reference inputs					
Positive reference voltage	$+V_{IR}$	−2		2.5	V
Negative reference voltage	$-V_{IR}$	−2.5		2	V
Reference resistance	64 R	96	128	195	Ω
Digital section					
Strobe input					
H input voltage	V_{IH}	−1.1	−0.9	−0.6	V
L input voltage	V_{IL}	−2.0	−1.7	−1.5	V
H input current	I_{IH}	5	30	100	µA
L input current	I_{IL}	5	30	100	µA
Data outputs (100 Ω to −2 V)					
H output voltage	V_{QH}	−1.1	−0.9	−0.7	V
L output voltage	V_{QL}	−2.0	−1.7	−1.5	V

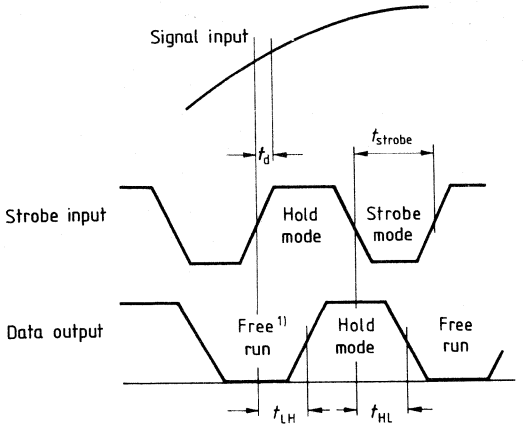
Characteristics (cont'd)

		Lower limit B	typ	Upper limit A	
Dynamic parameters					
Aperture time	t_d		2		ns
Aperture jitter			25		ps
Strobe[1]	t_{strobe}		4	5	ns
Signal transition time[2]	$t_{TLH\ Qmax}$		9		ns
Signal transition time[3]	$t_{THL\ Q\ min}$		11		ns
Strobe frequency[4]	f_{strobe}	100			MHz
Bandwidth (−3 dB)	B		130		MHz
Recovery time (1 V analog step)	t		5		ns

Notes on dynamic parameters

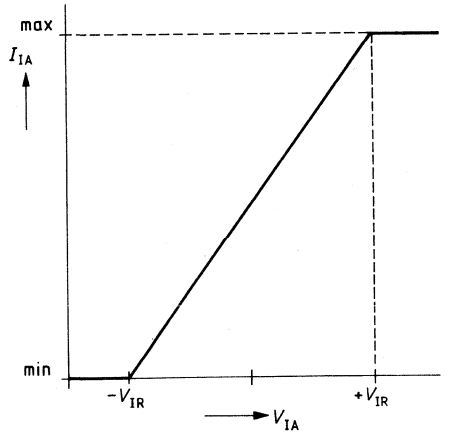
1) Minimal values are stated as necessary for operation at 100 MHz. At lower strobe frequencies it is particularly useful to use greater strobe times for increasing the maximal analog frequency, i.e. as long as the remaining hold time is adequate for secure data transfer.
2) The typical signal transition times $t_{TLH\ Qmax}$ are those measured with approx. 15 mV overdrive on the comparator. In addition to a certain dependence on code there is, for physical reasons (development of the feedback avalanche in the register stages), an exponential relationship between overdrive and delay of the output signal, this possibly leading to further signal delay at very low overdrive.
3) The details on $t_{THL\ Qmin}$ also refer to approx. 15 mV of overdrive. The transition time of the falling signal edge is considerably less dependent on the analog signal however.
4) The measurement is performed in the following test circuit with the settings stated.

Pulse diagram of strobe input and data outputs

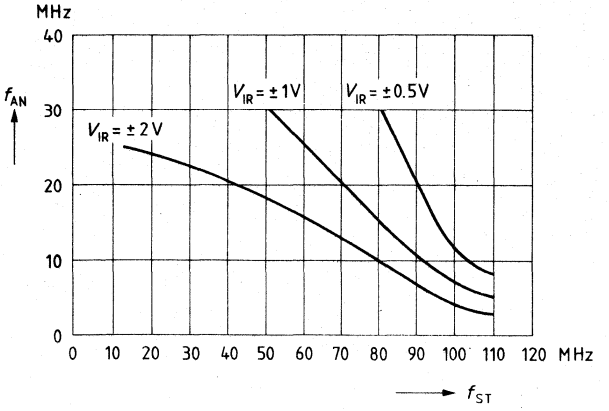


1) undefined output levels

Input current versus input voltage



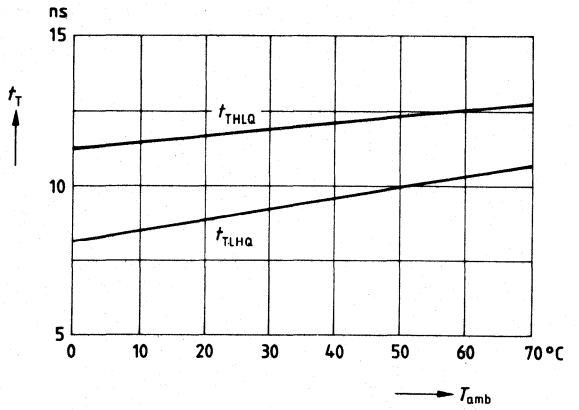
Maximum analog input frequency versus strobe frequency



Definition of f_{AN}:

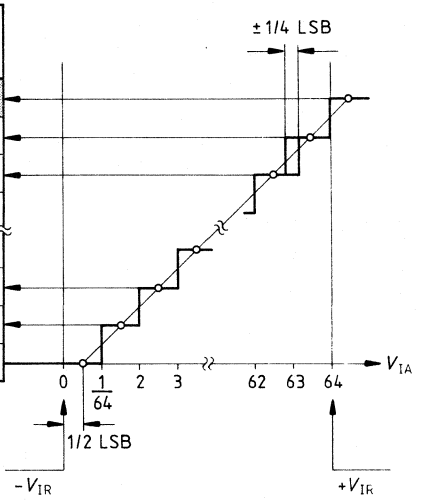
Upper limit of the analog input frequency which does not yet show missing codes.

Signal transition times versus ambient temperature

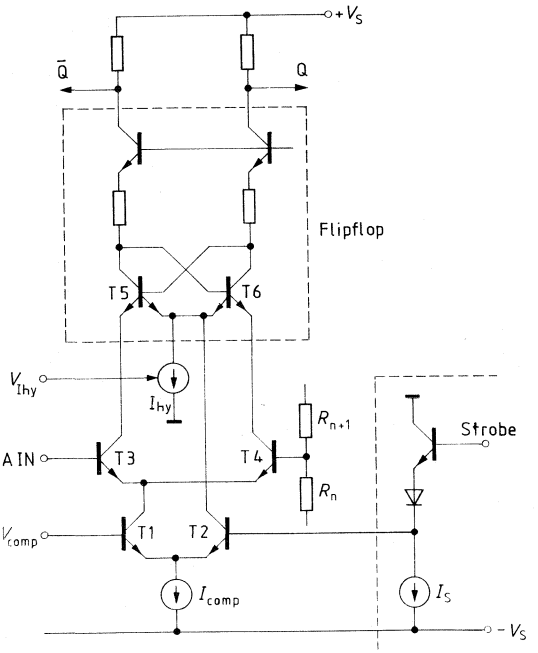


Transfer characteristic and truth table

Do	D6	D5	D4	D3	D2	D1
H	L	L	L	L	L	L
L	H	H	H	H	H	H
L	H	H	H	H	H	L
≈						≈
L	L	L	L	L	H	L
L	L	L	L	L	L	H
L	L	L	L	L	L	L

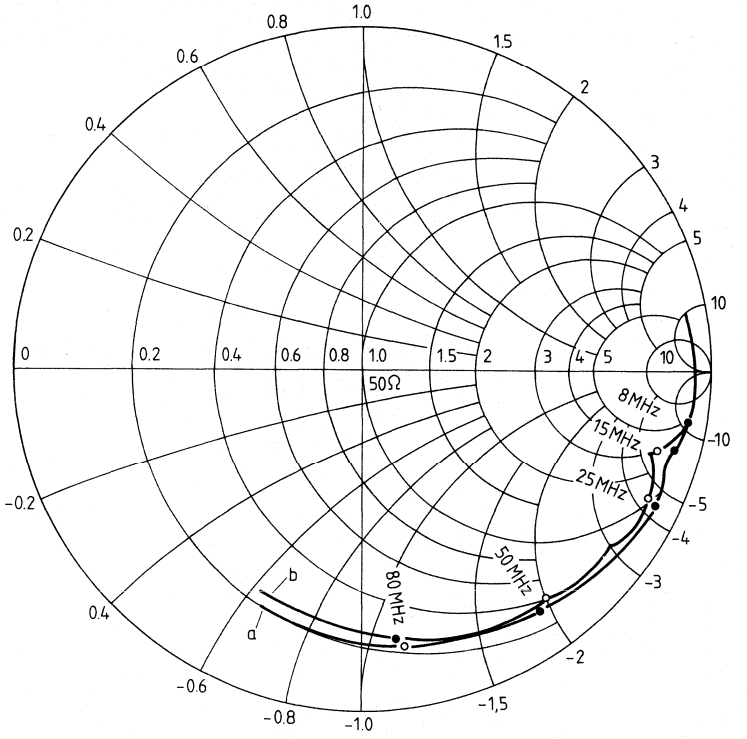


Input stage

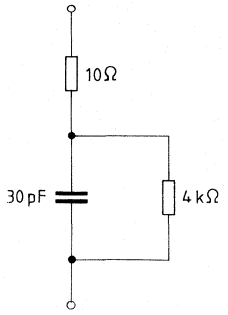


Smith diagram

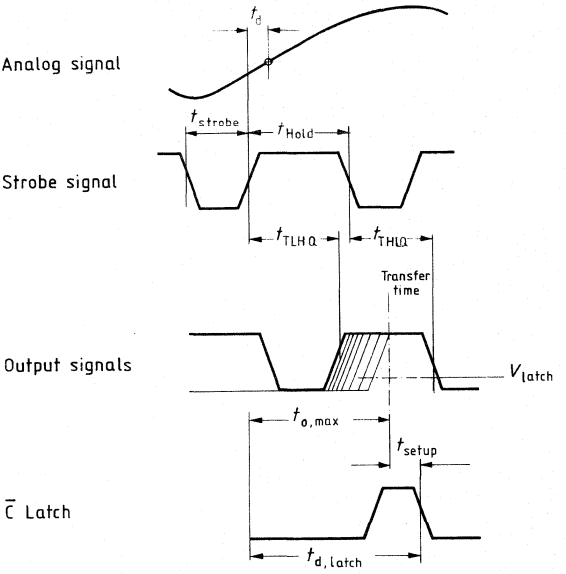
a) Nyquist plot of input impedance
b) Nyquist plot of equivalent circuit



Equivalent circuit

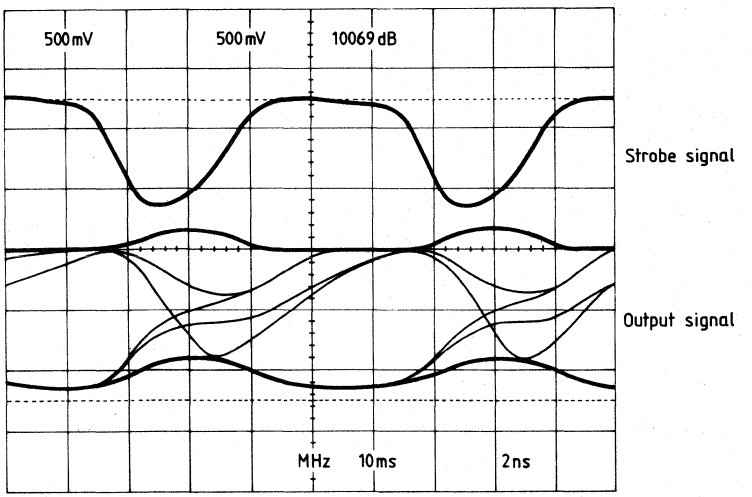


Schematic run of the signal in the measurement circuit for 100 MHz strobe frequency

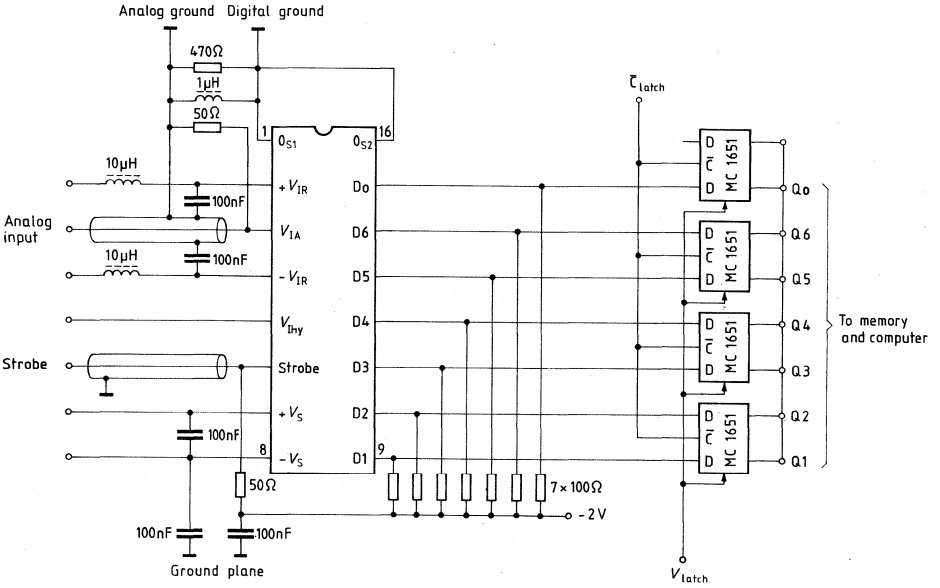


$t_{strobe} = 4.5$ ns, $t_{d,\,latch} = 15$ ns
$V_{latch} = -1.65$ V

Illustration of the signal run in the measurement circuit for 100 MHz strobe frequency



Measurement circuit



Bipolar IC

Type	Ordering code	Package	Fig. No.
SDA 6020	Q67000-Y584	DIC 16	9

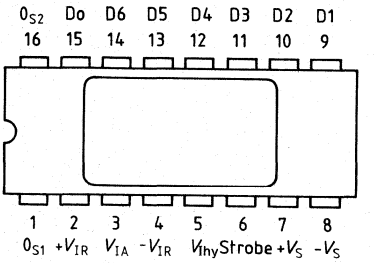
The SDA 6020 is an ultra-fast A/D converter with 6 bit resolution. In addition to a strobe frequency of 50 MHz and excellent linearity, it offers the following features:

- Conversion up to Nyquist frequency (25 MHz)
- 6-bit resolution (1.6%), simple extension to 8 bits
- ± 1/4 LSB linearity
- No sample and hold required
- Dynamic driving of reference inputs for analog addition and multiplication
- ECL-compatible (ECL → TTL matching possible, e.g. with SH 100.255)
- Low power dissipation of 450 mW
- Logic-compatible supply voltage +5 V; −5.2 V

Maximum ratings

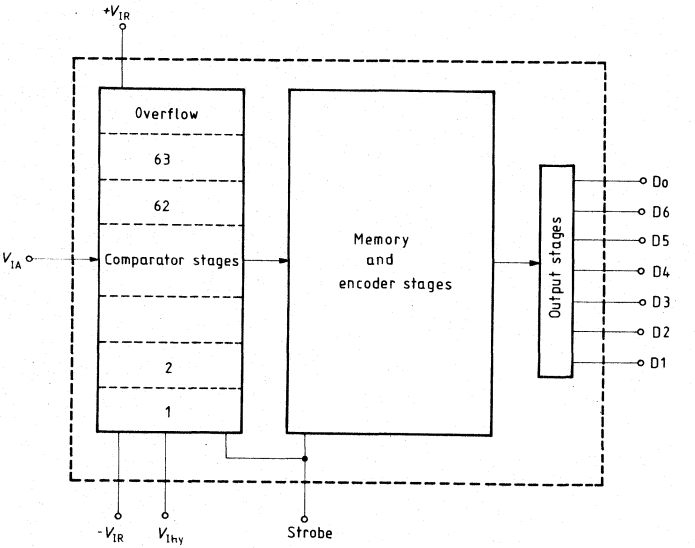
		Lower limit B	Upper limit A	
Supply voltage	$+V_S$	−0.3	6.0	V
Supply voltage	$-V_S$	−6.0	0.3	V
Input voltages	$V_{IA}, +V_{IR}, -V_{IR}$	−3.0	3.0	V
Strobe	V_{strobe}	$-V_S$	0	V
Hysteresis control	V_{Ihy}	0	3.0	V
Voltage difference	$0_{S1} - 0_{S2}$	−0.5	0.5	V
Operating temperature	T_{amb}	0	70	°C
Junction temperature	T_j		125	°C
Storage temperature	T_{stg}	−55	125	°C
Thermal resistance (system-air)	$R_{th\,SA}$		85	K/W

Pin configuration
top view



Pin No.	Symbol	Function
1	0_{S1}	Digital ground
2	$+V_{IR}$	Positive reference voltage (< +2.5 V)
3	V_{IA}	Analog signal input (max. ± 2.5 V)
4	$-V_{IR}$	Negative reference voltage (> −2.5 V)
5	V_{Ihy}	Hysteresis control (0 V to +2.5 V)
6	Strobe	Strobe input (ECL)
7	$+V_S$	Positive supply voltage (+5V)
8	$-V_S$	Negative supply voltage (−5.2 V)
9–14	D1 to D6	Data output bits 1 to 6 (ECL)
15	Do	Overflow
16	0_{S2}	Digital ground of output stages

Block diagram



Characteristics		Lower limit B	typ	Upper limit A	
Power supply					
Positive supply voltage	$+V_S$	4.5	5.0	5.5	V
Negative supply voltage	$-V_S$	−5.7	−5.2	−4.7	V
Current consumption					
at $+V_S = +5.0$ V; $V_{IA} \leq -V_{IR}$	I_S		30	60	mA
at $-V_S = -5.2$ V; $V_{IA} \leq -V_{IR}$	I_S		55	80	mA
Analog section $T_{amb} = 25$ °C; $+V_S = 5$ V; $-V_S = 5.2$ V					
Signal input					
Maximum input voltage	$V_{IA\,max}$	$-V_{IR\,min}$		$+V_{IR\,max}$	V
$V_{IA\,max} = \lvert (+V_{IR\,max}) - (-V_{IR\,min}) \rvert$				5	V
V_{IA} for 6-bit resolution	V_{IA}		0.3		V
V_{IA} for 1/2 LSB linearity	V_{IA}	1.2	0.6		V
V_{IA} for 1/4 LSB linearity	V_{IA}	2.4	1.2		V
Input current					
at $V_{IA} = +V_{IR}$ in sample mode	I_{IA}		200	800	µA
at $V_{IA} < -V_{IR}$ in sample mode	I_{IA}	−10		10	µA
$-V_{IR} < V_{IA} < +V_{IR}$ in hold mode	I_{IA}	−10		10	µA
Input capacitance					
at $V_{IA} < -V_{IR}$	C_{IA}			35	pF
Reference inputs					
Positive reference voltage	$+V_{IR}$	−2		2.5	V
Negative reference voltage	$-V_{IR}$	−2.5		2	V
Reference resistance	64 R	96	128	256	Ω
Digital section					
Strobe input					
H input voltage	V_{IH}	−1.1	−0.9	−0.6	V
L input voltage	V_{IL}	−2.0	−1.7	−1.5	V
H input current	I_{IH}	5	30	100	µA
L input current	I_{IL}	5	30	100	µA
Data outputs (100 Ω to −2 V)					
H output voltage	V_{QH}	−1.1	−0.9	−0.6	V
L output voltage	V_{QL}	−2.0	−1.7	−1.5	V

Characteristics (cont'd)

		Lower limit B	typ	Upper limit A	
Dynamic parameters					
Aperture time	t_d		2		ns
Aperture jitter			25		ps
Strobe	t_{strobe}		8	10[1]	ns
Signal transition time[2]	$t_{TLH\,Qmax}$		9		ns
Signal transition time[2]	$t_{THL\,Qmin}$		11		ns
Strobe frequency	f_{strobe}	50			MHz

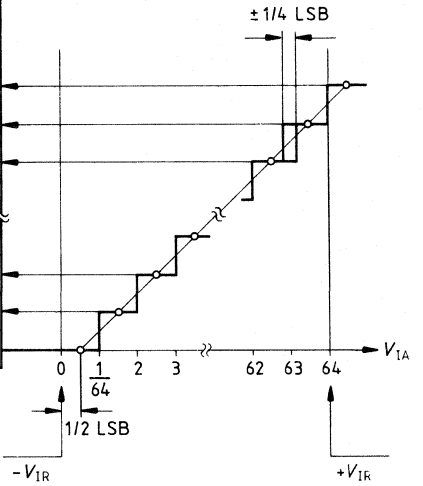
1) Exceeding this value at strobe frequencies of less than 50 MHz is quite permissible as long as the remaining hold time is adequate for secure data transfer.

2) The data transfer into the following circuit should occur with a delay t_d referred to the rising strobe edge in the range:

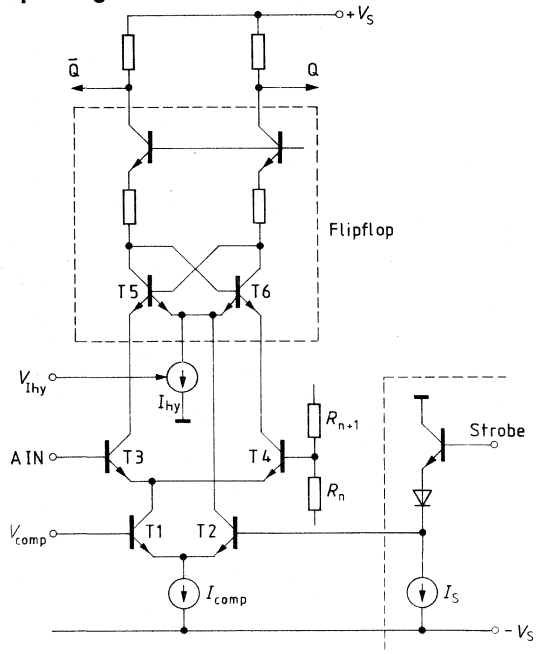
$$t_{TLH\,Qmax} + t_{hold/2} < t_d < t_{hold} + t_{THL\,Qmin}$$

Transfer characteristic and truth table

Do	D6	D5	D4	D3	D2	D1
H	L	L	L	L	L	L
L	H	H	H	H	H	H
L	H	H	H	H	H	L
≈						≈
L	L	L	L	L	H	L
L	L	L	L	L	L	H
L	L	L	L	L	L	L

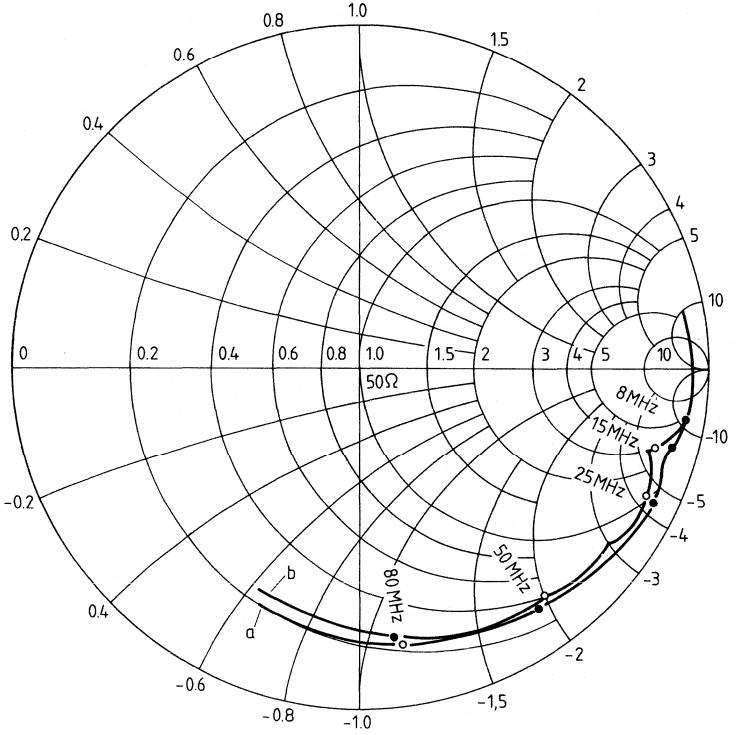


Input stage

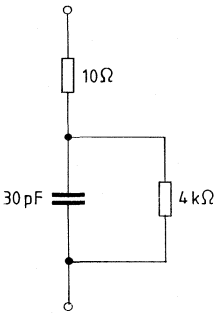


Smith diagram

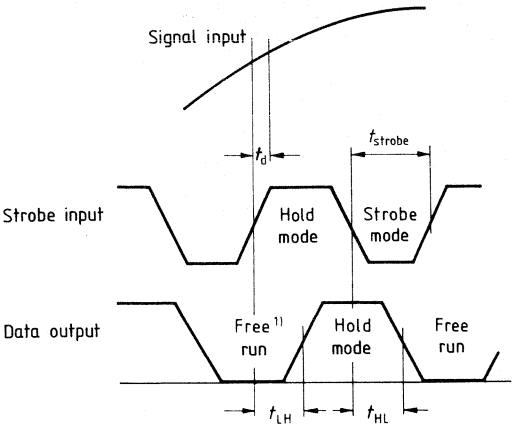
a) Nyquist plot of input impedance
b) Nyquist plot of equivalent circuit



Equivalent circuit

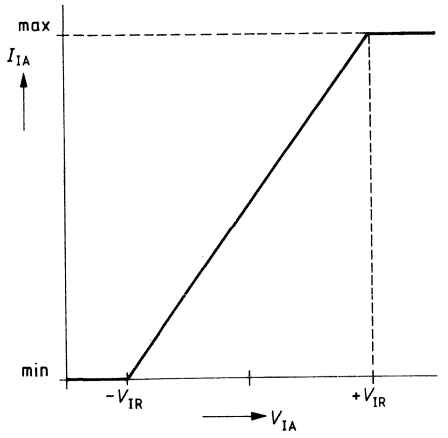


Pulse diagram of strobe input and data outputs

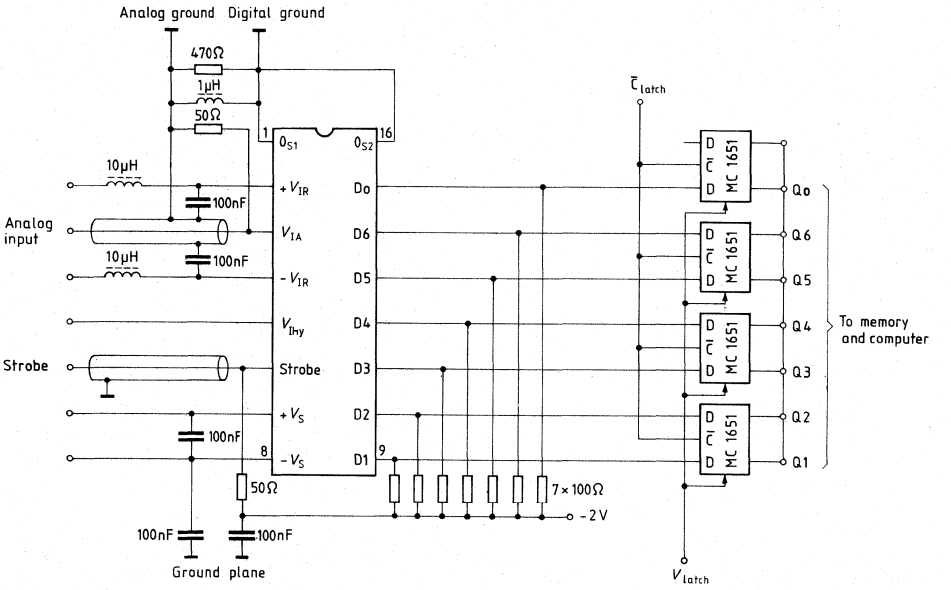


1) undefined output levels

Input current versus input voltage



Measurement circuit



Preliminary data **Bipolar IC**

Type	Ordering code	Package	Fig. No.
SDA 5200 N	Q67000-A2242	DIC 16	9

The SDA 5200 N is an ultrafast A/D converter with 6 bit resolution and overflow output. After cascading, it enables straightforward construction of 7 or 8 bit A/D converters, respecitively (refer to application circuit).

Apart from a guaranteed strobe frequency of 100 MHz and an excellent linearity, the SDA 5200 N is outstanding for a broad analog bandwidth which – from the analog side – enables application up to the limit of the Nyquist theorem.

The SDA 5200 N is pin-compatible to the ICs SDA 5010, SDA 6020, and SDA 5200 S (differing output code in the overflow).

Features

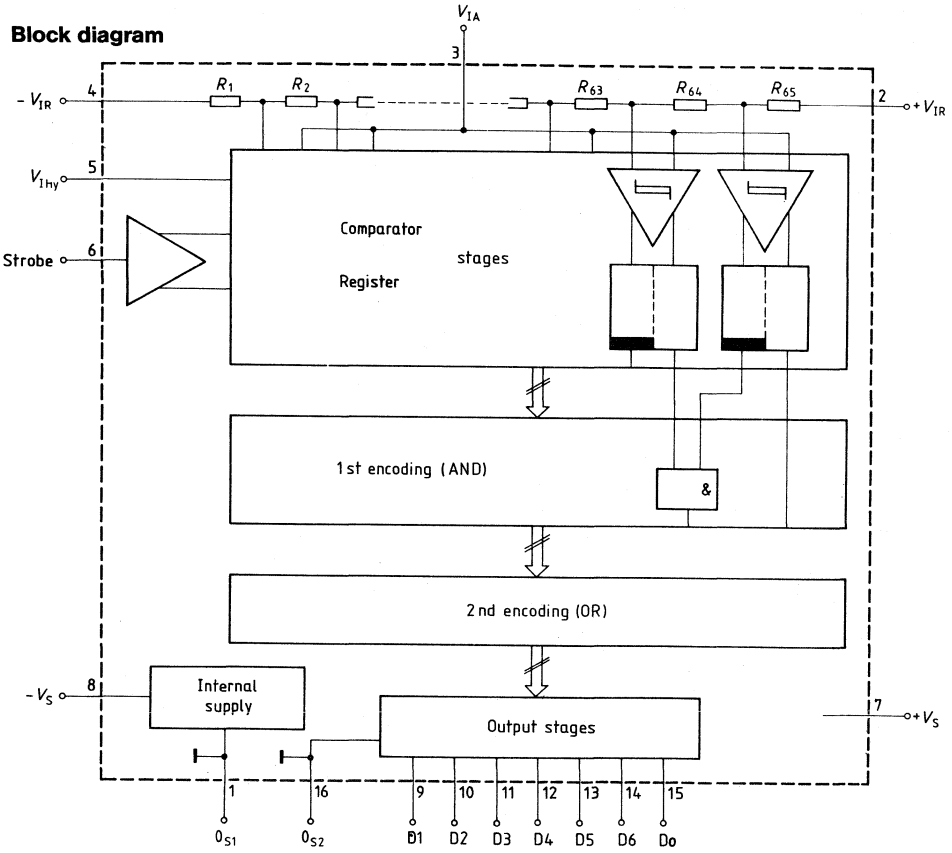
- Strobe frequency 100 MHz
- 6 bit resolution (1.6%)
- Overflow output (7th bit) at simultaneous blocking of the remaining outputs → simple cascading for 7 bit or 8 bit A/D converters
- Broad analog bandwidth (140 MHz)
- High slew rate of the input stages (typ. 0.5 V/ns)
- Processing of analog signals up to the Nyquist limit
- Linearity ± 1/4 LSB
- No sample and hold required
- Dynamic driving of reference inputs for analog addition and multiplication
- Power dissipation 550 mW
- ECL compatible
- Logic-compatible supply voltage +5 V; −5.2 V

The following versions[1] are available upon request:

- IC with a nonlinear conversion characteristic of a given characteristic curve
- IC with any output code (e.g. gray code)

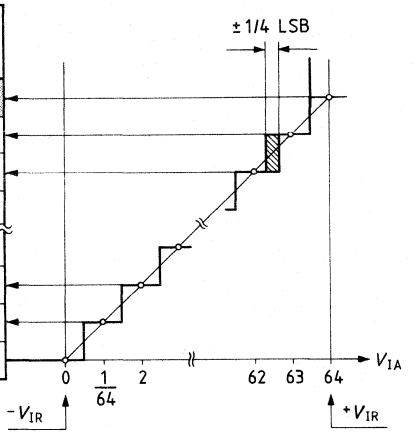
1) Conditions upon request.

Block diagram



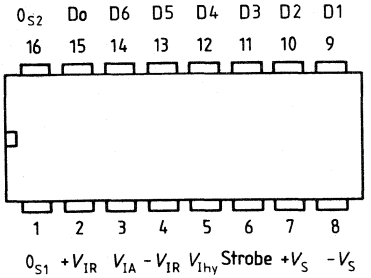
Transfer characteristic and truth table

Do	D6	D5	D4	D3	D2	D1
H	L	L	L	L	L	L
L	H	H	H	H	H	H
L	H	H	H	H	H	L
≈	≈	≈	≈	≈	≈	≈
L	L	L	L	L	H	L
L	L	L	L	L	L	H
L	L	L	L	L	L	L



Pin configuration

top view



Pin No.	Symbol	Function
1	0_{S1}	Digital ground 1
2	$+V_{IR}$	Positive reference voltage (+2 V)
3	V_{IA}	Analog signal input (max. +2 V; −3 V)
4	$-V_{IR}$	Negative reference voltage (−3 V)
5	V_{Ihy}	Hysteresis control (9 V to +2.5 V)
6	Strobe	Strobe input (ECL)
7	$+V_S$	Positive supply voltage (+5 V)
8	$-V_S$	Negative supply voltage (−5.2 V)
9 to 14	D1 to D6	Data outputs, bits 1 to 6 (ECL)
15	Do	Overflow output
16	0_{S2}	Digital ground 2

Maximum ratings

		Lower limit B	Upper limit A	
Supply voltage	$+V_S$	−0.3	6.0	V
Supply voltage	$-V_S$	−6.0	0.3	V
Input voltages	$V_{IA}, +V_{IR}, -V_{IR}$	−3.5	2.5	V
Strobe	V_{strobe}	$-V_S$	0	V
Hysteresis control	V_{Ihy}	0	3.0	V
Voltage difference	$0_{S1} - 0_{S2}$	−0.5	0.5	V
Operating temperature	T_{amb}	0	70	°C
Junction temperature	I_j		125	°C
Storage temperature	T_{stg}	−55	125	°C
Thermal resistance (system-air)	$R_{th\,SA}$		85	K/W

Characteristics

Power supply

		Lower limit B	typ	Upper limit A	
Pos. supply voltage	$+V_S$	4.5	5.0	5.5	V
Neg. supply voltage	$-V_S$	−5.7	−5.2	−4.7	V
Current consumption					
at $+V_S = +5.0$ V, $V_{IA} \leqq -V_{IR}$	I_{S+}		50	80	mA
at $-V_S = -5.2$ V, $V_{IA} \leqq -V_{IR}$	I_{S-}		55	80	mA

Analog section

Signal input

Max. input voltage	V_{IAmax}	$-V_{IRmin}$		$+V_{IRmax}$	V
$V_{IRmax} = \lvert(+V_{IRmax}) - (-V_{IRmin})\rvert$				5	V
V_{IA} for 6 bit resolution			0.3		V
V_{IA} for 1/2 LSB linearity		1.2	0.6		V
V_{IA} for 1/4 LSB linearity		2.4	1.2		V
Input current					
at $V_{IA} = +V_{IR}$	I_{IA}		150	500	µA
at $V_{IA} < -V_{IR}$	I_{IA}	−500		500	nA
Input capacitance					
at $V_{IA} < -V_{IR}$	C_{IA}		25		pF

Reference inputs

Pos. reference voltage	$+V_{IR}$	−2.5		2	V
Neg. reference voltage	$-V_{IR}$	−3.0		1.5	V
Reference resistance	R_{ref}	96	128	195	Ω

Digital section

Strobe input

H input voltage	V_{IH}	−1.1	−0.9	−0.6	V
L input voltage	V_{IL}	−2.0	−1.7	−1.6	V
H input current	I_{IH}		6	50	µA
L-input current	I_{IL}		6	50	µA

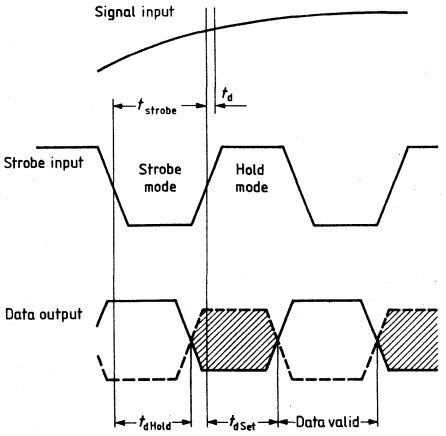
Data outputs (100 Ω to −2 V)

H output voltage	V_{QH}	−1.1	−0.9	−0.7	V
L output voltage	V_{QL}	−2.0	−1.7	−1.5	V

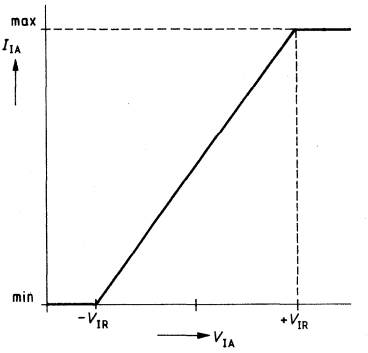
Characteristics (cont'd)

Dynamic parameters		Lower limit B	typ	Upper limit A	
Aperture time	t_d		2		ns
Aperture jitter			25		ps
Strobe	t_{strobe}		5		ns
Signal transition time	$t_{d\,Hold}$		12	17	ns
Signal transition time	$t_{d\,Set}$		12	17	ns
Strobe frequency	f_{strobe}	100			MHz
Max. slew rate			0.5		V/ns
bandwidth (−3 dB)	B		140		MHz

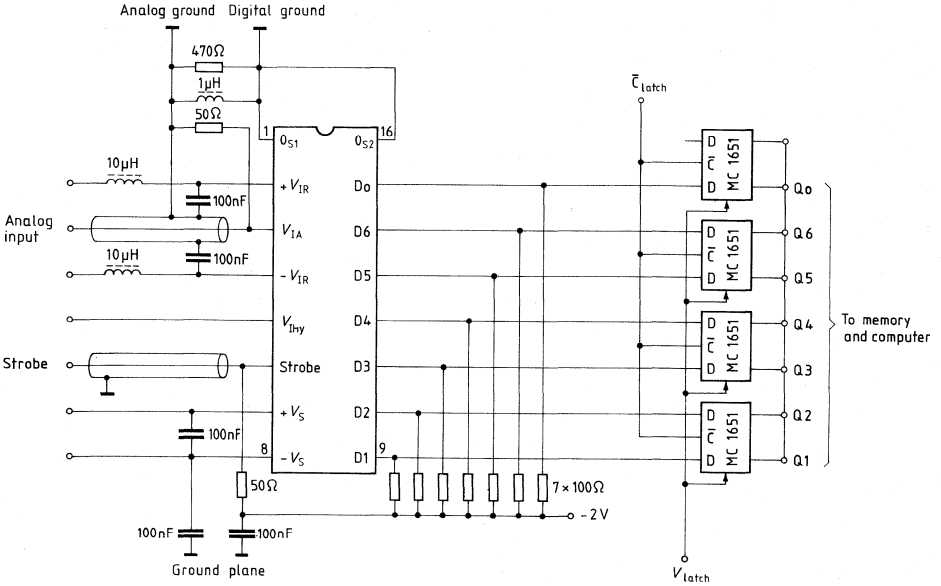
Pulse diagram of strobe input and data outputs



Input current versus input voltage

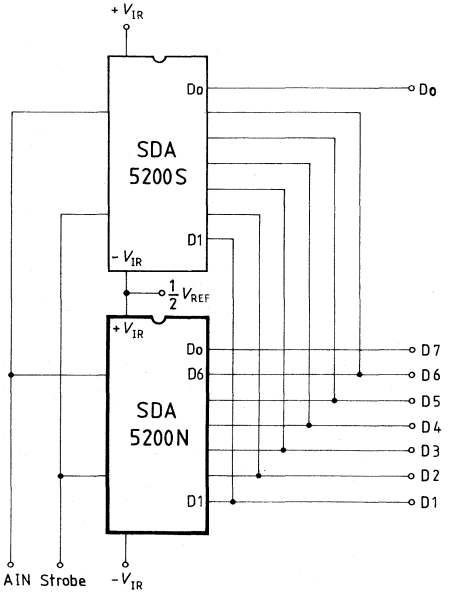


Test circuit



Application circuit

7 bit A/D converter with SDA 5200 S and SDA 5200 N



Preliminary data **Bipolar IC**

Type	Ordering code	Package	Fig. No.
SDA 5200 S	Q67000-A2243	DIC 16	9

The SDA 5200 S is an ultrafast 6 bit A/D converter with overflow output. It has been designed as terminating device for a 7 bit or 8 bit A/D converter comprising several cascaded ICs (refer to application circuit), or exclusively for 6 bit operation.

Apart from a guaranteed strobe frequency of 100 MHz and an excellent linearity, the SDA 5200 S is outstanding for a broad analog bandwidth which – from the analog side – enables application up to the limit of the Nyquist theorem.

The SDA 5200 S is pin-compatible to the ICs SDA 5010, SDA 6020, and SDA 5200 N (differing output code in the overflow).

Features

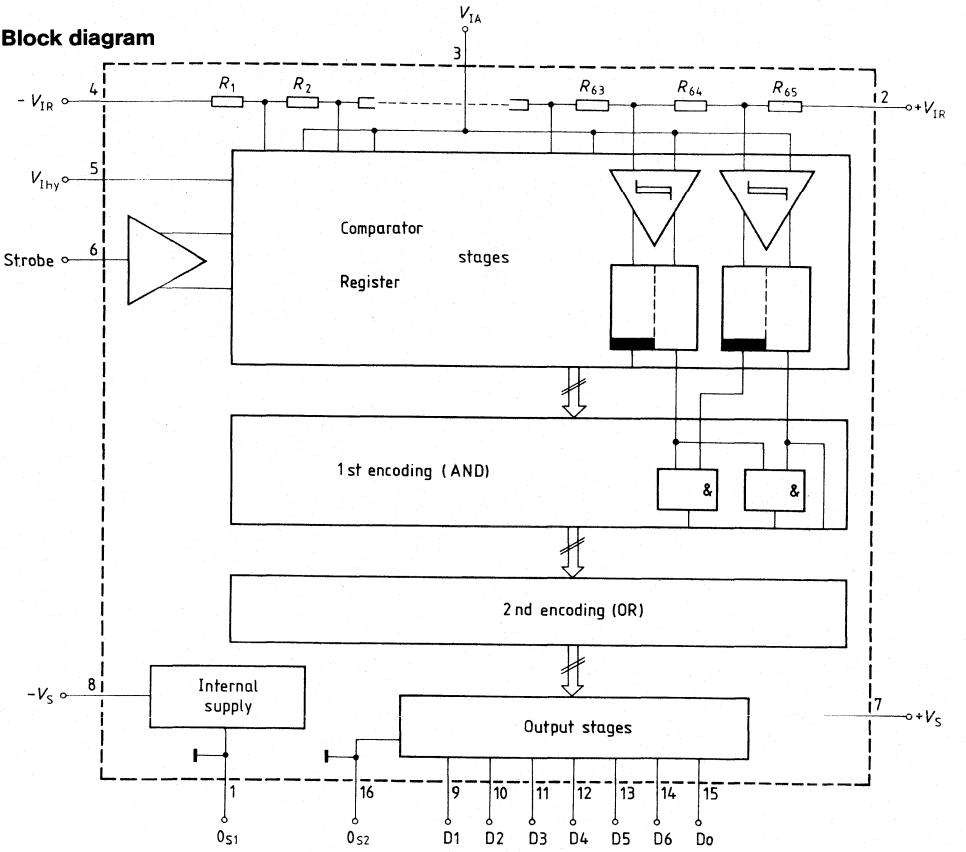
- Strobe frequency 100 MHz
- 6 bit resolution (1.6%)
- Overflow output (7th bit)
- Broad analog bandwidth (140 MHz)
- High slew rate of the input stages (typ. 0.5 V/ns)
- Processing of analog signals up to the Nyquist limit
- Linearity ± 1/4 LSB
- No sample and hold required
- Dynamic driving of reference inputs for analog addition and multiplication
- Power dissipation 550 mW
- ECL compatible
- Logic-compatible supply voltage +5 V; −5.2 V

The following versions[1] are available upon request:

- IC with a nonlinear conversion characteristic of a given characteristic curve
- IC with any output code (e.g. gray code)

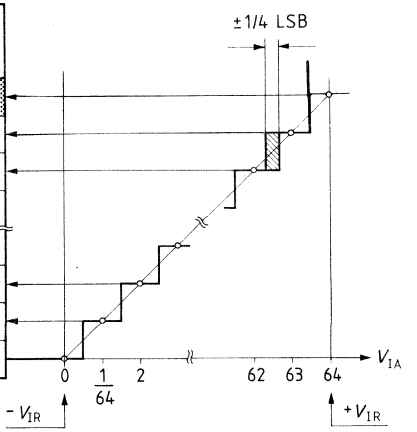
1) Conditions upon request.

Block diagram

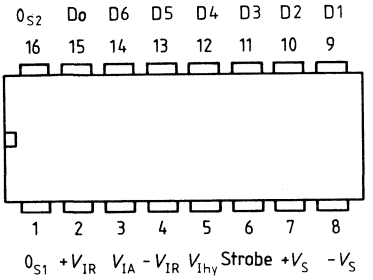


Transfer characteristic and truth table

Do	D6	D5	D4	D3	D2	D1
H	H	H	H	H	H	H
L	H	H	H	H	H	H
L	H	H	H	H	H	L
L	L	L	L	L	H	L
L	L	L	L	L	L	H
L	L	L	L	L	L	L



Pin configuration
top view



Pin No.	Symbol	Function
1	0_{S1}	Digital ground 1
2	$+V_{IR}$	Positive reference voltage (+2 V)
3	V_{IA}	Analog signal input (max. +2 V; −3 V)
4	$-V_{IR}$	Negative reference voltage (−3 V)
5	V_{Ihy}	Hysteresis control (9 V to +2.5 V)
6	Strobe	Strobe input (ECL)
7	$+V_S$	Positive supply voltage (+5 V)
8	$-V_S$	Negative supply voltage (−5.2 V)
9 to 14	D1 to D6	Data outputs, bits 1 to 6 (ECL)
15	Do	Overflow output
16	0_{S2}	Digital ground 2

Maximum ratings

		Lower limit B	Upper limit A	
Supply voltage	$+V_S$	−0.3	6.0	V
Supply voltage	$-V_S$	−6.0	0.3	V
Input voltages	$V_{IA}, +V_{IR}, -V_{IR}$	−3.5	2.5	V
Strobe	V_{strobe}	$-V_S$	0	V
Hysteresis control	V_{Ihy}	0	3.0	V
Voltage difference	$0_{S1} - 0_{S2}$	−0.5	0.5	V
Operating temperature	T_{amb}	0	70	°C
Junction temperature	I_j		125	°C
Storage temperature	T_{stg}	−55	125	°C
Thermal resistance (system-air)	$R_{th\,SA}$		85	K/W

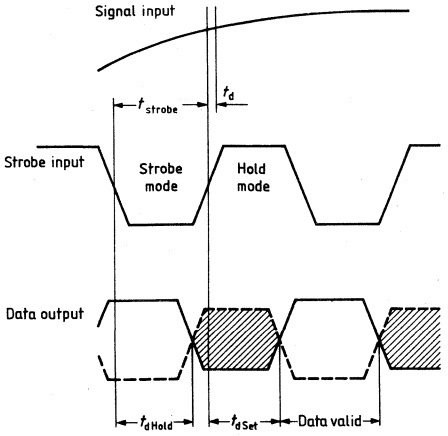
Characteristics

		Lower limit B	typ	Upper limit A	
Power supply					
Pos. supply voltage	$+V_S$	4.5	5.0	5.5	V
Neg. supply voltage	$-V_S$	−5.7	−5.2	−4.7	V
Current consumption					
at $+V_S = +5.0$ V, $V_{IA} \leqq -V_{IR}$	I_{S+}		50	80	mA
at $-V_S = -5.2$ V, $V_{IA} \leqq -V_{IR}$	I_{S-}		55	80	mA
Analog section					
Signal input					
Max. input voltage	V_{IAmax}	$-V_{IRmin}$		$+V_{IRmax}$	V
$V_{IRmax} = \lvert(+V_{IRmax}) - (-V_{IRmin})\rvert$				5	V
V_{IA} for 6 bit resolution			0.3		V
V_{IA} for 1/2 LSB linearity		1.2	0.6		V
V_{IA} for 1/4 LSB linearity		2.4	1.2		V
Input current					
at $V_{IA} = +V_{IR}$	I_{IA}		150	500	µA
at $V_{IA} < -V_{IR}$	I_{IA}	−500		500	nA
Input capacitance					
at $V_{IA} < -V_{IR}$	C_{IA}		25		pF
Reference inputs					
Pos. reference voltage	$+V_{IR}$	−2.5		2	V
Neg. reference voltage	$-V_{IR}$	−3.0		1.5	V
Reference resistance	R_{ref}	96	128	195	Ω
Digital section					
Strobe input					
H input voltage	V_{IH}	−1.1	−0.9	−0.6	V
L input voltage	V_{IL}	−2.0	−1.7	−1.6	V
H input current	I_{IH}		6	50	µA
L-input current	I_{IL}		6	50	µA
Data outputs (100 Ω to −2 V)					
H output voltage	V_{QH}	−1.1	−0.9	−0.7	V
L output voltage	V_{QL}	−2.0	−1.7	−1.5	V

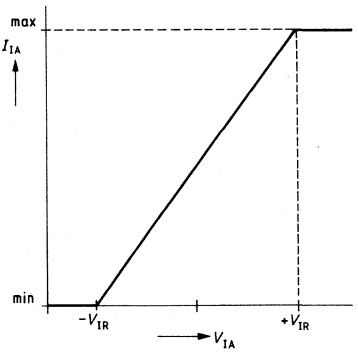
Characteristics (cont'd)

		Lower limit B	typ	Upper limit A	
Dynamic parameters					
Aperture time	t_d		2		ns
Aperture jitter			25		ps
Strobe	t_{strobe}		5		ns
Signal transition time	$t_{d\,Hold}$		12	17	ns
Signal transition time	$t_{d\,Set}$		12	17	ns
Strobe frequency	f_{strobe}	100			MHz
Max. slew rate			0.5		V/ns
bandwidth (–3 dB)	B		140		MHz

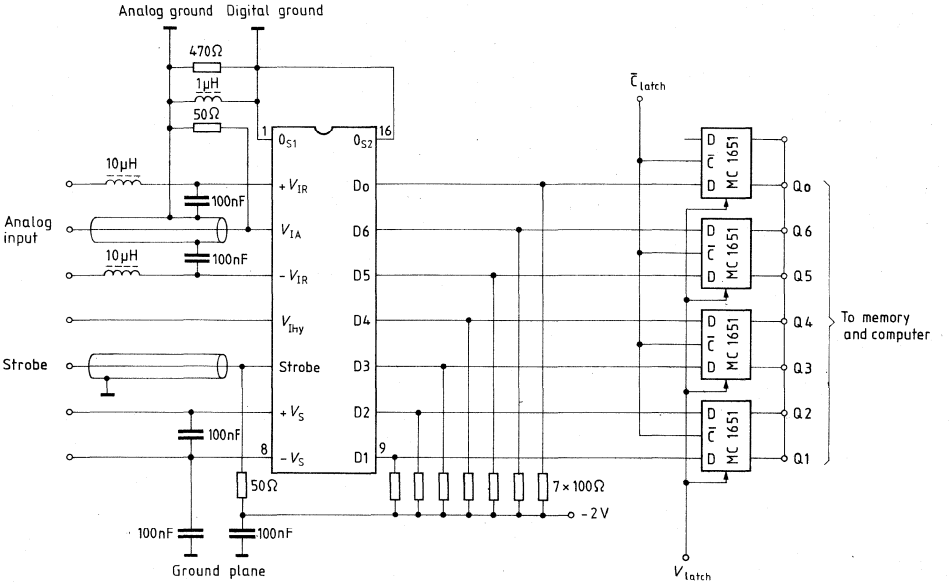
Pulse diagram of strobe input and data outputs



Input current versus input voltage

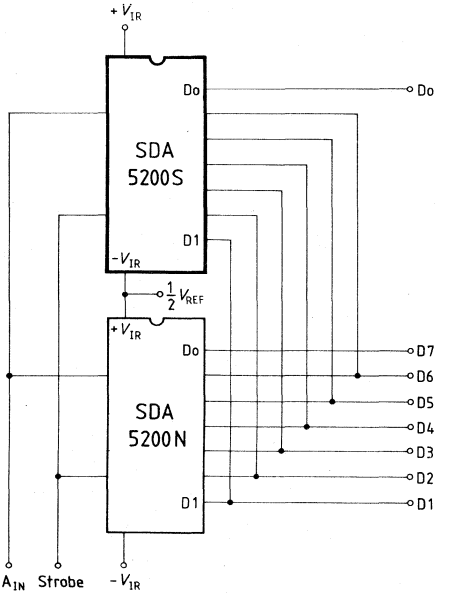


Test circuit



Application circuit

7 bit A/D converter with SDA 5200 S and SDA 5200 N



Timer ICs

Programmable Digital Timer

SAB 0529
SAB 0529 G

Bipolar IC

Type	Ordering code	Package	Fig. No.
SAB 0529	Q67000-H2176	DIP 18	11
SAB 0529 G	Q67000-H2952	SO 20	28

With the digital timer SAB 0529, delay times between 1 second and 31 1/2 hours can be set. Time base is the 50 Hz line frequency. A triac may be triggered by the SAB 0529 IC.

The SAB 0529 can be programmed to two operating modes: "momentary switching" and "switch-off delay" (according to DIN 46120). In the first mode, a rising edge at the start input activates the triac and starts the timing period. In the switch-off delay mode, the rising edge at the start input activates the triac; but the falling edge starts the timing period.

The versatile IC SAB 0529 covers a great variety of applications, e.g. electronic timers, cooking equipment control, espresso machines, hand-driers, coin changing machines and slot machines, stairwell-light time switches, industrial controls, developing systems for photographic labs, automatic starters (to preheat car engines), and operating-hours counters.

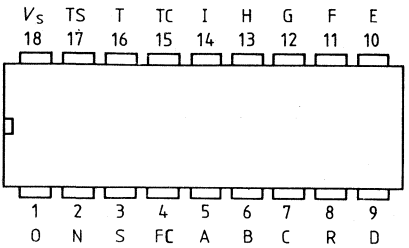
Features

- Direct operation from ac line or dc supply possible
- Time base is 50 Hz line frequency
- Triac triggering with voltage synchronization for resistive loads, or with current synchronization for inductive and capacitive loads
- Triac gate trigger current up to 100 mA
- Continuous output current to relay actuation max. 100 mA
- 8 overlapping timing periods between 1 second and 31 1/2 hours (at 50 Hz)
- 2 operating modes: momentary switching or switch-off delay, both are retriggerable
- Upon request, delay times can be tailored to customer's specification, requiring only minimum external components. This is possible through mask programming, but is based on minimum order quantities.

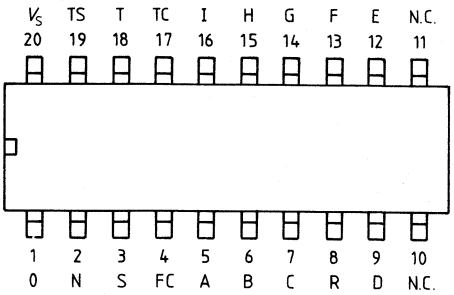
Pin configuration

top view

SAB 0529



SAB 0529 G

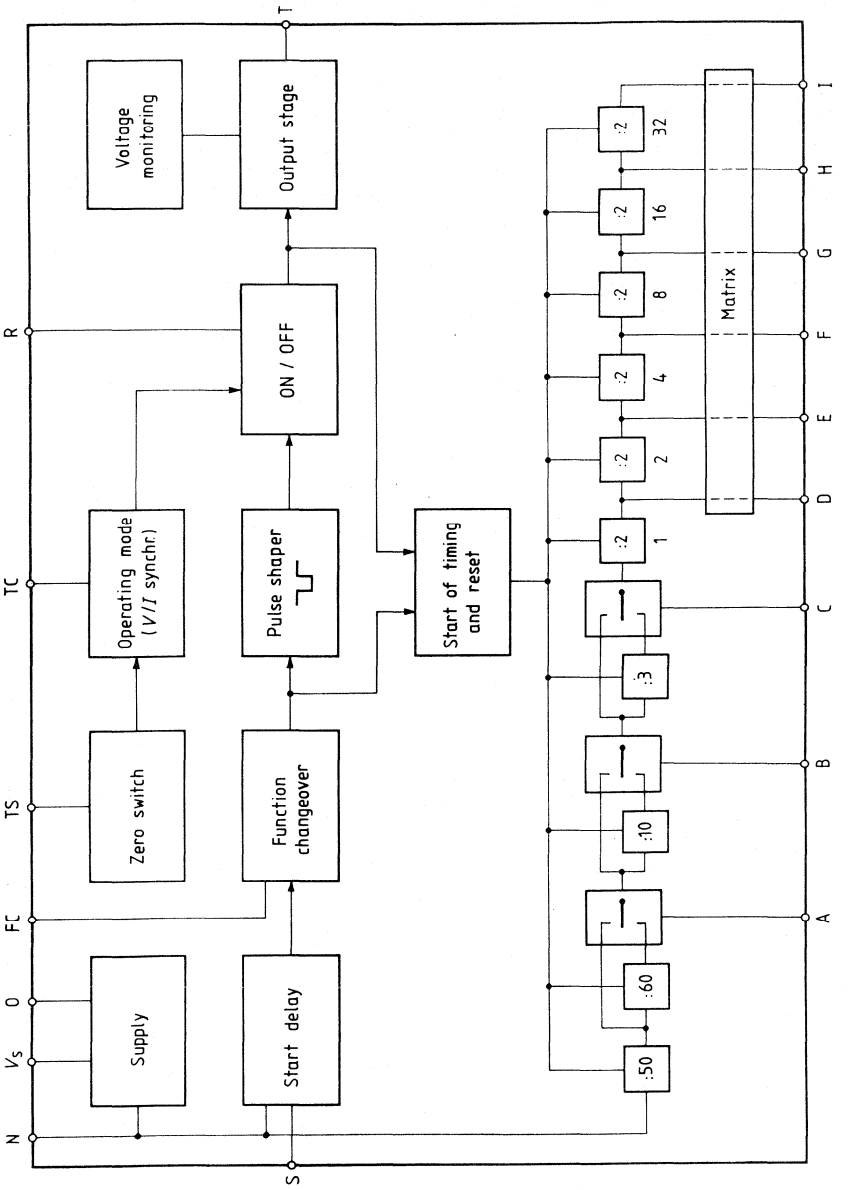


Pin No. SAB 0529	Pin No. SAB 0529G	Symbol	Function
1	1	0	Circuit ground
2	2	N	Line voltage via series resistor
3	3	S	Start
4	4	FC	Function changeover
5	5	A	Programming of basic timing unit
6	6	B	Programming of basic timing unit
7	7	C	Programming of basic timing unit
8	8	R	Reset
9	9	D	Basic timing unit x 1
10	12	E	Basic timing unit x 2
11	13	F	Basic timing unit x 4
12	14	G	Basic timing unit x 8
13	15	H	Basic timing unit x 16
14	16	I	Basic timing unit x 32
15	17	TC	Triac operation mode setting
16	18	T	Triac triggering
17	19	TS	Triac synchronization
18	20	V_S	Positive supply voltage

These values apply to the standard SAB 0529 version. By mask programming, each of those pins may be assigned a value between 1 and 63.

With the SO 20 package (SAB 0529 G), pins 10 and 11 are not connected.

Block diagram



Functional description

Through division of the line frequency into the portions 1:50, 1:60, 1:10, and 1:3, the basis for 8 timing periods is created. The timing period is selected via inputs A, B, and C, according to the following truth table.

Timing range	A	B	C	Basic timing unit	Max. time at 50 Hz line	
1	L	L	L	1 s	63 s	(approx. 1 min)
2	L	L	H	3 s	189 s	(approx. 3 min)
3	L	H	L	10 s	630 s	(10.5 min)
4	L	H	H	30 s	1890 s	(31.5 min)
5	H	L	L	1 min	63 min	(approx. 1 hr)
6	H	L	H	3 min	189 min	(approx. 3 hrs)
7	H	H	L	10 min	630 min	(10.5 hrs)
8	H	H	H	30 min	1890 min	(31.5 hrs)

L and H potentials are referred to terminal 0, e.g. L = 0, H = V_S

The time basis of the set period is multiplied by the corresponding value in the flipflops 1, 2, 4, 8, 16, 32.

The delay time at output T results from connecting a terminal between D and I with terminal R. Should several of the pins D to I be connected to R, the corresponding delay times are added.

Example

Line frequency = 50 Hz; set range 1 (basic timing unit = 1 s); D, F, and I are connected to R (value 37): resulting delay time is 37 seconds.

Mask programming of matrix

Upon request – however, based on a minimum order quantity (of 50,000 items) – assigning any value between 1 and 63 to each pin from D to I in the matrix is possible by mask programming. Thus, individual delay times tailored to the applications are available at those pins, and can be selected by means of a simple multiposition switch.

In such a case, however, it is no longer possible to add delay times when several pins between D and I are connected to R.

Example

Delay times of 3 s, 6 s, 9 s, 12 s, 15 s, and 18 s, at 50 Hz line frequency are required.

With the standard SAB 0529 version the following connections would have to be established (e.g. by a coding switch).

Timing period 2, basic timing unit 3 s: A, B on L potential, C on H potential

3 s: D – R
6 s: E – R
9 s: D – E – R
12 s: F – R
15 s: D – F – R
18 s: E – F – R

Mask programming would establish the necessary connection between pin D and I internally in the matrix, so a simple multiposition switch can select by delay times and connect them to R.

Timing period 2, basic timing unit 3 s: A, B on L potential, C on H potential
e.g. 3 s: D – R
6 s: E – R
9 s: F – R
12 s: G – R
15 s: H – R
18 s: I – R

Reset during a timing period is accomplished by interrupting the connection to *R*, or by applying an H potential to R (in the latter case a protective resistor between R and D through I is necessary as those pins are not protected against short circuit to V_S), or by turning on and off V_S.

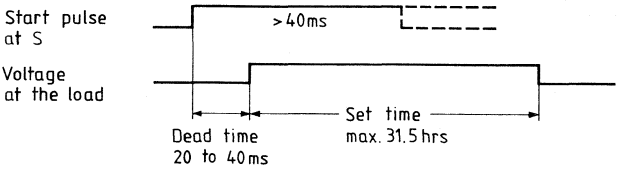
Application note

If R is connected to one of the pins D through I via a multiposition switch, and if during the changeover a reset of the timing period is to be avoided, a suitable capacitor is required between R and 0.

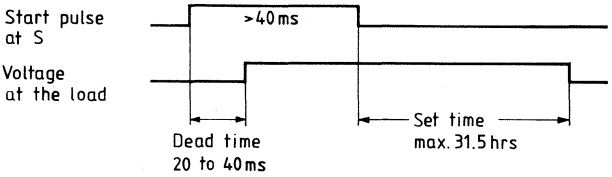
With the **connection of the supply voltage,** the circuit is automatically reset. A timing period does not commence if 0 potential is applied to S.

The SAB 0529 allows two operation modes which are set through pin FC (function changeover):

1. the **"momentary switching function"** in accordance with DIN 46120
   The triac at pin T turns on with the rising edge at the start input S and turns off when the set time has passed, independent of the start pulse length.



2. the **"switch-off delay"** in accordance with DIN 46120
   The triac turns on with the rising edge at S. The falling edge at S starts the timing period. The triac remains in on-state until the set period has passed.



To protect the start input S against external interference and contact bounce, it has a **dead time** of between 20 and 40 ms for its positive switching edge, depending on the phase of the 50-Hz line.

Both operation modes are **retriggerable** during the timing period.

Function changeover

FC	Function
L	momentary switching
H	switch-off delay

Triac stage

Pin TS (triac synchronization) is the input of a zero voltage switch and serves to synchronize the output T (open collector) with the load voltage or the load current.

With $V_S < 3$ V, the output current is disconnected.

The input TC has a double function:

- to change TS over to voltage synchronization
- to adjust the triac trigger pulse width (by connecting a capacitor C_e to TC) in case of current synchronization.

Three operation modes are possible by varying the connection of the pins TC and/or TS:

Operation mode 1

TC to V_S: Output T is connected to the zero voltage switch. T operates when $V_S - 1.3\ V \leq V_{TS} \leq V_S + 1.3\ V$.

Is utilized in case of voltage synchronization; see application circuit 1 (operation with resistive loads) and pulse diagram.

Operation mode 2

TC via C_e to Q: Output T is connected to the zero voltage switch via a monoflop. If $V_S - 1.3$ V is fallen below or $V_S + 1.3$ V exceeded at TS, the output T releases a triac gate trigger pulse determined by C_e.

Is utilized in case of current synchronization; see application circuit 2 and pulse diagram.

Operation mode 3

TC and TS to V_S: Output T conducts after release of start pulse.

Is utilized for any load in case of continuous triac triggering (e.g. low performance), or if any other load is to be operated instead of the triac (see application circuits 3, 4, 5).

Operation with line voltage

A series resistor R_s and a charging capacitor C_{ch} serve for line voltage supply. If a diode is connected in series with R_s (anode to N), the rms current consumption is halved. The series resistor may also be an *RC* combination (see application circuit 6).

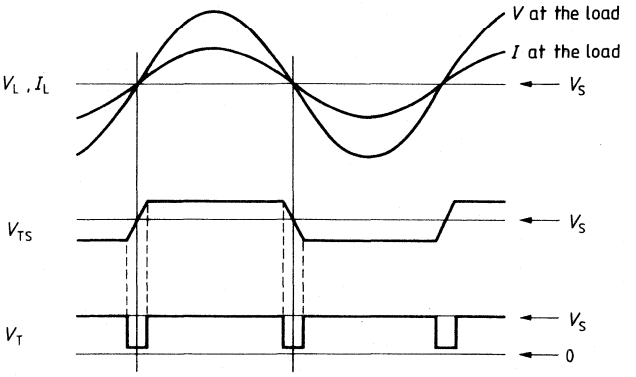
Operation with dc voltage

This IC can also be operated with dc voltage or current (see application circuits 4 and 5).

Pulse diagrams for triac operation modes 1 and 2

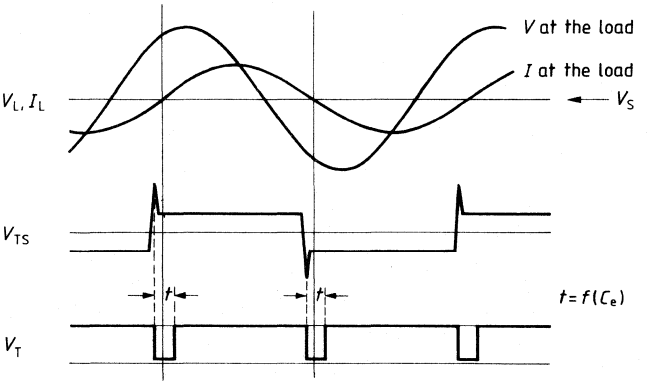
Operation mode 1

Voltage synchronization with resistive loads (TC to V_S)



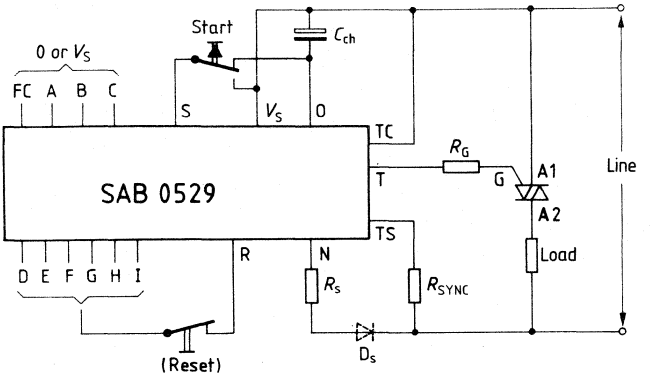
Operation mode 2

Current synchronization with nonresistive loads (capacitance C_e to TC)

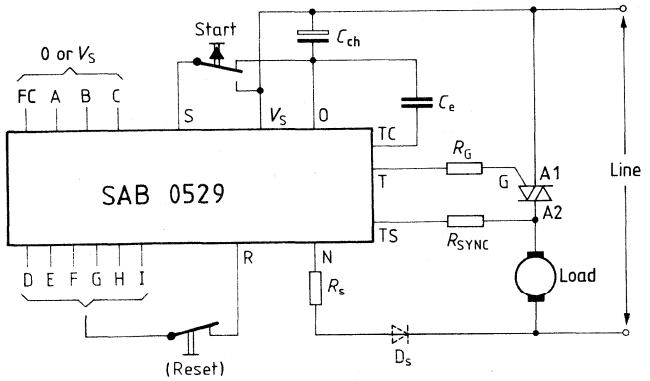


Application circuits

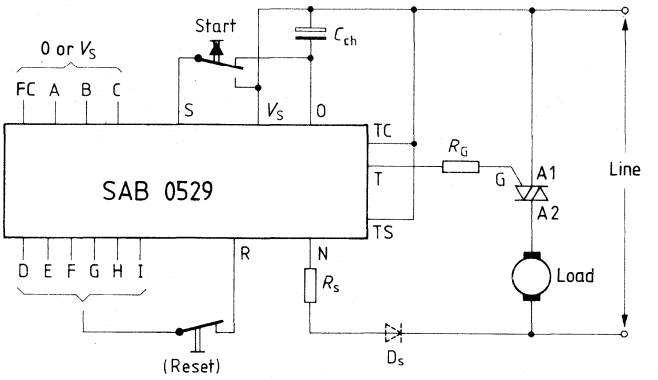
1. Operation with resistive loads



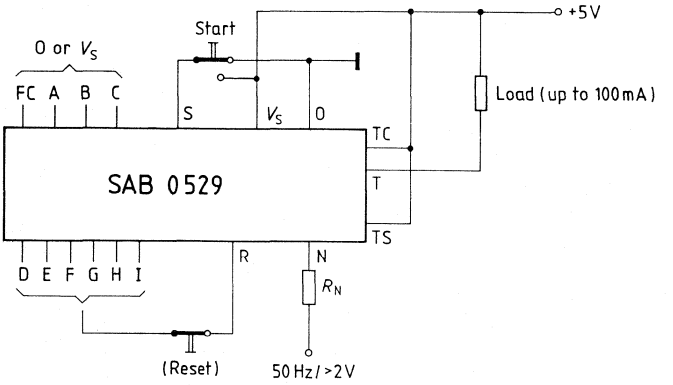
2. Operation with resistive, capacitive, or inductive loads



3. Operation with any load and continuous triac triggering

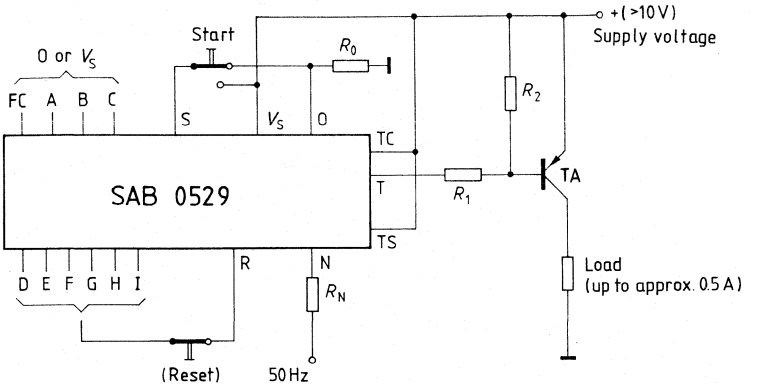


4. Operation with 5 V dc voltage



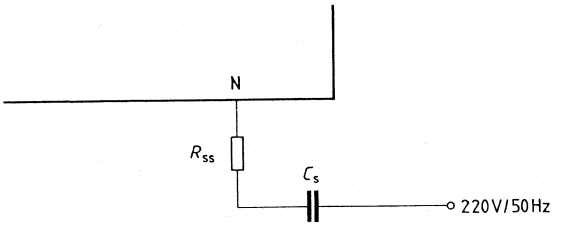
Note: The diode D in application circuits 1 to 3 must not necessarily be used. This diode, however, may halve the power dissipation at R_s.

5. Operation with dc voltage > 10 V (limited only by transistor TA)



6. Operation with capacitive series resistor

In the application circuits 1 to 3, a series connection of R and C may be utilized instead of R_S or R_S and D.



Note: If not required, the reset key may be omitted in application circuits 1 to 5.

Dimensioning the application circuits

The following formulae give reference values for operation with sine-shaped ac voltages of 50 Hz. The triac is always triggered in the 2nd and 4th quadrant (negative gate trigger current).

Trigger pulse length Z: $Z = \frac{\text{5 x holding current}}{\text{rms load current}}$ (ms); applies to $Z \leq 1$ ms

$$R_G = \frac{V_S - V_{ATL} - \text{gate trigger voltage}}{\text{gate trigger current}}$$

$$R_s = \frac{\text{0.5 x rms line voltage} - V_S}{I_S + \text{average gate trigger current}}$$ (with or without diode D)

average gate trigger current = gate trigger current x $\frac{Z}{10}$ (Z in ms)

Power dissipation at R_s:

$$\text{(without diode D)} = \frac{(\text{rms line voltage})^2}{R_s}$$

$$\text{(with diode D)} = 0.5 \text{ x } \frac{(\text{rms line voltage})^2}{R_s}$$

$$C_{ch} = 20 \text{ x } \frac{\text{rms line voltage}}{R_s}$$ (µF, V, kΩ)

(residual ac voltage at $V_{Spp} \leq 0.5$ V)

Note for C_{ch}

If short-term line failures are to be compensated, C_{ch} has to be accordingly larger (approx. 1000 µF for ≤ 5 s line failure).

Application circuit 1 (voltage sychronization for resistive load)

$$R_{SYNC} = \frac{\text{0.22 } Z \text{ x rms line voltage} - 1.3}{0.04} \geq \frac{\text{peak line voltage}}{4}$$ (kΩ, V, mA, ms)

Notes for application circuit 1

An average I_{TS} of 0.04 mA was inserted into the formula approximating R_{SYNC}.

As $I_{TS}+$ and $I_{TS}-$ contain production deviations, utilizing the determined R_{SYNC} requires certain tolerances to be taken into account for pulse length Z.

To minimize the effect of these tolerances, a resistor may be connected between V_S and TS, which generates a constant current of $\frac{V_{TS}}{R}$ to be added to I_{TS}.

However, a TC of −4 mV/K should be noted for V_{TS}.

Application circuit 2 (current synchronization)

$C_e = 22 \times Z$ (nF, ms)

$$R_{SYNC} \geq \frac{\text{max. on-state voltage} - 1.3}{I_{TSmin}}$$

$$R_{SYNC} \geq \frac{\text{peak line voltage}}{4}$$

} The largest value applies (kΩ, V, mA)

$$R_{SYNC} \leq \frac{\text{gate trigger voltage} - 1.3}{I_{TSmax}} \quad \text{(kΩ, V, mA)}$$

Notes for application circuit 2

In this circuit, an even shorter pulse length than determined for Z is sufficient to trigger the triac. This is possible by the trigger pulse being automatically repeated until the holding current is reached. Overdimensioning of Z for safety reasons is, therefore, not necessary. The disadvantage of multiple trigger pulses, however, is a somewhat larger interference band during the triggering.

The interference band and/or the interference amplitude generated also depend on the amount of the gate trigger voltage necessary to trigger the triac after each current zero passage. That voltage is determined by the size of R_{SYNC} and should not exceed 20 V.

Application circuit 3

Dimensioning of R_s, R_G, and C_{ch} as described at the beginning of this section.

Application circuit 4

$R_N \approx 20 \times$ ac voltage (50 Hz) (kΩ, V rms)

Application circuit 5

R_N see above. The ac voltage for the timing base must be greater than (supply voltage −4.8 V).

$$R_0 = \frac{\text{supply voltage} - 6.8\ \text{V}}{I_S + I_{R1}} \qquad I_{R1} = I_{B(TA)} + I_{R2}$$

$$R_1 = \frac{6.8\ \text{V} - V_{QTL} - V_{B(TA)}}{I_{R1}} \qquad I_{R2} \approx 0.05\ I_{B(TA)}$$

$$R_2 = \frac{V_{B(TA)}}{I_{R2}}$$

Application circuit 6

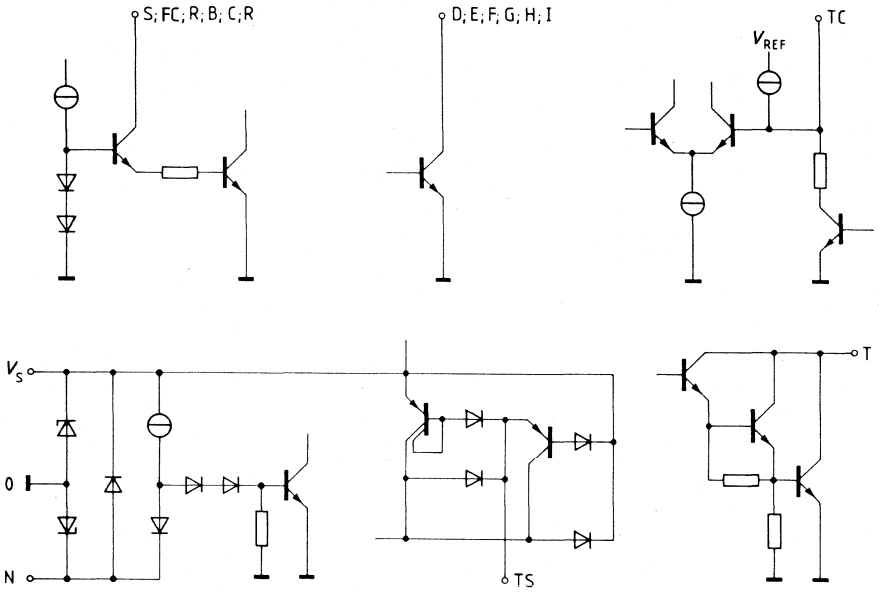
$$C_s = \frac{3.5}{R_s}\ (\mu\text{F, k}\Omega)$$

$$R_{ss} = 0.2\ R_s$$

} applies to 50 Hz

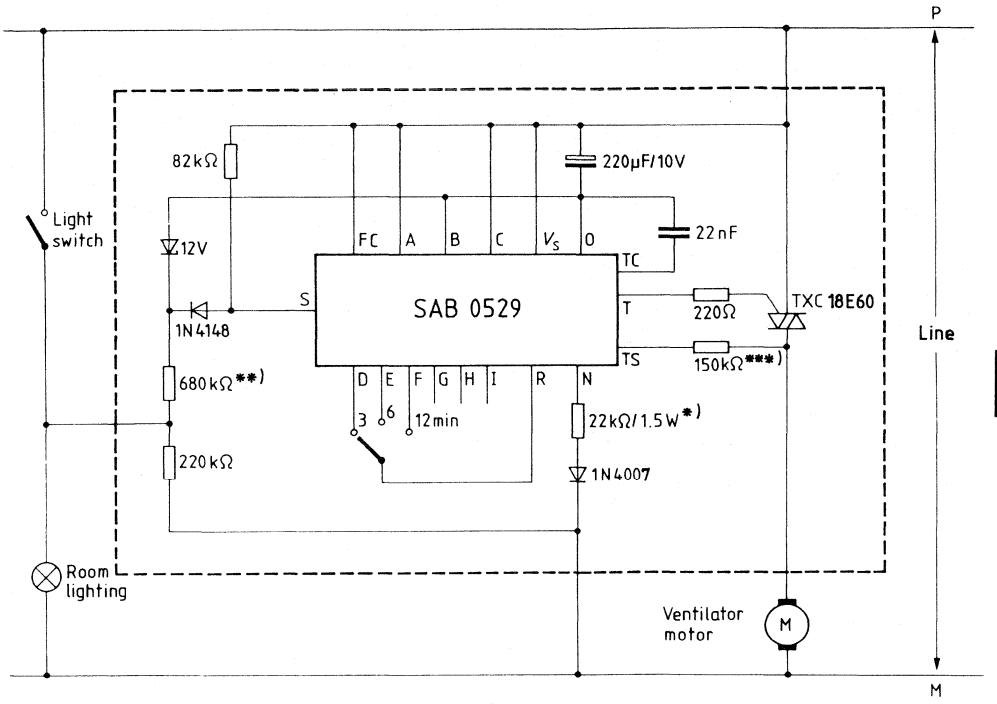
To limit the inrush current, R_{ss} has to be $\geq 0.2\ R_s$. Otherwise, the circuit may be damaged.

Internal connection of inputs, outputs, and supply pins



Typical application

Time control for ventilator motor, adjustable to 3, 6, or 12 minutes' ventilation



*) for 220 Vac, 10 kΩ for 110 Vac;
**) for 220 Vac, 330 kΩ for 110 Vac;
***) for 220 Vac, 82 kΩ for 110 Vac;
} (high-voltage proof)

Maximum ratings

		Lower limit B	Upper limit A		Notes
Supply voltage at impressed dc voltage	V_S	−0.3	5.5	V	
Peak current at N	I_{Np}	−35	35	mA	50 Hz operation
DC voltage from N (rms)	$-I_{Nrms}$		12.5	mA	with $V_S \leq 7.5$ V
AC at N with impressed current	I_{Nrms}		25	mA	50 Hz operation with $V_S \leq 7.5$ V
Voltage at S, FC, A, B, C, R	V	−0.3	7.5	V	
Voltage at N, with N utilized as clock input	V_{NT}	−0.3	V_S	V	
Voltage at TC	V_{TC}	−0.3	V_S	V	
Current at TS	I_{TS}	−4	4	mA	
Voltage at T	V_T	−0.3	7.5	V	
Peak current in T	I_{Tp}		150	mA	1 ms (10 ms interval)
Continuous current in T	I_T		100	mA	
Current in D, E, F, G, H, I	I		0.5	mA	D, E, F, G, H, I on-state
Voltage at D, E, F, G, H, I	V	−0.3	7.5	v	D, E, F, G, H, I off-state
Short-term peak current at N	I_{Np}	−350	350	mA	0.3 ms (100 ms interval) with $C_{ch} > 40$ µF
Junction temperature	T_j		125	°C	
Storage temperature	T_{stg}	−55	125	°C	
Thermal resistance (system-air)					
SAB 0529	$R_{th\,SA}$		70	K/W	
SAB 0529 G	$R_{th\,SA}$		105	K/W	

All voltages are referred to pin 0, unless otherwise specified.

Operating range

Supply voltage at impressed dc voltage	V_S	4.5	5.5	V	Voltage between pin 0 and V_S
Impressed dc or impressed ac at N[2]					
DC supply from N (rms)	$-I_N$	2.5[1]	12.5	mA	see application circuit
AC supply at N (rms)	I_{Nrms}	5[1]	25	mA	see application circuit
Ambient temperature	T_{amb}	0	70	°C	

1) Only the supply current for the IC, i.e. without triac gate current. The rms gate current additionally flows through N. (The IC may be operated with dc or ac; see also application circuits).
2) The voltage between 0 and V_S is between 5.5 V and 7.0 V for impressed ac and between 6.0 V and 7.5 V for impressed dc. Operation, however, is also assured if V_S falls to 4.5 V (e.g. due to ripple at V_S with dc supply).

Characteristics

$V_S = 4.5$ V to ≤ 5.5 V (7.5 V)[1], $T_{amb} = 0$ °C to 70 °C

		Test conditions	Lower limit B	typ	Upper limit A	
Supply current at V_S and/or N	I_S	$I_S = -I_N$		1.4	2.5	mA
V_S with impressed current at N:						
Impressed ac	V_S	$I_{N\,rms} = 5$ mA	5.5	6.2	7.0	V
Impressed dc	V_S	$-I_N = 2.5$ mA	6.0	6.8	7.5	V
Switching threshold at:						
A, B, C, S, FC, R	V_A		0.3	0.6	1	V
N (if N is clock input)	V_N		0.6	1.2	2	V
TC	V_{TC}			3.5	4.5	V
TS (for voltages $> V_S$)	V_{TS+}			$V_S+1.3$		V
TS (for voltages $< V_S$)	V_{TS-}			$V_S-1.3$		V
L input current at:						
A, B, C, S, FC, R	$-I_{IL}$	$V_A \ldots = 0$ V			20	µA
N (if N is clock input)	$-I_{INL}$	$V_N = 0$ V			40	µA
H input current at:						
A, B, C, S, FC, R	I_{IH}	$V_A \ldots = V_S \leq 5.5$ V			20	µA
N (if N is clock input)	I_{INH}	$V_N = V_S$			10	µA
TC	I_{ITCH}	$4.5\text{ V} \leq V_{TC} \leq V_S$			50	µA
Pos. switching current at TS	I_{TS+}	$V_{TS} = V_{TS+}$	27	45	81	µA
Neg. switching current at TS	I_{TS-}	$V_{TS} = V_{TS-}$	18	30	54	µA
L voltage at D, E, F, G, H, I	V_L	$I_L = 0.5$ mA			0.3	V
Reverse current at D, E, F, G, H, I	I_H				1	µA
L output voltage at T	V_{QTL}	$I_T = 1$ mA		1.5	1.8	V
		$I_T = 10$ mA		1.6	2	V
		$I_T = 100$ mA		1.8	2.3	V

1) with impressed current at N.

MOS IC

Type	Ordering code	Package	Fig. No.
SAJ 141	Q67100-N62	DIP 8	6

The SAJ 141 is an async counter using MOS depletion technology. At three open-drain outputs, it generates the dividing ratios 1000:1, 100:1, or 10:1 of the input frequency. Counted are the LH transitions.

The IC contains a second input with higher switching thresholds to fit applications requiring high noise immunity.

A special reset arrangement provides that the first LH transition appears at the corresponding output not before 10, 100, or 1 000 pulses have been counted.

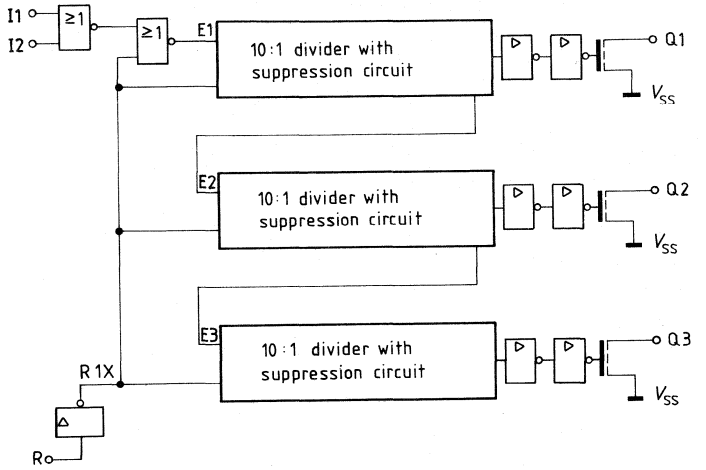
Maximum ratings

		Lower limit B	Upper limit A	
Supply voltage	V_{DD}	−20	0.3	V
Input voltage	V_I	−20	0.3	V
Output current	I_Q	−15	0	mA
Ambient temperature during operation (range 1)	T_{amb}	−25	70	°C
Junction temperature	T_j		125	°C
Storage temperature	T_{stg}	−55	125	°C
Thermal resistance (system-air)	$R_{th\,SA}$		135	K/W

Electrical characteristics
$T_{amb} = 25$ °C

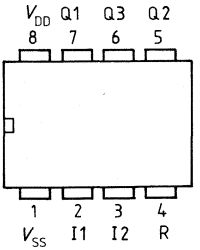
		Test conditions	Lower limit B	typ	Upper limit A	
Supply voltage	V_{DD}		−16		−4.75	V
Supply current	I_{DD}		−6	−3		mA
H input voltage	V_{IH1}	applies also to reset input	−1.2		0.3	V
L input voltage	V_{IL1}		−16		−4.5	V
H input voltage	V_{IH2}		−2.5		0.3	V
L input voltage	V_{IL2}		−16		−8	V
H output voltage	V_{QH}	$R_Q = 10$ kΩ	−2			V
L output voltage	V_{QL}	$R_Q = 10$ kΩ			V_{DD}+0.3	V
H input resistance	R_{IH}		10			MΩ
L input resistance	R_{IL}		10			MΩ
Permissible output current	I_Q		−10			mA
Dynamic characteristics						
Input frequency	f_I		0		1	MHz
Pulse width	t_{WLI}		450		∞	ns
Pulse interval	t_{WHI}		450		∞	ns
HL transition time	t_{THLI}				0.3	ms
LH transition time	t_{TLHI}				0.3	ms
at $f = 1$ MHz, division 10:1						
Pulse width	t_{WHQ}	$C_Q = 10$ pF, $R_Q = 10$ kΩ	2			µs
Delay time	t_{DLH}			0.8	2	µs
HL transition time	t_{THLQ}				3	µs
LH transition time	t_{TLHQ}			0.4	1	µs

Block diagram



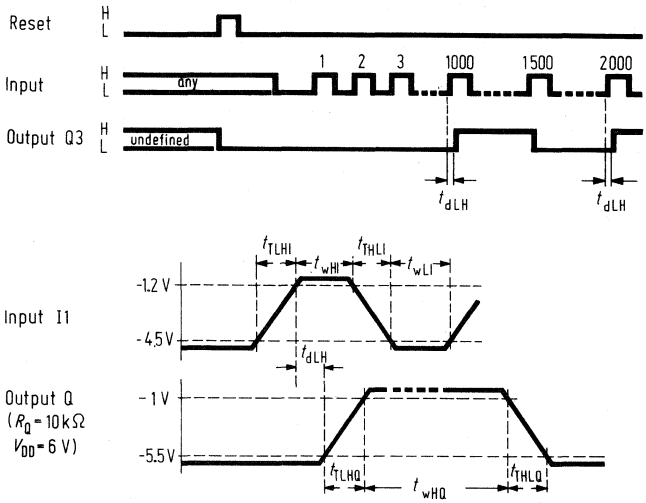
Pin configuration

top view



I = Inputs
Q = Outputs
R = Reset input

Timing diagrams



Inputs I1 and I2 are gated which each other

Input	Level	Function
I1	L	I2 blocked
I1	H	LH transitions at I2 are counted
I2	L	I1 blocked
I2	H	LH transitions at I1 are counted

Audible Signal ICs

Three-Tone Chime
Single-Tone Chime
Dual-Tone Chime

SAB 0600
SAB 0601
SAB 0602

Bipolar IC

Type	Ordering code	Package	Fig. No.
SAB 0600	Q67000-H1948	DIP 8	6
SAB 0601	Q67000-H2312		
SAB 0602	Q67000-H2313		

Three-tone chime SAB 0600

This IC generates the tone sequence of a 3-tone chime. The sound pattern is created by three harmonically tuned frequencies which are switched in succession to a summing point and decay individually in amplitude.

The tone color is adjusted by an external *RC* network (R_1, C_1, and C_2). An 8 Ω loudspeaker can be connected directly via a 100 µF capacitor.

An appropriate design of the loudspeaker housing (shaped as tube or horn) enhances the volume and tone quality and contributes to a pleasant, melodious sound.

Features

- Melodious sound
- Few components required
- Integrated output stage for 8 Ω loudspeaker
- Standby current < 1 µA

Single-tone chime SAB 0601 and dual-tone chime SAB 0602

The two variants SAB 0601 and SAB 0602 were derived from type SAB 0600 by suppressing the last two tones or last tone, respectively, of the three-tone sequence. The SAB 0600 data applies correspondingly.

Maximum ratings

		Lower limit B	Upper limit A	
Supply voltage	V_S	−0.5	11	V
Input voltage at E	V_E	−0.5	V_S	V
Neg. input current at E	$-I_E$		2	mA
Load resistance at Q	R_L	7		Ω
Current consumption at start of tone sequence (refer to measurement circuit)	I_{SM}		90	mA
Current consumption at end of tone sequence (refer to measurement circuit)	I_{SO}		35	mA
Oscillator frequency at C (due to power dissipation)	f_{OSC}	6		kHz
Junction temperature	T_j		150	°C
Storage temperature	T_{stg}	−55	125	°C
Thermal resistance (system-air)	$R_{th\,SA}$		120	K/W

Operating range

Supply voltage	V_S	7	11	V
Ambient temperature	T_{amb}	0	70	°C
Oscillator frequency at C	f_{OSC}	6	100	kHz

Characteristics

$V_S = 7$ V to 10 V; $T_{amb} = 25$ °C

		min	typ	max	
Standby input current	I_0		< 1	10	µA
Supply current with open output	I_{SO}		20	35	mA
Max. output power at 8 Ω (tone 3)	P_Q		0.16		W
Max. output voltage at Q (tone 3)	V_{Qpp}		2.8	4.0	V
Deviation of the max. individual amplitudes referred to tone 3	ΔV_{QM}		± 5		%
Frequency variation of basic oscillator with $R_1, C_1 =$ const.	Δf_o		± 5		%
Triggering voltage at E	V_E	1.5		V_S	V
Input current at E ($V_E = 6$ V)	I_E	500	700		µA
Noise voltage immunity at E	$V_{EN\,pp}$		0.3		V
Triggering delay at $f_o = 13.2$ kHz (t_d varies in inverse proportion to f_o)	t_d	2		5	ms
Min. value of external load resistor	R_1		10		kΩ
Max. value of external load resistor	R_1		100		kΩ

Measurement circuit

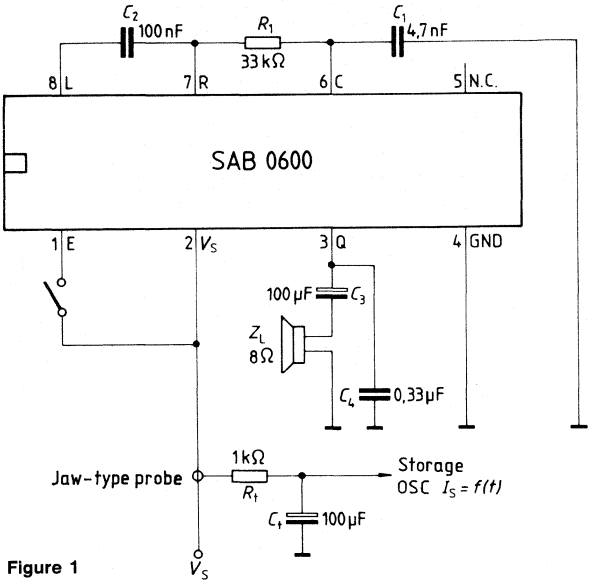


Figure 1

Integral current consumption in the measurement circuit

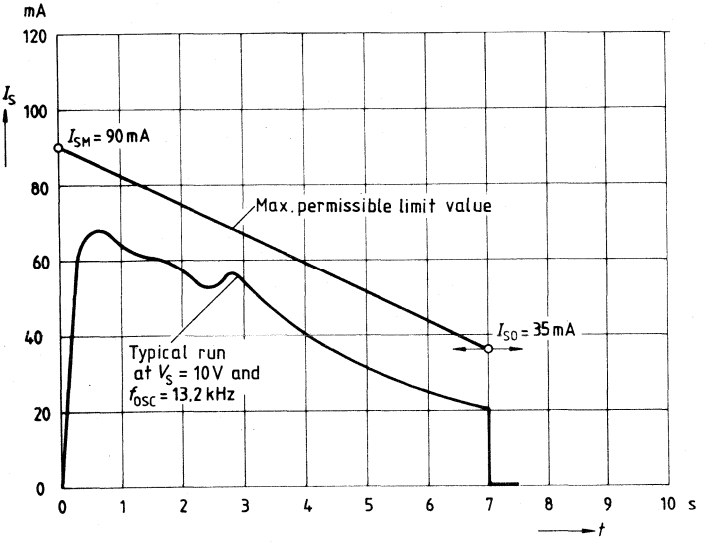


Figure 2

Block diagram

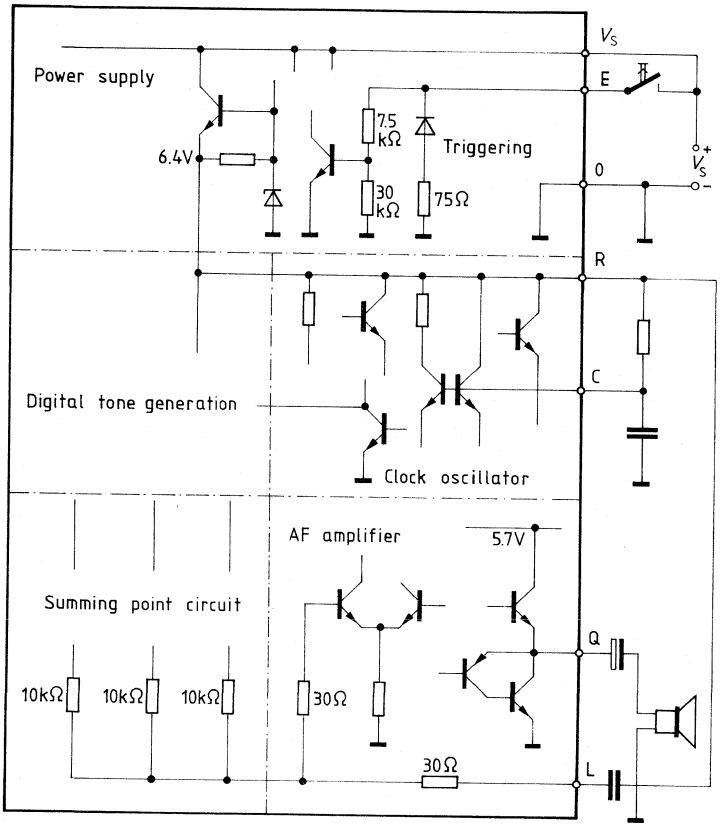


Figure 3

Typical application circuit

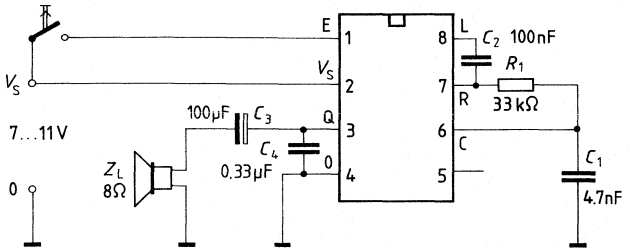


Figure 4

Functional description

The three frequencies – 660 Hz, 550 Hz, and 440 Hz – are obtained by dividing the output of a 13.2 kHz oscillator. One of these three frequencies is divided again to obtain the time base for the tone-decay process. From this time base, 4-bit D/A converters (one for each tone) generate the decay voltage with which the three tones are successively activated and, overlapping each other, are attenuated. The basic frequency is determined by an external *RC* network (pins R and C).

The output stage can drive an 8 Ω loudspeaker with approximately 0.16 W via 100 µF. The output voltage is of square shape. To obtain a melodions output tone as required, the higher harmonics may be reduced by shunting pin L through a suitable capacitor to ground. The output volume can be regulated here by means of a potentiometer.

The circuit only draws current in the active state, and automatically switches off after the tones have decayed. The circuit is activated by a short pulse, between 1.5 V and V_S in amplitude, applied to the triggering connection E (pin 1). If the trigger voltage is still, or again, present when the tones have decayed, the three tones are repeated.

The circuit is not activated when a trigger pulse on E is shorter than 2 ms (interference suppression).

To prevent triggering of the circuit by cross-talk voltages, especially in case of long input lines, the noise voltage peaks should be limited to 0.3 V at the IC input. For this purpose the control line (possibly in front of a series resistor) can be shunted to ground through a suitable capacitor.

Application for ac and dc triggering (figure 5)

The input can alternatively be triggered with direct or alternating current. An internal diode circuit hereby short-circuits the input for negative halfwaves.

The peak voltage of the positive halfwave is added to the battery voltage. A series resistor must be connected into the trigger line to limit the voltage at input E (pin 1) to a maximum value equal to V_S.

The minimum input current at pin E of the SAB 0600 (pin 1) is 500 µA at 6 V. If the voltage drop occurring at 500 µA at the series resistor R_3 (figure 5) amounts to at least the ac peak voltage between A and B ($\hat{V}_{AB}$ ~), the IC will be safe.

The formula $$R_{3\,min} = \frac{\hat{V}_{AB\,max.}}{500\ \mu A}$$

determines the lower limit for R_3.

The upper limit for R_3 is determined by the lowest trigger voltage between A and 0 (pin 4). In the application shown in figure 5, this will be the battery voltage if the device is also to be operated independently of the bell system (triggering by short circuit of A and B).

For reliable triggering, the SAB 0600 requires a current of at least 50 µA with approx. 1.5 V at pin E. Assuming this current, the voltage drop at R_3 must, therefore, not exceed $V_S - 1.5$ V.

The formula $$R_{3\,max} = \frac{V_{S\,min.} - 1.5\ V}{50\ \mu A}$$

results in the upper limit for R_3.

Calculation example for the circuit in figure 5

max. $V_{AB\,rms} = 25$ V max. $\hat{V}_{AB} = 25\ V \times \sqrt{2} = 35.4$ V

$$R_{3\,min} = \frac{35.4\ V}{500\ \mu A} = 70.8\ k\Omega$$

min. $V_S = 6$ V

(The operating range of the SAB 0600 may extend to 6 V for individual components).

$$R_{3\,max} = \frac{6\ V - 1.5}{50\ \mu A} = 90\ k\Omega$$

In this example, a value of 82 kΩ ± 10% would be suitable for R_3.

Circuit for SAB 0600 application in home chime installations utilizing ac and dc triggering; adjustable sound and volume

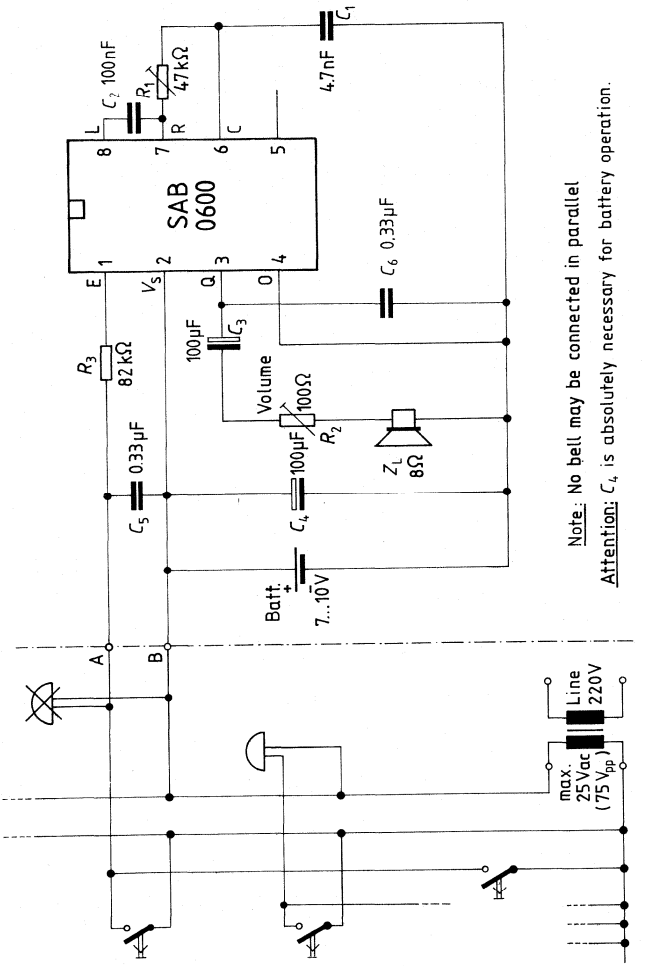


Figure 5

PCB layout information: Because of the high peak currents at V_S, Q, and 0 (ground) and to avoid RF oscillations, the lines should be designed in a flatspread way or as star pattern. Star points are the terminals of capacitor C_4.

Further details regarding the circuit in figure 5

Because an ohmic contact between A and B causes triggering of the chime, no bell may be connected in parallel to the chime. However, paralleling several chimes does not cause any problems.

In older batteries, the higher internal resistance of the battery may cause voltage drops becoming apparent as distortions. C_4 serves as a buffer element expanding the service life of the battery.

The trigger line connected to pin A acts – in open state – as antenna for noise pulses which could trigger the chime unintentionally. Capacitor C_5 will largely suppress such interference.

If there is the risk of incorrect polarity connection when changing the battery, the battery line should be protected by a diode.

For the selection of components, the following recommendations are given:

Capacitors:

C_1: 4.7 nF/≥ 10 V, ± 5%; e.g. MKT
C_2: 100 nF/≥ 10 V, ± 20%; e.g. MKT
C_3: 100 µF/≥6.3 V, ± 100/—10%; e.g. aluminum electrolytic
C_4: 100 µF/≥ 10 V, + 100/—10%; e.g. aluminum electrolytic
C_5, C_6: 330 nF/≥ 50 V, + 100/—20%; e.g. ceramic

Resistors:

R_3: 82 kΩ/0.1 W, ± 10%, carbon film resistor
R_1: When a fixed resistor is used, 0.1 W ± 5% metal film resistor.

Preliminary data **Bipolar IC**

Type	Ordering code	Package	Fig. No.
SAE 0700	Q67000-A2445	DIP 8	6

The audible signal device SAE 0700 generates two tone frequencies in a ratio of approx. 1.4 : 1 that follow one another in a periodic sequence. The tone frequency can be varied throughout a range between 100 Hz and 15 kHz by an external resistor. The switching frequency of 0.5 to 50 Hz is set by an external capacitor. The SAE 0700 can be used to drive either a loudspeaker or a piezo-ceramic transducer. The SAE 0700 can be supplied with voltage in two ways:

1. rms ac voltage from 10 V
2. dc voltage from 9 to 25 V

The SAE 0700 issues the tone sequence for as long as the supply voltage is applied. After application of the supply voltage, the tone sequence commences with the higher of the two tones.

Features

- Direct ac-voltage feeding possible through integrated bridge rectifier
- Integrated overvoltage protection through Z diode, approx. 28 V
- Bridge rectifier provides for protection against incorrect polarity in dc operation
- Few external components (one resistor and one capacitor minimum)

Block diagram (with external components for dc supply)

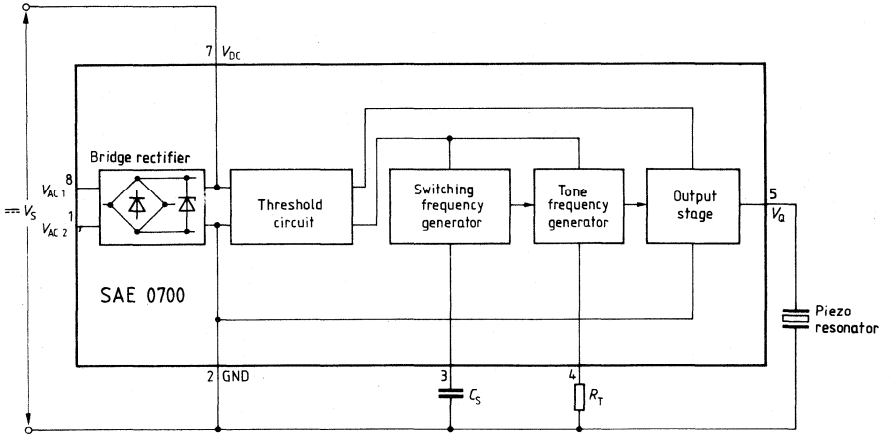


Figure 1

Functional description

The audible signal device SAE 0700 (see blcok diagram, **fig. 1**) includes the following functional blocks:

- bridge (for voltage supply) and overvoltage protection
- threshold circuit
- switching-frequency generator
- tone-frequency generator
- output stage

Bridge rectifier: The bridge rectifier enables direct feeding with ac voltage or dc voltage (independent of polarity). DC-voltage supply without integrated bridge is also possible via pins V_{DC} and GND.

If the voltage is supplied via the bridge, the input voltage V_{81} should be dimensioned such that at least 9 V appear at the pin V_{DC} (also with output loading). It should also be noted that in the case of voltage supply via the bridge, the maximum output current has to be limited to 50 mA.

Response of the SAE 0700 as a result of spikes on the AC line is prevented by a built-in initial resistance R_{INI}. In a voltageless condition R_{INI} provides for discharging the storage capacitor of V_{DC} to ground.

The Z diode following the bridge serves as overvoltage protection. The bridge circuitry shown in **figure 2** efficiently protects the SAE 0700 against damage as a result of the following voltage values:

- overvoltages in acc. with VDE 0433 (2 kV – 10/700 µs)
- ac voltages up to 220 V/50 Hz for a duration of 30 s

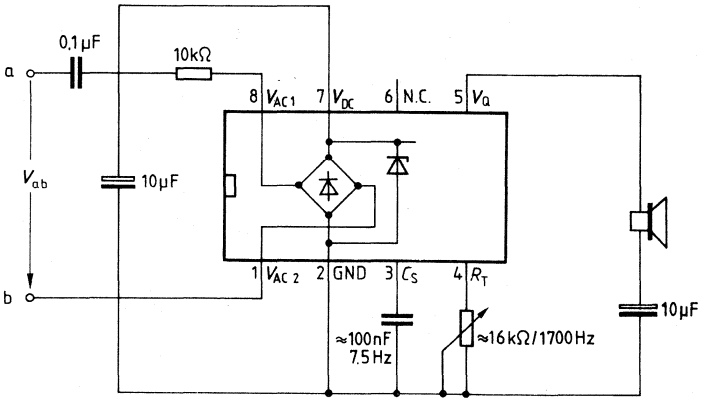


Figure 2

Threshold circuit: With a threshold voltage of typically 8.6 V this ensures that the SAE 0700 is not activated by noise pulses.

Switching-frequency generator: This switches periodically between the two frequencies produced by the tone-frequency generator. Wiring with a capacitor C_S produces a switching frequency f_S according to the following formula:

$$f_S\ [\text{Hz}] = \frac{750}{C\ [\text{nF}]} \pm 25\% \quad \text{(valid from 0.5 to 50 Hz)}$$

Tone-frequency generator: This generates a squarewave voltage with the two tone frequencies f_{T1} and f_{T2}. The basic frequency f_{T1} and the second tone frequency f_{T2} are calculated according to the following formulae:

$$f_{T1}\ [\text{Hz}] = \frac{2.72 \times 10^4}{R\ [\text{k}\Omega]} \pm 25\% \quad \text{(valid from 0.1 to 15 kHz)}$$

$$f_{T2}\ [\text{Hz}] = f_{T1} \times (0.725 \pm 5\%)$$

The tone-frequency generator is temperature-compensated for better stability.

Output stage: This boosts the generated tone voltage for direct driving of a piezo-ceramic transducer or a loudspeaker, possibly across a dropping resistor.

Pin configuration

Pin No.	Symbol	Function
1	V_{AC2}	AC-voltage input
2	GND	Ground
3	C_S	Connection for capacitor C_S
4	R_T	Connection for resistor R_T
5	Q	Output
6	N.C.	Not connected
7	V_{DC}	DC-voltage input
8	V_{AC1}	AC-voltage input

Maximum ratings

		Lower limit	Upper limit	
Voltage at pin 7	V_{DC}	−0.5	26	V
Voltage at pin 3	V_{32}	−0.5	5.5	V
Voltage at pin 4	V_{42}	−0.5	7	V
Output voltage at pin 5	V_Q	−0.5	V_{DC}+0.5	V
AC voltage at pin 8 and 1 (peak value)	V_{AC}		28	V
Input current of bridge	I_{81}	−50	50	mA
AC input current of bridge	$I_{81\,rms}$		25	mA
Output current (50 µs, duty cycle 1 : 10)	I_Q	−100	100	mA
Output current	$I_{Q\,rms}$		50	mA
Total power dissipation (T_{amb} = 25 °C)	P_{tot}		0.8	W
Junction temperature	T_j		150	°C
Storage temperature	T_{stg}	−40	125	°C
Thermal resistance (system-air)	$R_{th\,SA}$		120	K/W

Operating range

Supply voltage	V_{DC}	9	25	V
Tone frequency	f_{T1}	0.1	15	kHz
Ambient temperature	T_{amb}	−25	85	°C

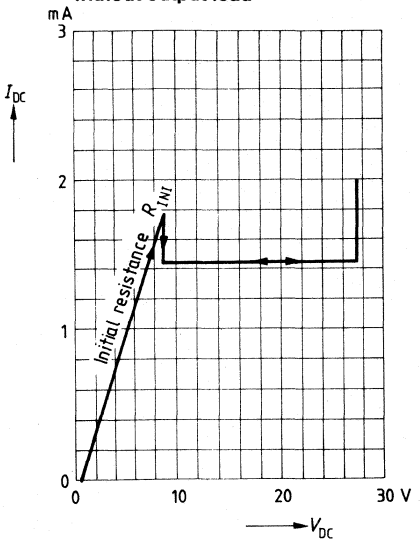
Characteristics

T_{amb} = −25 °C to 85 °C

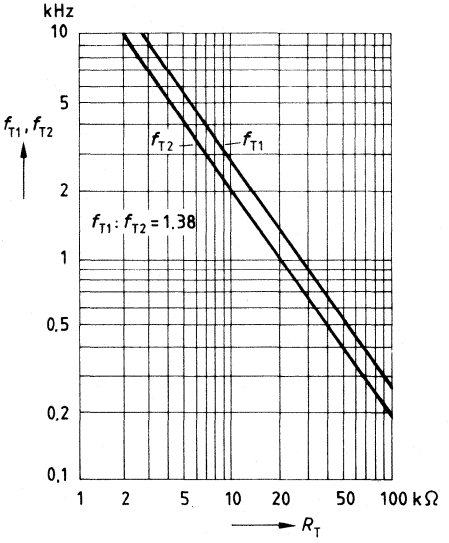
		Test conditions	Lower limit B	typ	Upper limit A	
Current consumption	I_{DC}	V_{DC} = 9 V to 25 V, w/o load		1.5	1.8	mA
Switching threshold	$V_{DC\,ON/OFF}$		8	8.6	9	V
Initial resistance	R_{INI}	see characteristic, figure 3	3.5	4.7	6	kΩ
Output-voltage swing	V_Q	I_Q = ± 10 mA	V_{DC}−3.7	V_{DC}−3		V
Tone frequency	f_{T1}	V_{DC} = 15 V, V_{32} = 0 V, R_T = 16 kΩ	1.275	1.700	2.125	kHz
Switching frequency	f_S	V_{DC} = 15 V, C_S = 100 nF	5.6	7.5	9.4	Hz
Tone frequency ratio	f_{T1}/f_{T2}		1.31	1.38	1.45	
Temperature coefficient of tone frequencies	TC_f			8×10^{-4}		K^{-1}

Characteristic curves

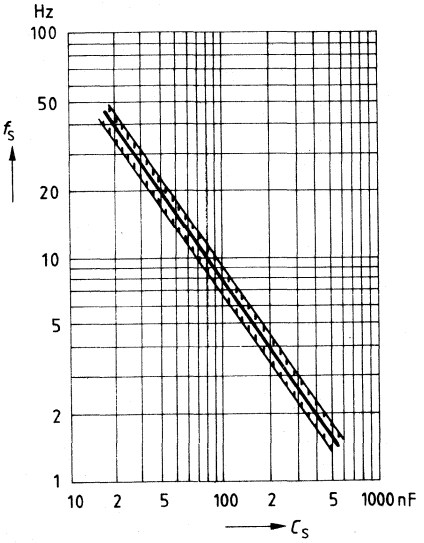
Current consumption versus supply voltage V_{DC} without output load



Tone frequencies f_{T1} and f_{T2} versus resistance R_T



Switching frequency f_S versus capacitance C_S



Remote Control Systems

Summary of types

Type	Ordering code	
SAB 3210[1)]	Q67100-Y396	Infrared remote control system – transmitter
SAB 4209	Q67100-Y460	Infrared remote control system – receiver (four analog functions)
SDA 2008[1)]	Q67100-Y503	Infrared remote control system – transmitter
SDA 2114 P[1)]	Q67000-A1859	Infrared diode driver IC incl. power-on transistor for PMOS control
SDA 2208	Q67000-A2201	Remote control transmitter with IR diode driver
SDA 3205[1)]	Q67100-Y578	Infrared remote control system – receiver
SDA 3206	Q67100-Y577	Infrared remote control system – transmitter

1) Detailed technical data on those types are to be found in the Siemens Data Book "ICs for Entertainment Electronics" edition 1984/85, Ordering No.: B/2749-101

MOS IC

Type	Ordering code	Package	Fig. No.
SAB 4209	Q 67100-Y460	DIP 18	11

The receiver circuit SAB 4209, developed in MOS depletion technology, evaluates the IR signals coming from the transmitter circuit SDA 3206 or SDA 2208, respectively. Through a serial interface, which is externally accessible, the instructions are forwarded to the program memory and the analog memory. The SAB 4209 permits the control of 16 programs and four analog functions. In addition, the circuit includes a keyboard changeover and one input or output for the ON/OFF function.

Features

- At the serial interface (I-bus) 30 instructions can be applied in addition to those intended for the SAB 4209, i.e. for teletext.
- Through the serial interface, instructions can be transferred into the SAB 4209 directly, whereby these instructions have an absolute priority over IR signals coming from the transmitter.
- The program outputs are short-circuit-resistant and can be set externally.
- The SAB 4209 can be operated with the built-in oscillator as well as with an external clock.

Maximum ratings (referred to $V_{DD} = 0$ V)

Supply voltage range	V_{SS}	−0.3 to 18	V
Input voltage range	V_i	V_{SS} −18 to V_{SS} +0.3	V
Total power dissipation	P_{tot}	500	mW
Power dissipation per output	P_q	100	mW
Junction temperature	T_j	125	°C
Storage temperature range	T_{stg}	−40 to 125	°C

Operating range (referred to $V_{DD} = 0$ V)

Supply voltage range	V_{SS}	11 to 16	V
Ambient temperature range	T_{amb}	0 to 70	°C

Characteristics

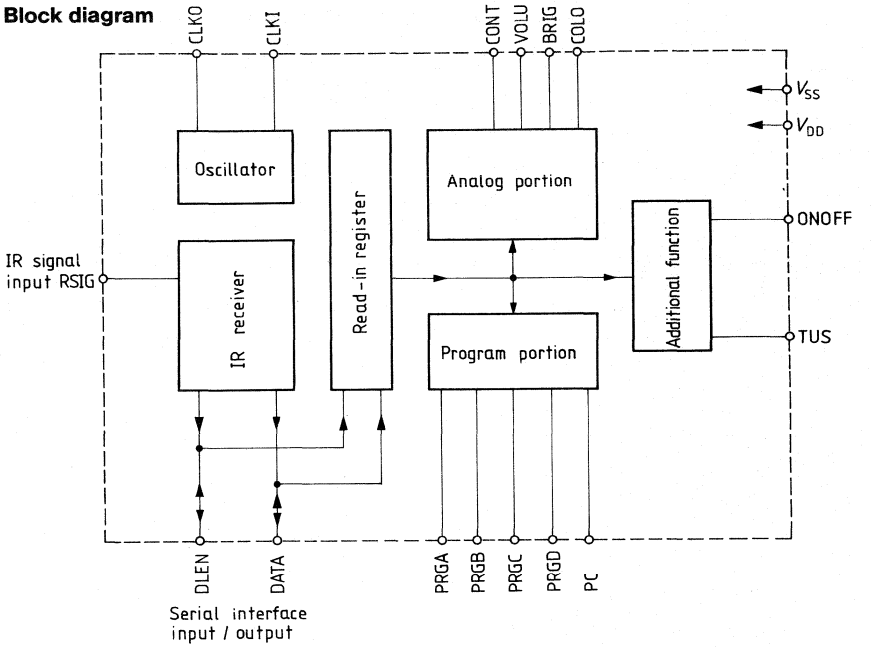
(referred to $V_{DD} = 0$ V, $T_{amb} = 0°C$ to 70 °C)

		min	typ	max	
Current consumption (outputs not connected)	I_{DD}		5	10	mA
Inputs					
Clock input CLKI					
L input voltage	V_{iL}	0		V_{SS} −7	V
H input voltage	V_{iH}	V_{SS} −1			V
Input current	I_i			V_{SS} 15	µA
Transition times	t_{THL}, t_{TLH}			4	µs
Frequency	f	20	60	70	kHz
Remote control signal input RSIG					
Input alternating voltage	V_{iH}	V_{SS} −1		V_{SS}	V
	V_{iL}	0		V_{SS} −3.5	V
Input resistance	R_i	0.2			MΩ
Serial interface inputs					
DLEN and DATA					
L input voltage	V_{iL}	0		V_{SS} −7	V
H input voltage	V_{iH}	V_{SS} −1		V_{SS}	V
H input current ($V_i = V_{SS}$) (internal pull-low resistor)	I_{iH}			2	mA
Delay time + transition time	$(t_d + t_T)_{HL}$			1	µs
	$(t_d + t_T)_{LH}$			1	µs
Program stepping input PC					
H input voltage	V_{iH}	V_{SS} −1.5		V_{SS}	V
L input voltage	V_{iL}	0		V_{SS} −7	V
H input current ($V_i = V_{SS}$) (internal pull-low resistor)	I_{iH}			10	µA
Outputs					
Standby output ONOFF					
H input voltage ($I_{iH} < 1$ mA)	V_{iH}	V_{SS} −1		V_{SS}	V

Characteristics (referred to $V_{DD} = 0$ V, $T_{amb} = 0$ °C to 70 °C)

Outputs		min	typ	max	
Serial interface outputs					
H output voltage ($I_{load} \leq 200$ µA)	V_{qH}	V_{SS} −1.5		V_{SS}	V
L output voltage ($I_q = 10$ µA)	V_{qL}	0		0.35	V
Delay and transition time	$t_{dH} + t_{THL}$			5	µs
($C_L = 50$ pF referred to CLKI)	$t_{dL} + t_{THL}$			5	µs
Program memory outputs PRGA, PRGB, PRGC, PRGD					
H output voltage ($I_q = 0.1$ mA)	V_{qH}	V_{SS} −0.5		V_{SS}	V
L output voltage ($I_q = 10$ µA)	V_{qL}	0		1	V
Program stepping output PC					
H output voltage ($I_q = 0.3$ mA)	V_{qH}	V_{SS}−1.5		V_{SS}	V
L output voltage (no load)	V_{qL}	0		2	V
Analog function outputs COLO, BRIG, VOLU, CONT					
H output voltage ($I_q = 1$ mA)	V_{qH}	V_{SS} −1.5		V_{SS}	V
L output voltage ($I_q = 1$ µA)	V_{qL}	0		0.35	V
Standby and spare outputs ONOFF, TUS					
H output voltage ($I_q = 0.3$ mA)	V_{qH}	V_{SS} −1.5		V_{SS}	V
L output voltage ($I_q = 1$ µA)	V_{qL}	0		0.35	V
Clock output CLKO					
H output voltage (no load)	V_{qH}	V_{SS} −1		V_{SS}	V
L output voltage (no load)	V_{qL}	0		1	V

Block diagram



Pin configuration

Pin No.	Function
1	V_{SS}, supply voltage
2	CLKO, clock output
3	CLKI, clock input
4	PRGD, program control output
5	PRGC, program control output
6	PRGB, program control output
7	PRGA, program control output
8	PC, program change, strobe input/output
9	TUS, keyboard changeover
10	VOLU, volume control output
11	ONOFF, standby output
12	CONT, contrast output
13	BRIG, brightness output
14	COLO, color contrast output
15	RSIG, IR input
16	DLEN, I-bus input/output
17	V_{DD}, supply voltage
18	DATA, I-bus input/output

Description of functions

1 Infrared receiver (pin RSIG)

The infrared receiving portion accepts the IR signal, processes it and transfers the instructions received to the serial interface. The IR signal consists of alternating current pulses with a frequency of approx. 30 kHz and a duration of approx. 0.5 ms per cycle. The instructions are transferred as 7-bit words (1 start bit, 6 information bits) in the biphase code. See timing diagram 1.

The infrared signals are repeated approx. every 120 ms. All instructions are issued by the receiving portion as repeat instructions, with a sequence frequency equal to that of the incoming IR signals.

2 Serial interface (I-BUS) as an output and input (pins DLEN, DATA)

Output at the serial interface (I-BUS) is performed according to the timing diagram 2. The outputs are open-drain stages with built-in load resistors, which may also be used as inputs.

In addition, all instructions may be entered via the serial interface, see timing diagram 3 (the infrared instructions will not be processed in the circuit, before they have passed the serial interface).

The input is tested to protect the transfer of the instructions against capacitive and inductive noise pulses. Therefore, the leads at the serial interface must be kept close together.

Input through the serial interface has absolute priority over an infrared input.

It is possible to read out instructions through the serial interface. However, at the same time they can be changed through an external circuit in such a way that they cannot be interpreted any longer by the receiver portions. For example, pin DLEN of the instructions for direct program selection can be kept on high level for two clock pulse periods beyond the output time, whereby the program memory is no longer addressed and the program instructions can be used as digit-instructions for other purposes (e.g. teletext page-selection).

3 Analog-value memory (outputs VOLU, BRIG, COLO, CONT)

The SAB 4209 contains 4 analog-value memories for setting volume, brightness, color saturation, and contrast.

The analog values can be altered in approx. 60 steps. The speed of alteration corresponds to the sequence-frequency of the repeat instructions (approx. 8 Hz). The analog values are put out as square pulses with a frequency of approx. 1 kHz, whereby the duty cycle corresponds to the analog value. The analog voltage value originates in an external low-frequency passing filter through formation of the mean values of timing.

By means of the command "normal position", the analog memories are set to a mask-programmed basic position ($\nu_{VOLU} = 1/3$, $\nu_{CONT} = \nu_{BRIG} = \nu_{COLO} = 1/2$, whereby $\nu = t_{High}/T$). When the supply voltage rises starting at 0, the analog values are also set to the normal position.

Volume control output VOLU

The volume output is internally kept on a low level

- approx. 128 ms prior to the H pulse appearing at the output after a program change instruction,
- when the quicktone-flipflop is set,
- when the circuit is in a "standby" mode,
- when pin PC is on a high level.

Quicktone

An appropriate command sets a flipflop in the actually complementary state.
The flipflop is reset

- by instruction "Vol +",
- by condition "standby",
- by an instruction to the program memory,
- by the instruction "normal position".

As long as the quicktone flipflop is set, the volume output is kept "low".

As long as the circuit remains in the "standby" condition, the adjustment instructions for the analog memory are ineffective.

After the "standby" condition is ended, the analog outputs move into the basic position.

4 Program memory (outputs and inputs PRGA, PRGB, PRGC, PRGD)

The program memory consists of a 4-bit ring counter which permits the addressing of 16 programs.

The 16 programs may be addressed through remote control by selecting 1...16 or, through up- and downcounting of the ring counter.

When the supply voltage rises starting at zero, the program outputs are set to LLLH. By changing one mask it is possible to set a different program. The outputs of the program memory are also effective as inputs, because they can be set or reset externally through a low-resistance control.

Strobe output, stepping sequence input (pin PC)

When the program counter receives an instruction via remote control, a positive pulse is produced at output PC after a certain time delay. At the start of the delay time the volume output VOLU is muted. Muting can be reverted by means of the trailing edge of the PC pulse (see timing diagram 4). The output PC can be also connected to a capacitor to extend the muting (up to approx. 0.5 s).

The same muting behavior results when the supply voltage rises starting at zero, and pin ONOFF is simultaneously kept on low (see timing diagram 5).

Pin connection PC may also be used as an input. If a positive potential is applied externally, the program counter proceeds by one step. Thereby the external capacitor will have a debouncing effect (see timing diagram 6). During "standby" condition the output "PC" is on a static positive level. With each program change a single PC pulse will be generated.

5 Standby-output/input (pin ONOFF)

This pin controls the power supply by means of a transistor. When a program is called up — and also in connection with some other instructions specified in table 1 — the set is turned on by this output.

In = low, standby = high

Through the instruction "standby" the set is put into a "standby" mode. When the supply voltage rises starting at zero, the set is also switched to "standby".

Pin ONOFF also acts as an input when controlled from a low resistance source, e.g. with a wiping contact at the mains-switch.

6 Keyboard changeover (pin TUS)

The output is controlled by a toggle-flipflop. With each depression of the corresponding key of the transmitter the output changes in the opposite condition.

The preference position is low.

The position is set

- when the supply voltage is turned on,
- when condition "standby" exists,
- when the instruction "normal position" is issued.

The output can be set and reset externally by low-ohmic connections.

When the output is in the high condition, the incoming instructions are no longer evaluated in the receiver module, but only output at the serial interface. Exception: The instructions "Keyboard changeover" (No. 7) and "Standby" (No. 2) are always evaluated.

Table 1
Coding of instructions on the I BUS and for IR transmission

No.	Code	Instruction	After instruction TUS
	FED CBA		
0	000 000	Normal position	Previous condition is maintained
1	001	Quicktone (muting)	
2	010	Standby	Standby + TR (keyboard reset)
3	011		Previous condition is maintained
4	100	Program step + /ON	"
5	101	Program step −/ON	"
6	110	ON	"
7	111	TUS/ON	TR (keyboard reset)
8	001 000	Volume +	Previous condition is maintained
9	001	Volume −	
10	010	Brightness +	"
11	011	Brightness −	"
12	100	Color +	"
13	101	Color −	"
14	110	Contrast +	"
15	111	Contrast −	"

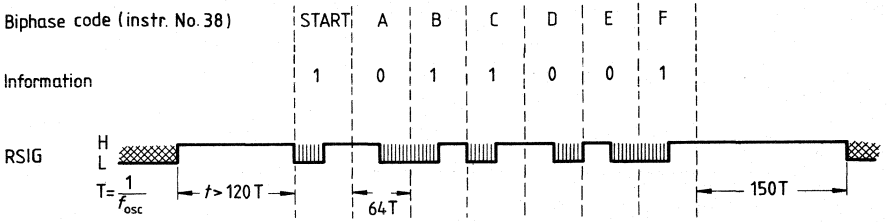
Table 1 (cont'd)
Coding of instructions on the I BUS and for IR transmission

No.	Code	Instruction	After instruction 7
	FED CBA	D C B A (PRG output)	Keyboard changeover
16	010 000	L L L L /ON	Previous condition
17	001	L L L H /ON preferred position	is maintained
18	010	L L H L /ON	"
19	011	L L H H /ON	"
20	100	L H L L /ON	"
21	101	L H L H /ON	"
22	110	L H H L /ON	"
23	111	L H H H /ON	"
24	011 000	H L L L /ON	"
25	001	H L L H /ON	"
26	010	H L H L /ON	"
27	011	H L H H /ON	"
28	100	H H L L /ON	"
29	101	H H L H /ON	"
30	110	H H H L /ON	"
31	111	H H H H /ON	"

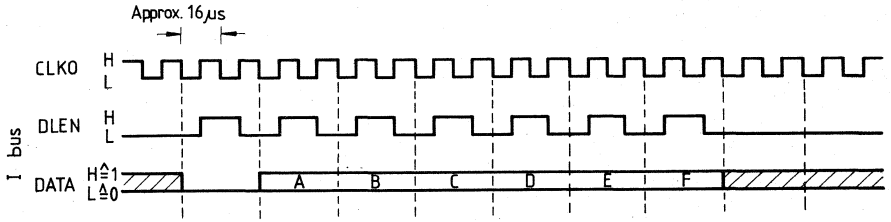
Instructions 32 to 61 are not processed by the circuit but only edited through the serial interface.

Instruction 63 (= 111 111) must remain free (see timing diagram 1).
Instruction 62 (= 111 110) is the end-instruction. (See data sheet of SAB 3210)

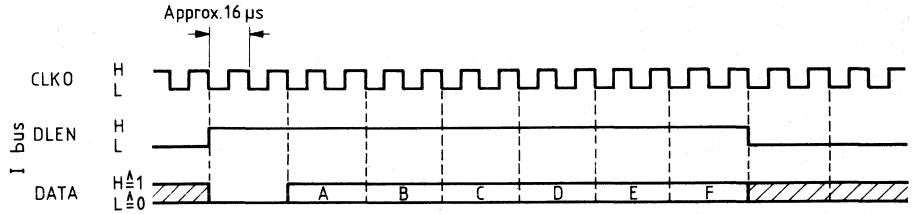
Timing diagram 1
(biphase coding)



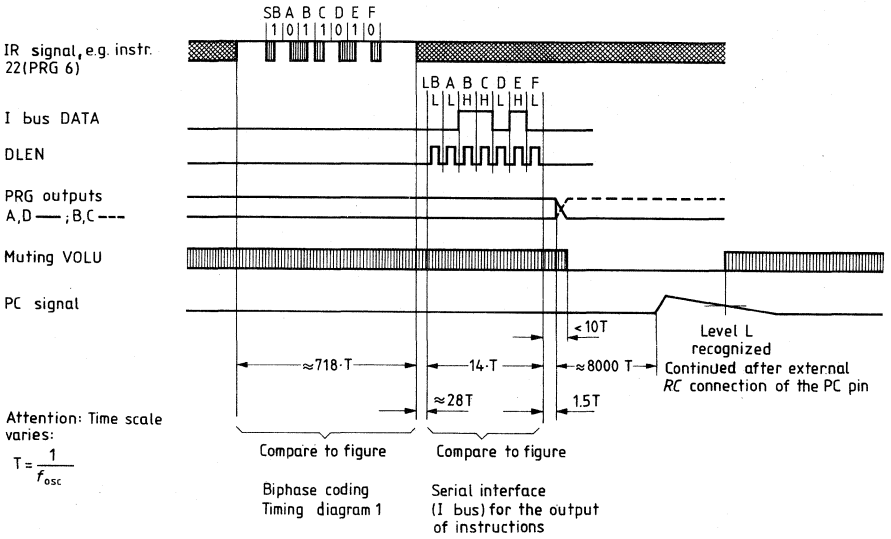
Timing diagram 2
Serial interface (I bus) for the output of instructions



Timing diagram 3
Serial interface (I bus) for the input of instructions

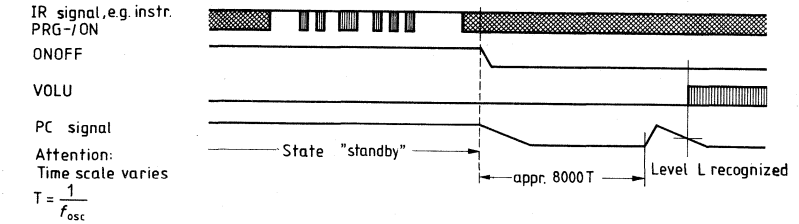


Timing diagram 4

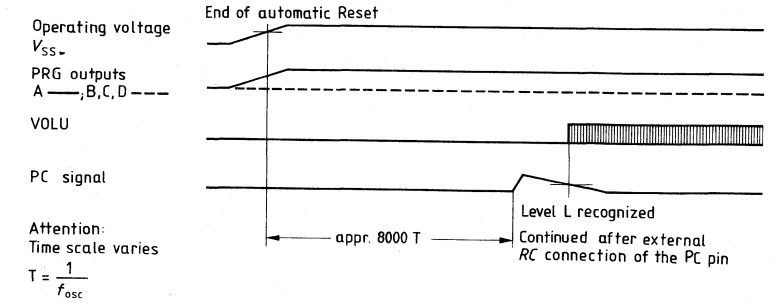


Timing diagram 5

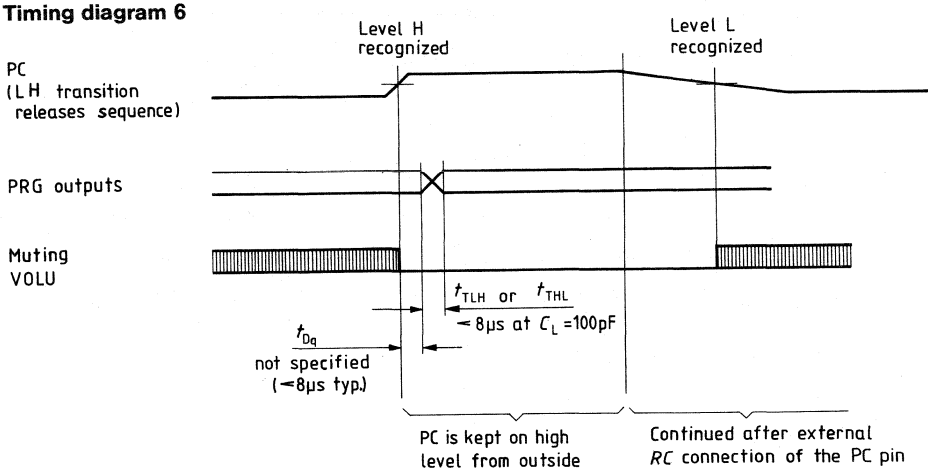
Example a) Switching on by means of an IR instruction



Example b) ONOFF is connected to V_{DD} during the supply voltage rise via wiping contact



Timing diagram 6



Preliminary data **Bipolar IC**

Type	Ordering code	Package	Fig. No.
SDA 2208	Q67000-A2201	DIP 20	12

The SDA 2208 is designed as a remote control transmitter for direct driving of infrared transmitter diodes. The commands are generated by an input matrix (i.e. keyboard) in the form of biphase codes. Distributed over 8 levels, there are a max. of 512 commands available, or 64 commands per level.

Maximum ratings

Supply voltage range	V_S	−0.3 to 10.5	V
Matrix rows	V_{row}	−0.3 to V_S	V
Matrix columns	V_{col}	−0.3 to V_S	V
Programming pin (PPIN)	V_{PP}	−0.3 to V_S	V
Oscillator input (OSC)	V_{OSC}	−0.3 to 2	V
Infrared output (IRA)			
inhibited	V_q	−0.3 to 10.5	V
in operation	V_q	−0.3 to 8	V
Junction temperature	T_j	125	°C
Storage temperature range	T_{stg}	−55 to 125	°C

Operating range

Supply voltage range	V_S	4 to 10	V
Ambient temperature range	T_{amb}	0 to 70	°C
Oscillator frequency range	f_{OSC}	430 to 530	kHz
Frequency deviation (tolerance of the external circuitry = 0)			
at ceramic resonator	Δf_{OSC}		
at *LC* circuit	Δf_{OSC}		

Characteristics

($4\ V \leq V_S \leq 10\ V$; $0\ °C \leq T_{amb} \leq 70\ °C$)

		min.	typ.	max.	
Current consumption					
standby mode	I_S			1	µA
transmitting phase	I_S			10	mA
Output IRA, current consumption					
inhibited	I_q		< 1	10	µA
conductive ($2 < V_q < 6\ V$)	I_q	500		1000	mA
Connecting resistance (row-column or column-PPIN)	R_{RC}			500	Ω

Pin configuration

Pin No.	Function
1	Ground
2	Output IRA
3	Supply voltage V_S
4	R2
5	R7
6	R1
7	R6
8	R8
9	R4
10	R3
11	R5
12	PPIN
13	CH
14	CE
15	CB
16	CC
17	CG
18	CD
19	CF
20	Oscillator input OSC

The abbreviation R means 'row' and C means 'column'.

Detailed description of functions

Voltage supply

Being absent in the quiescent state, voltage consumption will begin subsequently to connecting the component's matrix. However, after the matrix has been disconnected, the IC will automatically complete the message before returning to the quiescent state.

Clock input

The clock input is eqipped with a ceramic resonator. This resonator oscillates with its parallel resonant frequency. In addition, an external clock signal can be fed into the OSC pin. As an alternative, the oscillator can be operated by using an *LC* circuit with a coupling capacitor.

Input matrix

The matrix is comprised of 8 rows and 8 columns, whereby the supply voltage V_S is used as column A. Messages are transmitted by connecting the respective rows with the columns.

As a result, the transmitter is switched on and a message is generated. A message includes a start command, a varying number of information commands (depending, like the length of the message, on the duration of the matrix connection) as well as an end command.

If less than 8 rows are required for the key matrix, a smaller-sized package can be used for the IC.

Programming via PPIN

The programming pin (PPIN) is used to provide access to all command sets or 512 commands, since the 8x8 matrix limits the use to one command set or 64 commands only. By having the command sets subdivided into 8 levels of 64 commands each, a specific level can be selected by either keeping the PPIN open or by combining it with one of the seven column inputs (SPB to SPH).

Connecting the PPIN with one column alone does not increase the standby-current consumption I_S.

Operating errors and their prevention

As a prerequisite for errorfree message output with at least one information command, the matrix connection has to be free from interference at a clock frequency-dependent, minimum duration (approx. 60 ms at 500 kHz clock frequency). The applied circuit is equipped with a preventive mechanism (key bouncing) against erroneous outputs by means of automatic resetting during any detected distortions. In addition, operating errors such as connecting more than one respective row and column are recognized, ending the transmission of the message by continuously transmitting end commands. Operating errors can only be cancelled by disconnecting all matrix connections. When operating the level selection key (PPIN function), it has to be activated before or simultaneously with the matrix key. Otherwise, the level key will not be effective. Also, simultaneous depressing of several level keys has the same effect on the message as an erroneous matrix operation.

Composition of the message

After the device has been switched on, command No. 511 (10 bit word length) will respond as start command to indicate to the receiver the onset of transmission. Depending on the duration of the matrix connection, a series of identical information commands will appear. If the message is ended by disconnecting the matrix connection, not more than one additional information command will be issued which is immediately followed by the end command. The end command is identical with the start command.

Command structure

Each command is comprised of a presignal, an infrared interval, a start bit and 9 information bits.

The presignal will appear for $256/f_{CLK}$. During this time, a simple amplitude adjustment of the input amplifier can be performed by the receiver.

The infrared interval appears between the end of the presignal and the onset of the start bit. Again, the receiver is provided with enough time to recognize transmission distortions based on the limits of the transmission range.

The start bit has been permanently programmed as :1: and is used for synchronization purposes between transmitter and receiver.

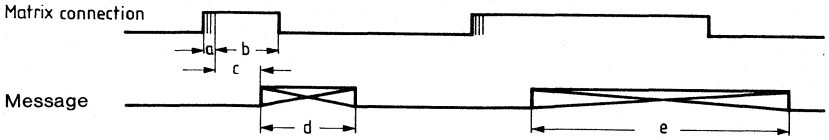
The bit structure is illustrated in the pulse diagram.

Output driver stage

By providing a fully integrated driver stage, the infrared transmitting diodes can be directly connected to the infrared output IRA. Once a range has been defined, the diode current is maintained on a constant level to stabilize the transmitting power of the infrared diodes.

Pulse diagrams

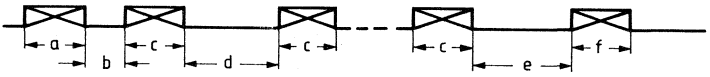
Typical operating process



for 500 kHz
b = 60.928 ms
c = 26.624 ms
d = 177.664 ms

a) bounce
b) minimum key operating time to complete message with one information command
c) delay between the on-set of interference-free matrix connection and begin of message transmission
d) message with one information command
e) message with several identical information commands

Composition of message



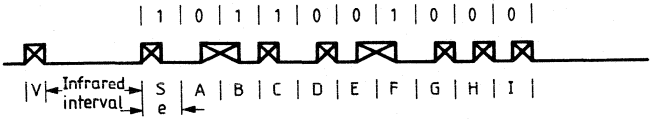
for 500 kHz
a = c = f = 13.312 ms
b = 19.968 ms
d = e = 177.76 ms

a) start command 10 bits
b) time interval between start and information command
c) information command 10 bits
d) time interval between identical information commands
e) time interval between information and end command
f) end command 10 bits

The timespan of an interference-free matrix connection determines the number of identical information commands.

Pulse diagrams

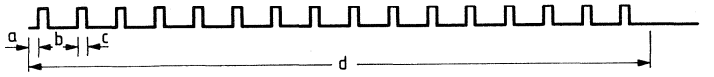
Command structure in biphase code



Time duration single bit e: $512/f_{CLK}$
presignal V: $256/f_{CLK}$
infrared interval: $5x256/f_{CLK}$

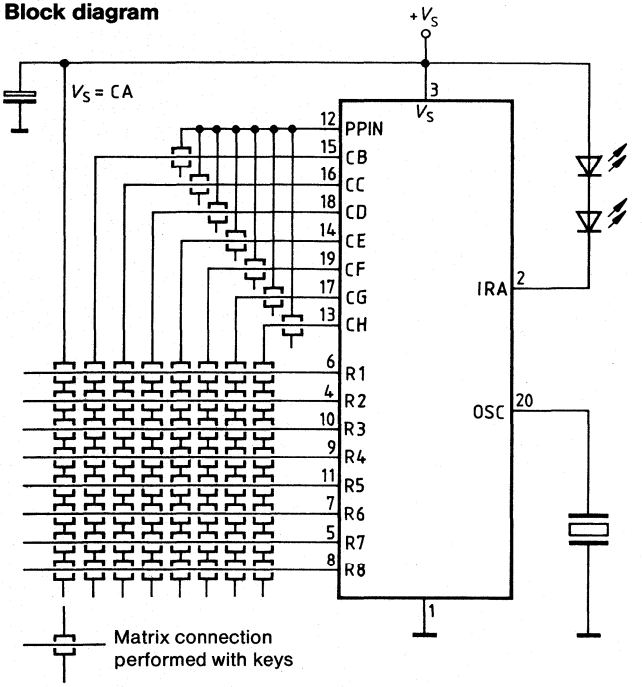
start bit S is always 1
bits A to I are addressable

Structure of the carried half bit (as well as the presignal)



$a = c = 4/f_{CLK}$
$b = 16/f_{CLK}$
$d = 256/f_{CLK}$
16 pulses per half bit

Block diagram



Truth table

No. of the command	Matrix connection row – column	Binary code IRA information command A B C D E F G H I
0	1A	0 0 0 0 0 0 0 0 0
1	1B	1 0 0 0 0 0 0 0 0
2	1C	0 1 0 0 0 0 0 0 0
3	1D	1 1 0 0 0 0 0 0 0
4	1E	0 0 1 0 0 0 0 0 0
5	1F	1 0 1 0 0 0 0 0 0
6	1G	0 1 1 0 0 0 0 0 0
7	1H	1 1 1 0 0 0 0 0 0
8	2A	0 0 0 1 0 0 0 0 0
9	2B	1 0 0 1 0 0 0 0 0
10	2C	0 1 0 1 0 0 0 0 0
11	2D	1 1 0 1 0 0 0 0 0
12	2E	0 0 1 1 0 0 0 0 0
13	2F	1 0 1 1 0 0 0 0 0
14	2G	0 1 1 1 0 0 0 0 0
15	2H	1 1 1 1 0 0 0 0 0
16	3A	0 0 0 0 1 0 0 0 0
17	3B	1 0 0 0 1 0 0 0 0
18	3C	0 1 0 0 1 0 0 0 0
19	3D	1 1 0 0 1 0 0 0 0
20	3E	0 0 1 0 1 0 0 0 0
21	3F	1 0 1 0 1 0 0 0 0
22	3G	0 1 1 0 1 0 0 0 0
23	3H	1 1 1 0 1 0 0 0 0
24	4A	0 0 0 1 1 0 0 0 0
25	4B	1 0 0 1 1 0 0 0 0
26	4C	0 1 0 1 1 0 0 0 0
27	4D	1 1 0 1 1 0 0 0 0
28	4E	0 0 1 1 1 0 0 0 0
29	4F	1 0 1 1 1 0 0 0 0
30	4G	0 1 1 1 1 0 0 0 0
31	4H	1 1 1 1 1 0 0 0 0
32	5A	0 0 0 0 0 1 0 0 0
33	5B	1 0 0 0 0 1 0 0 0
34	5C	0 1 0 0 0 1 0 0 0
35	5D	1 1 0 0 0 1 0 0 0
36	5E	0 0 1 0 0 1 0 0 0
37	5F	1 0 1 0 0 1 0 0 0
38	5G	0 1 1 0 0 1 0 0 0
39	5H	1 1 1 0 0 1 0 0 0
40	6A	0 0 0 1 0 1 0 0 0

Truth table (cont'd)

No. of the command	Matrix connection row-column	Binary code IRA information command A B C D E F G H I
41	6B	1 0 0 1 0 1 0 0 0
42	6C	0 1 0 1 0 1 0 0 0
43	6D	1 1 0 1 0 1 0 0 0
44	6E	0 0 1 1 0 1 0 0 0
45	6F	1 0 1 1 0 1 0 0 0
46	6G	0 1 1 1 0 1 0 0 0
47	6H	1 1 1 1 0 1 0 0 0
48	7A	0 0 0 0 1 1 0 0 0
49	7B	1 0 0 0 1 1 0 0 0
50	7C	0 1 0 0 1 1 0 0 0
51	7D	1 1 0 0 1 1 0 0 0
52	7E	0 0 1 0 1 1 0 0 0
53	7F	1 0 1 0 1 1 0 0 0
54	7G	0 1 1 0 1 1 0 0 0
55	7H	1 1 1 0 1 1 0 0 0
56	8A	0 0 0 1 1 1 0 0 0
57	8B	1 0 0 1 1 1 0 0 0
58	8C	0 1 0 1 1 1 0 0 0
59	8D	1 1 0 1 1 1 0 0 0
60	8E	0 0 1 1 1 1 0 0 0
61	8F	1 0 1 1 1 1 0 0 0
62	8G	0 1 1 1 1 1 0 0 0
63	8H	1 1 1 1 1 1 0 0 0

	G H I
Command 0 to 63: PPIN free	0 0 0
Command 64 to 127: PPIN connected with CB	1 0 0
Command 128 to 191: PPIN connected with CC	0 1 0
Command 192 to 255: PPIN connected with CD	1 1 0
Command 256 to 319: PPIN connected with CE	0 0 1
Command 320 to 383: PPIN connected with CF	1 0 1
Command 384 to 447: PPIN connected with CG	0 1 1
Command 448 to 511: PPIN connected with CH	1 1 1

In every command set, the assignment command – matrix connection (row – column) is analogous to the group 0 to 63.

Example:

Command 64 is generated, when PPIN is connected with CB, and R1 with CA.

MOS IC

Type	Ordering code	Package	Fig. No.
SDA 3206	Q 67100-Y 577	DIP 18	11

The SDA 3206 transmitter IC, developed in PMOS depletion technology, converts the input instructions into a 6-bit biphase code. The instructions are transmitted via an infrared transmitter stage onto an IR receiver stage of the SAB 4209.

Features

- Low current consumption of typically 3 mA (max. 5 mA). An external NPN transistor, controlled by the transmitter IC, disconnects the battery from the IC, thus substantially increasing the battery life time.
- 5 V to 10 V supply voltage

Maximum ratings

(all voltages referred to $V_{DD} = 0$ V)

Supply voltage range	V_{SS}	−0.3 to 18	V
Input voltage range	V_i	V_{SS} −18 to V_{SS} +0.3	V
Total power dissipation	P_{tot}	500	mW
Power dissipation per output	P_q	100	mW
Storage temperature range	T_{stg}	−55 to 125	°C
Thermal resitance (system-air)	$R_{th\,SA}$	90	K/W

Operating range

(referred to $V_{DD} = 0$ V)

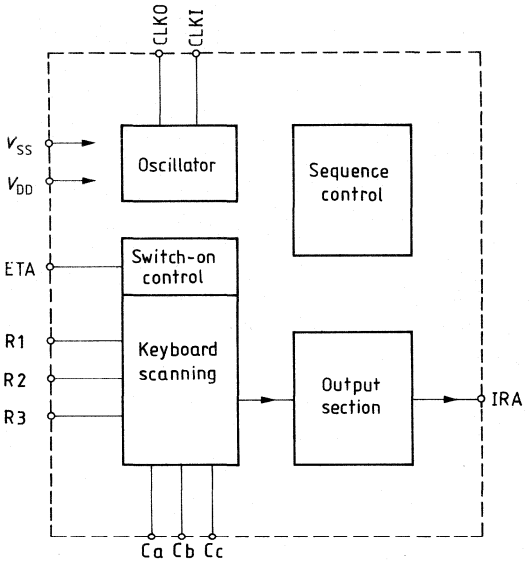
Supply voltage range	V_{SS}	5 to 10	V
Ambient temperature range	T_{amb}	0 to 70	°C

Characteristics

(all voltages referred to $V_{DD} = 0$ V)

		min.	typ.	max.	
Current consumption without load	I_{DD}		3	5	mA
Oscillator					
Clock input CLKI					
H input voltage	V_{iH}	$V_{SS}-1$		V_{SS}	V
L input voltage	V_{iL}	0		$V_{SS}-4$	V
Clock output CLKO					
H output voltage	V_{qH}	$V_{SS}-1$		V_{SS}	V
L output voltage	V_{qL}	0		+1	V
Leakage current, total current					
of column output Ca, Cb, Cc, ETA, IRA ($V_q = -10$ V; $V_{SS} = 0$ V; $T_{amb} = 25$ °C)				1	µA
Column resistors					
Ra, Rb, Rc towards $-V_S$	R_C	33		47	kΩ
Remote control signal — output IRA					
H output voltage ($I_{qH} = 4$ mA; $V_{SS} \geq 6$ V)	V_{qH}	$V_{SS}-5$		V_{SS}	V
Switch-on transistor — output ETA					
H output current ($V_q = V_{SS} - 4$ V)	I_{qH}	0.1		0.5	mA

Block diagram



Pin configuration

Pin No.	Function
1	V_{SS}
2	Column a
3	Column b
4	Column c
5	
6	V_{DD}
7	ETA (switch-on transistor output)
8	IRA (infrared output)
9	Row 1
10	Row 2
11	Row 3
12	
13	
14	
15	
16	
17	CLKI (oscillator input)
18	CLKO (oscillator output)

Pins 5, 12, 13, 14, 15, 16 are not allowed to be connected.

Description of functions

Since the SDA 3206 operates at a wide range of supply voltage with low current consumption, it is suitable for battery supply. The IC contains a control output for an NPN transistor, which disconnects the IC from the battery if the keyboard is not activated.

Input keyboard

The transmitter includes an input matrix consisting of 3 columns and 3 rows. A column output has to be connected to a row input in order to input an instruction. As a result, the transmitter is switched on and a corresponding instruction is transmitted.

End instruction

After having actuated a key, the selected instruction is transmitted maximally one more time depending on the exact instant of the release. After the last transmission of the desired instruction the end instruction is transmitted which informs the receiver that the key has been released.

Output

The transmitter converts the incoming instruction into a biphase code (timing diagram 1). Prior to the 6 information bits, a start bit is transmitted.

The output signal is keyed with the clock frequency divided by 2 ($f_{CLK}/2$ approx. 30 kHz); the signal controls an infrared transmitter stage. The idling output is high-ohmic. Prior to an IR instruction, a presignal is released which facilitates the gain control in the IR preamplifier.

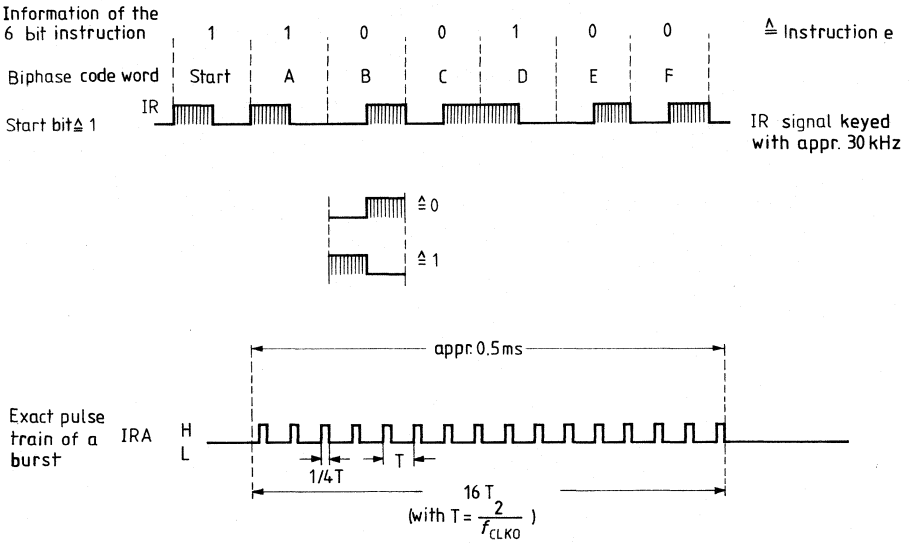
Timing

The clock frequency is set at 60 kHz. Instructions are transmitted at an interval of approx. 120 ms, with each of them lasting approx. 7 ms (timing diagram 1). The instructions cannot be recognized before a debounce time of 20 ms has elapsed.

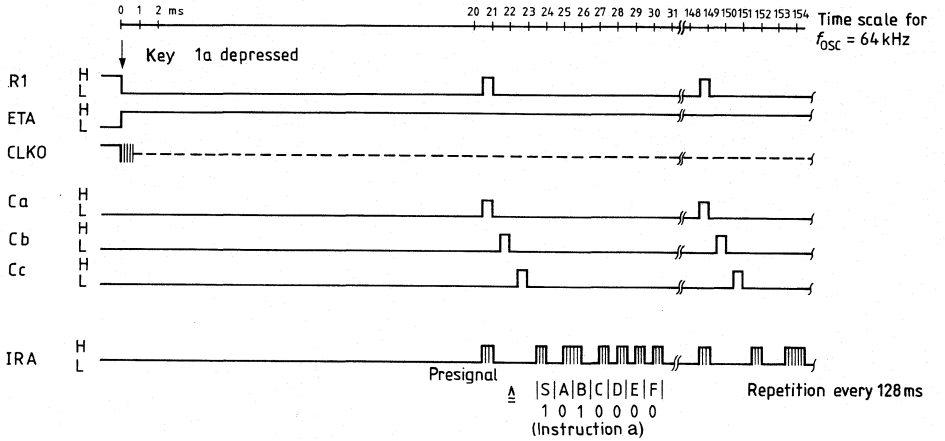
Instruction set with assignment of the instructions to the keys

Instruction	Code F E D	C B A	Logic operation
a	0 0 0	0 1 0	1c
b	0 0 0	1 0 0	2a
c	0 0 0	1 0 1	2b
d	0 0 1	0 0 0	3a
e	0 0 1	0 0 1	3b
f	1 1 1	1 1 0	End instruction

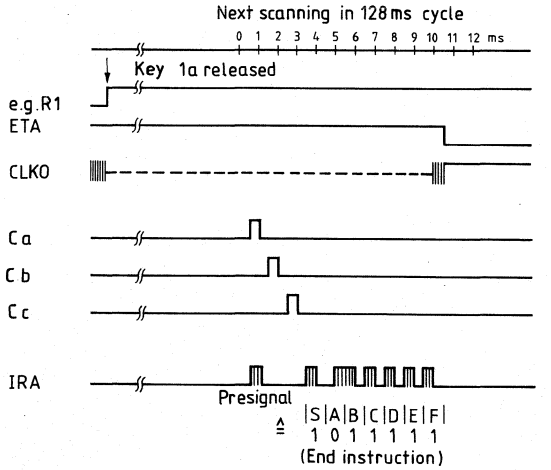
Timing diagram 1
(biphase coding without presignal)



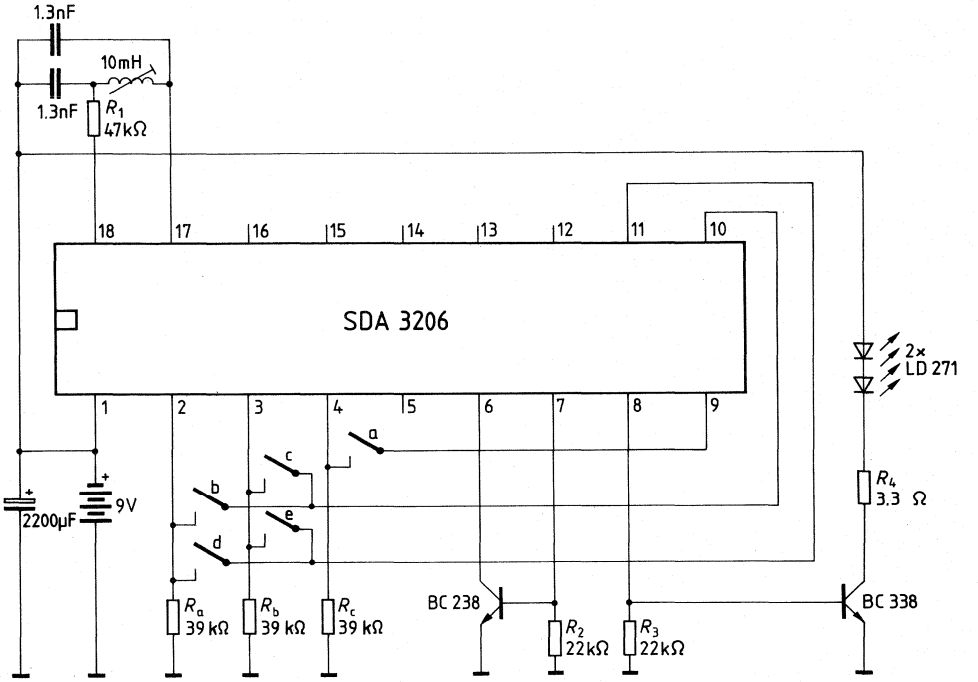
Timing diagram 2
(pressing a key)



Timing diagram 3
(releasing a key)



Typical external connection



ICs for Radiotelephone Apparatus

Bipolar IC

Type	Ordering code	Package	Fig. No.
TBB 469	Q67000-A2025	DIP 22	13

The TBB 469 is an FM narrow-band IC particularly intended for radio receivers. It is suited for the conversion, limiting, demodulation, and AF processing of an FM-modulated signal.

The input signal is routed via an RF amplifier to a crystal-controlled mixer. The IF signal is routed via an external selection to an adjustable limiter amplifier followed by a coincidence demodulator. The AF signal is routed via a low pass to an AF amplifier. Gain and frequency response of the first amplifier can be set externally. The second amplifier contains the volume control and a muting input for additional field strength-dependent regulation.

Maximum ratings

		Lower limit	Upper limit	
Supply voltage	V_S	0	15	V
Load current of V_{stab}	I_{stab}	0	50	µA
Junction temperature	T_j		125	°C
Storage temperature	T_{stg}	−55	125	°C
Thermal resistance (system-air)	$R_{th\,SA}$		70	K/W

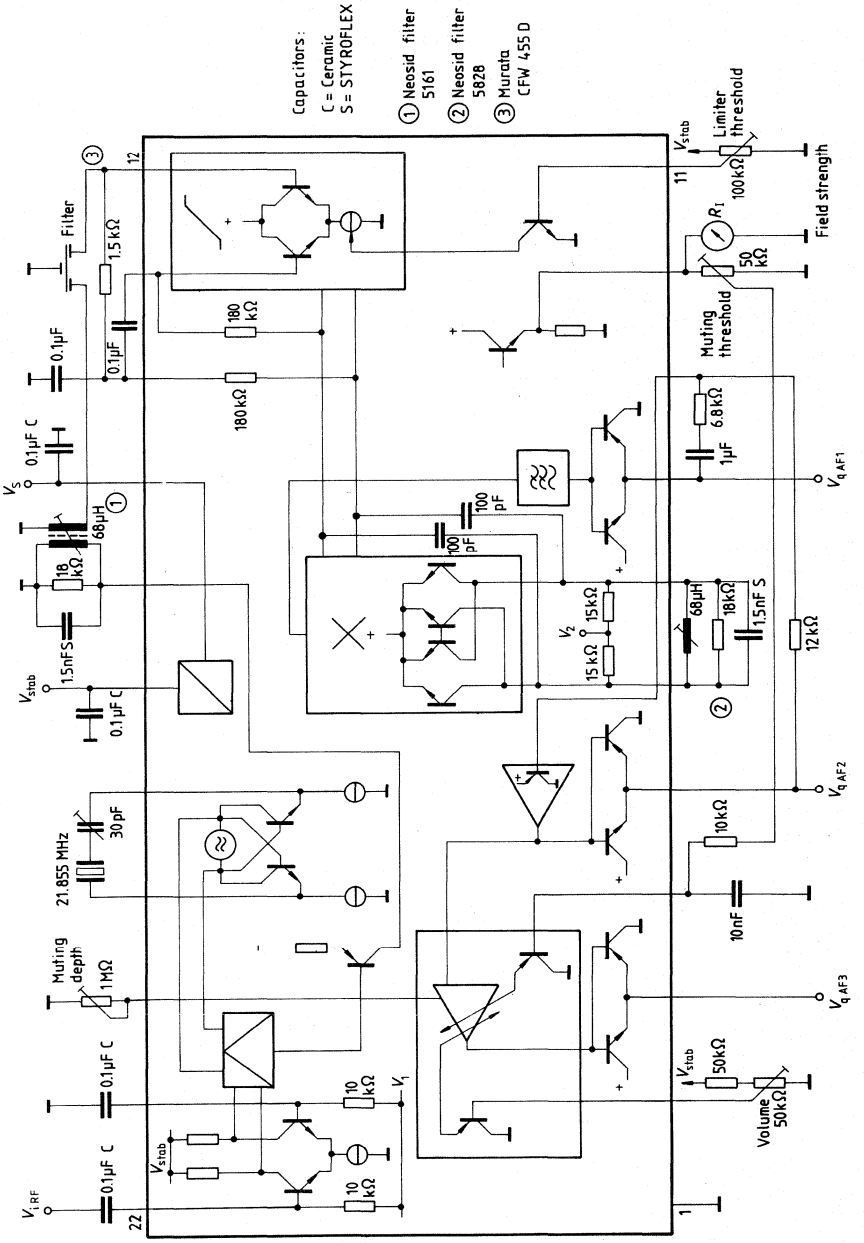
Operating range

Supply voltage	V_S	3	12	V
Ambient temperature	T_{amb}	−30	80	°C

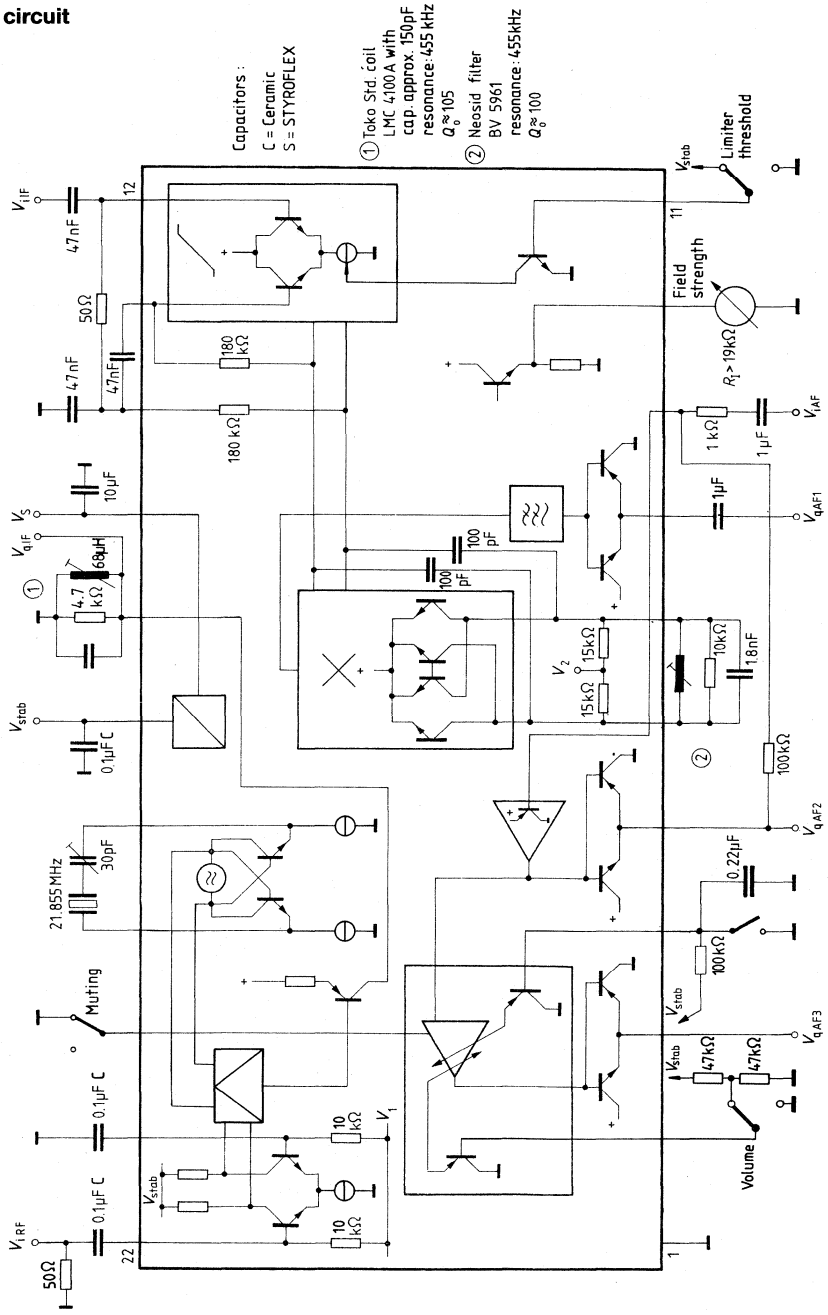
Characteristics at $V_S = 4.5$ V; $T_{amb} = -30$ °C to 60 °C		Test conditions	Lower limit	typ	Upper limit	
Supply current	I_S			3.0	5.0	mA
Reference voltage	V_{stab}		1.4	1.9	2.6	V
RF prestage						
Voltage gain	G_V	$f_I = 10...50$ MHz[1] (−3 dB)	36	42	48	dB
Input impedance	Z_i			10//3		kΩ//pF
Noise figure	NF			6		dB
IF limiter amplifier at $\Delta f = \pm 2.8$ kHz, $f_{i\,IF} = 455$ kHz $f_{mod} = 1$ kHz, $V_{i\,IF\,rms} = 10$ mV; Q factor approx. 15:						
Input resistance	R_I			20		kΩ
IF bandwidth	B_{IF}	$V_{qAF1} = -3$ dB	500			kHz
Limiter threshold	$V_{lim\,rms}$			10	20	µV
Setting range of the limiter threshold	ΔV_{lim}	$V_{10} = 0$ V/V_{stab}	16	20	24	dB
AM suppression	AMS	$m = 30\%$	40			dB
Signal-to-noise ratio	$a_{S/N}$			40		dB
Field strength	V_{10}	$V_{i\,IF} = 0$ V			100	mV
	V_{10}	$V_{i\,IF} = 10$ mV	0.8	1.2		V
AF output voltage	V_{QAF1}		30	60		mV
Min. load resistance	R_{q1}		300			Ω
AF bandwidth	B_{AF}	$V_{qAF1} = -3$ dB	20	35		kHz
Total harmonic distortion	THD			1	2	%
AF amplifier 2						
Voltage gain	G_V	$V_{i\,AF} = 1$ mV	31	37	43	dB
Min. load resistance	R_{q2}		1			kΩ
Input impedance	R_I		10			kΩ
Signal-to-noise ratio	$a_{S/N}$			40		dB
Total harmonic distortion[1]	THD			2		%
AF amplifier 3						
Voltage gain	G_V	$V_2 = 0$ V, $V_{11} = 1$ V		10		dB
Max. output voltage	$V_{q\,AF3\,rms}$	$THD = 10\%$			300	mV
Min. load resistance	R_{q3}		5			kΩ
Total harmonic distortion	THD			2		%
Volume control range	ΔG_{vol}			80		dB
Muting depth	M	$V_4 = 0$ V/1 V				
		$R_{mute} = \infty$	3	6	10	dB
		$R_{mute} = 0$	20	26	40	dB
Noise voltage in acc. with DIN 45405[2]	V_n	$V_2 = 1/2\ V_{stab}$		30		μV_{0S}

1) dependent on external components
2) AQL = 2.5

Application circuit



Test circuit



Bipolar IC

Type	Ordering code	Package	Fig. No.
TBB 1469	Q67000-A1909	DIP 16	8

The TBB 1469 is an FM narrow-band IC particularly intended for radio receivers. It is suited for the conversion, limiting, demodulation, and AF processing of an FM-modulated signal. The input signal is routed via an AF amplifier to a crystal-controlled mixer. The IF signal is routed via an external selection to a limiter amplifier followed by a coincidence demodulator. The AF signal is routed via a low pass to an externally adjustable AF amplifier. ESD protective diodes are internally connected to the RF inputs.

Maximum ratings

		Lower limit	Upper limit	
Supply voltage	V_S	0	15	V
Load current	I_{stab}	0	50	µA
Junction temperature	T_j		125	°C
Storage temperature	T_{stg}	−40	125	°C
Thermal resistance (system-air)	$R_{th\,SA}$		85	K/W

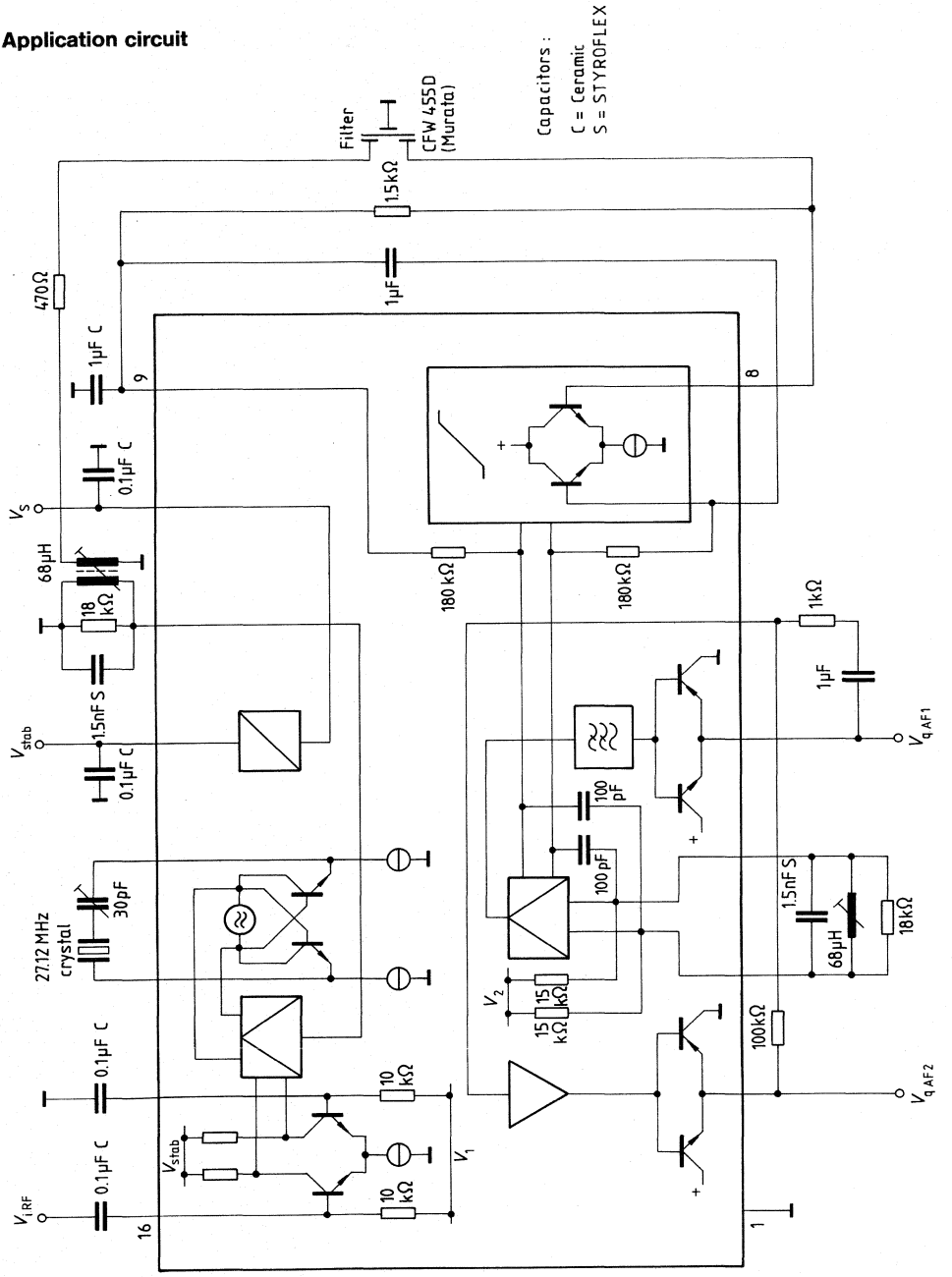
Operating range

Supply voltage	V_S	3	12	V
Ambient temperature	T_{amb}	−30	80	°C

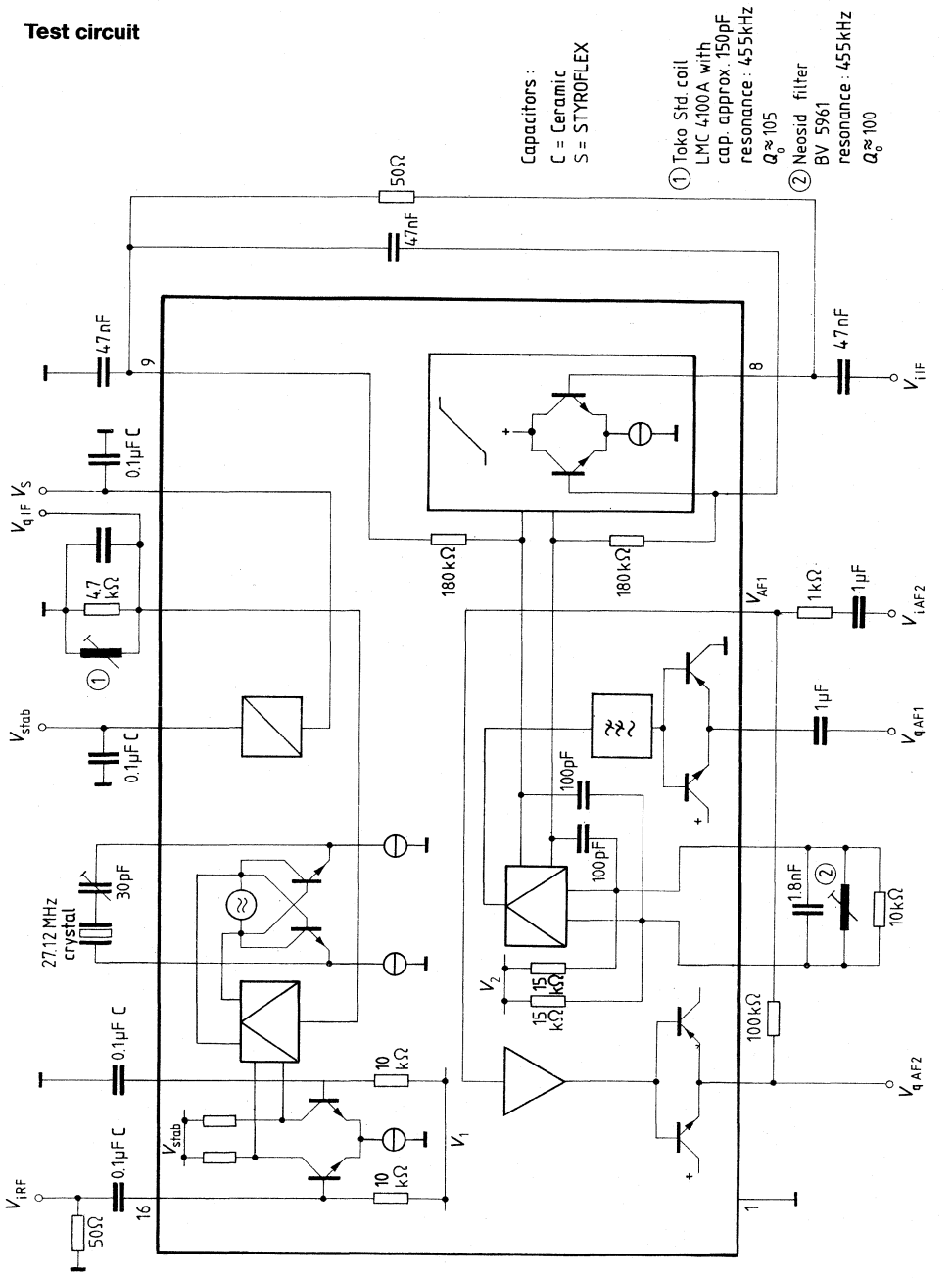
Characteristics V_S=4.5 V; T_{amb}=−30 °C to 60 °C		Test conditions	Lower limit	typ	Upper limit	
Supply current	I_S			2.7	4.0	mA
Reference voltage	V_{stab}		1.4	1.9	2.6	V
RF prestage						
Voltage gain	G_V	f_i = 10...50 MHz[1] (−3 dB)	36	42	48	dB
Input impedance	Z_i			10//3		kΩ//pF
Noise figure	NF			6		dB
IF limiter amplifier at $\Delta f = \pm$ 2.8 kHz, $f_{i\,IF}$ = 455 kHz f_{mod} = 1 kHz, $V_{i\,IF\,rms}$ = 10 mV; Q factor approx. 15						
Input resistance	R_i			20		kΩ
IF bandwidth	B_{IF}	V_{qAF1} = −3 dB	500			kHz
Limiter threshold	$V_{lim\,rms}$			10	30	µV
AM suppression	AMS	m = 30%	40			dB
AF output voltage	V_{qaF1}		30	60		mV
Min. load resistance	R_q		300			Ω
Total harmonic distortion	THD			1	2	%
Signal-to-noise ratio	$a_{S/N}$			40		dB
AF bandwidth	B_{AF}	V_{qAF1} = −3 dB	20	35		kHz
AF amplifier						
Voltage gain	G_V	V_{iAF} = 1 mV	31	37	43	dB
Min. load resistance	R_L		1			kΩ
Input impedance	R_i		10			kΩ
Signal-to-noise ratio	$a_{S/N}$			40		dB

1) dependent on external components

Application circuit



Test circuit



Preliminary data **Bipolar IC**

Type	Ordering code	Package	Fig. No.
TBB 2469 G	Q67000-A2392	MIDIP 20 (S0 20 L)	28

The TBB 2469 G is an FM narrow-band IC particularly intended for radio receivers. It is suited for the conversion, limiting, demodulation, and AF processing of an FM-modulated signal.

The input signal is routed via an HF amplifier to a crystal-controlled mixer. The IF signal is routed via an external selection, to a limiter amplifier followed by a coincidence demodulator. The AF signal is routed via a low pass to an AF amplifier. Gain and frequency response of the first amplifier can be set externally. The second amplifier contains the volume control.

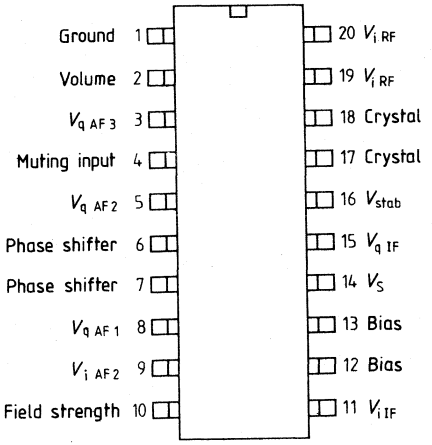
Maximum ratings

		Lower limit	Upper limit	
Supply voltage	V_S	0	15	V
Load current of V_{stab}	I_{Stab}	0	50	µA
Junction temperature	T_j		125	°C
Storage temperature	T_{stg}	−40	125	°C
Thermal resistance (system-air)	$R_{th\,SA}$		120	K/W

Operating range

Supply voltage	V_S	3	12	V
Ambient temperature	T_{amb}	−30	80	°C

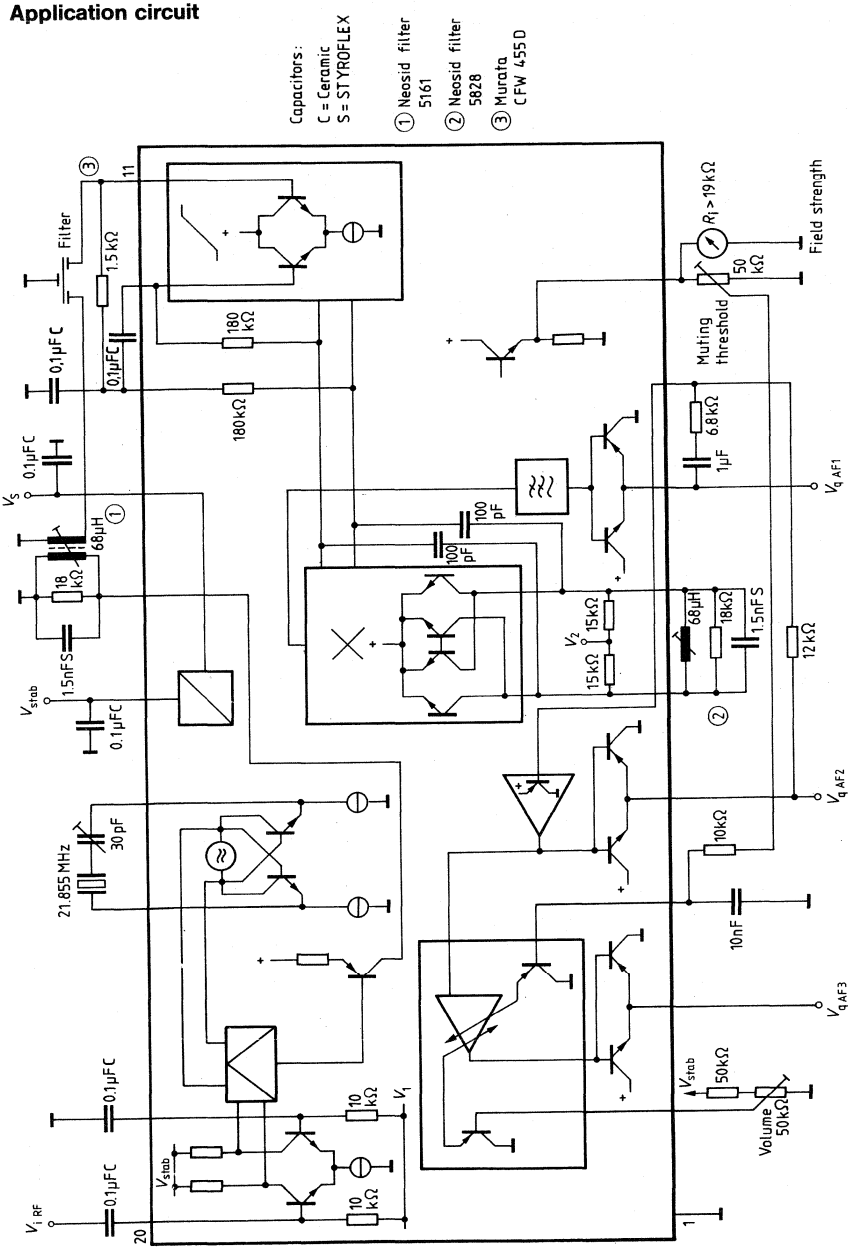
Pin configuration
top view



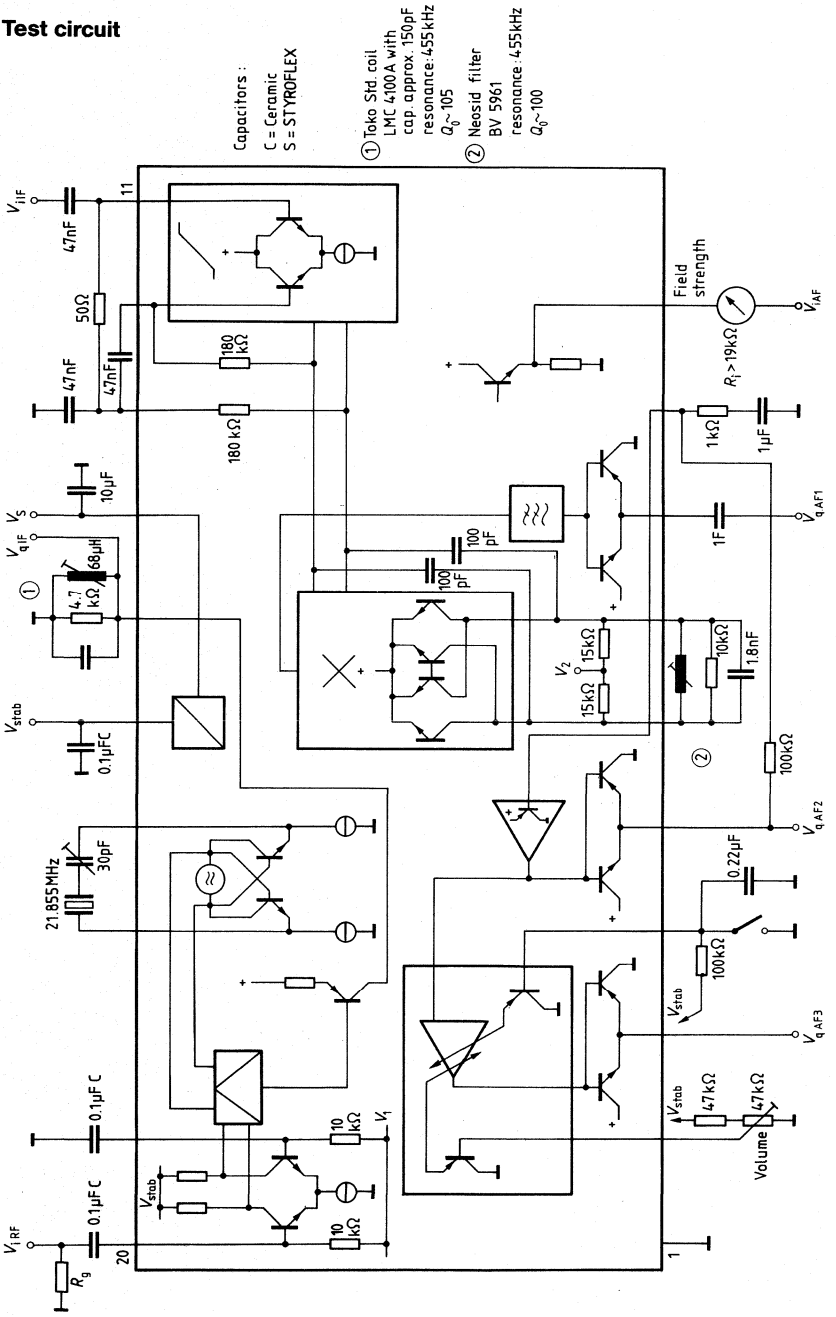
Characteristics at V_S=4.5V, T_{amb}=−30°C to 60°C		Test conditions	Lower limit	typ	Upper limit	
Current consumption	I_S			3.0	5.0	mA
Reference voltage	V_{stab}		1.4	1.9	2.6	V
RF prestage						
Voltage gain	G_V	f_i=10...50 MHz[1] (−3 dB)	36	42	48	dB
Input impedance	Z_i			10//3		kΩ//pF
Noise figure	NF			6		dB
IF limiter amplifier at $\Delta f = \pm$ 2.8 kHz, $f_{i\,IF}$ = 455 kHz[1] f_{mod} = 1 kHz, $V_{i\,IF\,rms}$ = 10 mV, Q factor appr. 15						
Input resistance	R_i			20		kΩ
IF bandwidth	B_{IF}	$V_{q\,AF1}$ = −3 dB	500			kHz
AM suppression	AMS	m = 30%	40			dB
Signal-to-noise ratio	$a_{S/N}$			40		dB
Field strength	V_{i0}	$V_{i\,IF}$ = 0 V			100	mV
	V_{10}	$V_{i\,IF}$ = 10 mV		1.9		V
AF output voltage	$V_{q\,AF1}$		30	60		mV
Min. load resistance	R_{q1}		300			Ω
AF bandwidth	B_{AF}	$V_{q\,AF1}$ = −3 dB	20	35		kHz
Total harmonic distortion[1]	THD			1	2	%
AF amplifier 2						
Voltage gain	G_V	$V_{i\,AF1}$ = 1 mV		37		dB
Min. load resistance	R_{q2}		1			kΩ
Input impedance	R_i		10			kΩ
Signal-to-noise ratio	$a_{S/N}$			40		dB
Total harmonic distortion[1]	THD			2		%
AF amplifier 3						
Voltage gain	G_V	V_2 = 0 V, V_{11} = 1 V		10		dB
Max. output voltage	$V_{q\,AF3\,rms}$	THD = 10%			300	mV
Min. load resistance	R_{q3}		5			kΩ
Total harmonic distortion[1]	THD			2		%
Volume control range	ΔG_{vol}			80		dB
Noise voltage in acc. with DIN 45405[2]	V_n	V_2 = 1/2 V_{stab}		20	50	μV_{0s}

1) dependent on external components
2) AQL = 2.5

Application circuit



Test circuit



Preliminary data **CMOS IC**

Type	Ordering code	Package	Fig. No.
TBB 146	Q67100-Y914	DIP 20	12

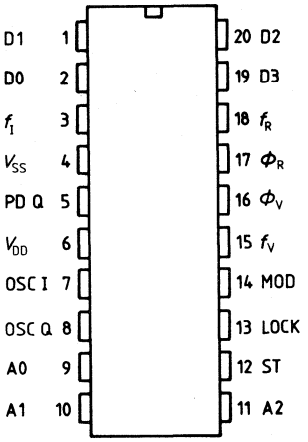
The TBB 146 is a highly integrated CMOS PLL component that can be programmed via a 4-bit data bus and exhibits the following technical features:

- Supply voltage range 3 to 6 V
- Cutoff frequency of 15 MHz for 5 V supply
- Internal or external reference oscillator
- Programmable division ratios
  reference frequency divider from 3 to 4095
  comparison frequency divider from 3 to 4095 and 1 to 127
- Dual-modulus operation
- Programming of frequency dividers via a 4-bit data bus
- Anti-backlash phase detector and lock detector
- Function and pin-compatible with MC 145146
  (with the exception of the supply voltage 3 V to 6 V compared to 3 V to 9 V)

Applications

- AM/FM radios
- Cordless telephones
- Multichannel equipment
- Navigation equipment
- CB and amateur radio

Pin configuration
top view



Inputs			Outputs		
Symbol	Pin No.	Function	Symbol	Pin No.	Function
A 0	9	Adress inputs	f_R	18	Frequency divider outputs
A 1	10		f_V	15	
A 2	11		LOCK	13	Lock detector output
D 0	2	Data inputs	MOD	14	Switching pulse for prescaler (modulus control)
D 1	1				
D 2	20				
D 3	19		OSC Q	8	Oscillator output
f_I	3	Comparison frequency	PD Q	5	Tristate output of phase detector
OSC I	7	Reference frequency			
			Φ_R	17	Phase detector outputs
			Φ_V	16	
			ST	12	Transfer signal for programming (ST = H)

Circuit description

At the beginning of the count cycle the frequency dividers are set to the set values.

The VCO divider *A* counts from the programmed value to 0 and, after reaching the value 0, switches the MOD output to H. The MOD output is reset to L when the VCO divider *N* reaches a value of 0. The dividers are subsequently set anew and the procedure is repeated.

In dual-modulus operation the MOD output can be used to control a prescaler (*P* for H, *P*+1 for L). The effective overall division ratio is thus $N_T = N \times P + A$. If A is counted up from 0 to *N*−1 for each value of *N*, finer resolution is possible than in signal-modulus operation.

The reference frequency can be fed in by connecting an oscillator at OSC I, or it can be generated internally by connecting a crystal (plus capacitors to V_{SS}) to the pins OSC I and OSC Q.

At the beginning of the count cycle the reference divider is set to the set value (latches 5 through 7). When it reaches 0 it is programmed anew and the procedure is repeated.

The divider outputs f_R and f_V drive the phase and lock detector, in which the following output signals are produced:

Input conditions	PD Q	LOCK
Frequency $f_V > f_R$	negative pulses	negative pulses
Frequency $f_V < f_R$	positive pulses	negative pulses
Frequency and phase coincidence $f_V = f_R$	high impedance	sustained positive signal

To prevent backlash as a result of the high-impedance state of the PD Q output, short output pulses are generated for each count cycle at PD Q depending on V_{DD} and V_{SS} and V_{SS} and with Φ_R, Φ_V and LOCK on V_{SS}.

Maximum ratings

		Condition	Lower limit	Upper limit	
Supply voltage	V_{DD}	referred to $V_{SS}=0$	−0.3	7	V
Input voltage	V_{IM}		−0.3	V_{DD}+0.3	V
Total dissipation	P_{tot}			500	mW
Dissipation per output	P_Q			100	mW
Junction temperature	T_j			125	°C
Storage temperature	T_{stg}		−55	125	°C
Thermal resistance (system-air)	$R_{th\,SA}$			75	K/W

Operating range

		Test conditions	Lower limit	Upper limit	
Supply voltage	V_{DD}	referred to $V_{SS}=0$	3	6	V
Open-loop current	I_{DD}	$V_{DD}=6$ V (outputs not wired)		3.2	mA
Operating temperature	T_{amb}		−40	85	°C

Characteristics

$V_{DD}=5$ V; $T_{amb}=25$ °C; voltages referred to $V_{SS}=0$ V

		Test conditions	Lower limit	Upper limit	
H input voltage	V_{IH}		0.7 V_{DD}		V
L input voltage	V_{IL}			0.3 V_{DD}	V
H output voltage at LOCK, OSC Q, PD Q	V_{QH}	$V_I=V_{DD}$ or V_{SS}	V_{SS}−0.05		V
L output voltage at LOCK, OSC Q, PD Q	V_{QL}	$V_I=V_{DD}$ or V_{SS}		V_{SS}+0.05	V
Input current	I_I			1	µA
H output current at f_R, f_V, Φ, LOCK, PD Q	I_{QH}	$V_Q=4.6$ V; $TC=-0.35\%/K$	−0.51		mA
L output current at f_R, f_V, Φ, LOCK, PD Q	I_{QL}	$V_Q=0.4$ V; $TC=-0.35\%/K$	0.51		mA
Output current at PD Q	I_{IL}	PD Q in high impedance state, $V_{DD}=6$ V		± 0.5	µA
Transition time at f_R, f_V, Φ, LOCK PD Q	t_{QLH},t_{QHL}	$C_{ch}=50$ pF		100	ns
Pulse width at ST, D, A	t_W		35		ns
Output pulse width PD Q, Φ, f_R, f_V	t_{QW}		50	150	ns
Input capacitance	C_I	$V_I=0$ V		5	pF
Output capacitance OSC Q	C_Q			6	pF

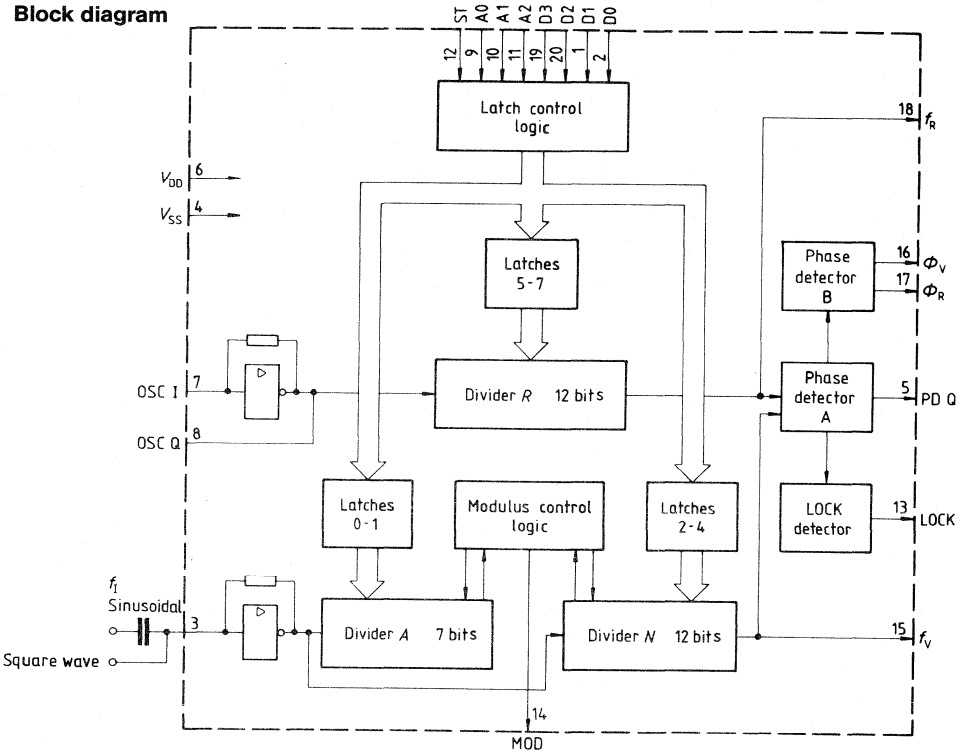
Characteristics

$V_{DD} = 5$ V; voltages referred to $V_{SS} = 0$ V

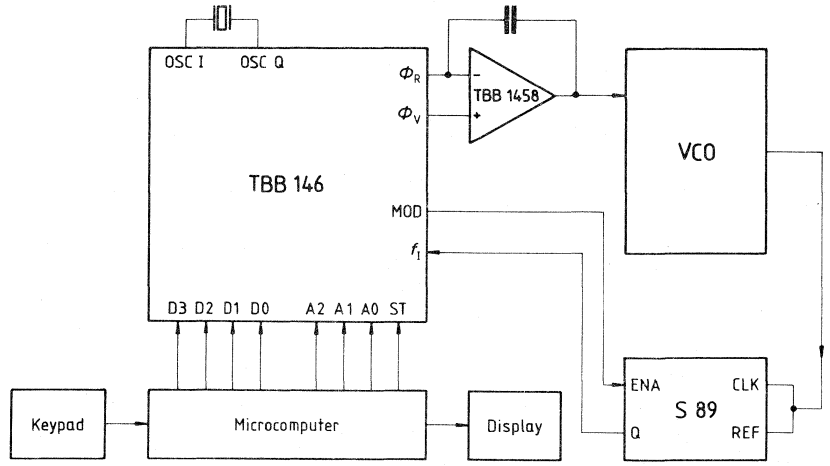
		Test conditions	−40 °C		25 °C		85 °C		
			B	A	B	A	B	A	*)
Comparison frequency f_I									
H input current	I_{IH}	$V_{DD} = 6$ V		15		10		8	µA
L input current	I_{IL}	$V_{DD} = 6$ V		15		10		8	µA
H pulse width	t_{WH}		25		33		33		ns
L pulse width	t_{WL}		25		33		33		ns
H-L transition time	t_{THL}					4			µs
L-H transition time	t_{TLH}					4			µs
Operating frequency	f	square wave signal V_{DD}–V_{SS}		19		15		15	MHz
	f	sinusoidal signal (peak to peak) 500 mV		18		15		15	MHz
Input capacitance	C_I	to V_{SS}		7		7		7	pF
Reference frequency OSC I									
H input current	I_{IH}	$V_{DD} = 6$ V		15		10		8	µA
L input current	I_{IL}	$V_{DD} = 6$ V		15		10		8	µA
H pulse width	t_{WH}		15		18		23		ns
L pulse width	t_{WL}		15		18		23		ns
H-L transition	t_{THL}					4			µs
L-H transition	t_{TLH}					4			µs
Operating frequency	f	square wave signal V_{DD}–V_{SS}		33		27		21	MHz
	f	sinusoidal signal (peak to peak) 500 mV		20		17		15	MHz
Input capacitance	C_I	to V_{SS}		7		7		7	pF
Modulus control MOD									
H output current	I_{QH}	$V_{QH} = 4.6$ V	0.45		−0.75		0.23		mA
L output current	I_{QL}	$V_{QL} = 0.4$ V	0.90		1.5		0.45		mA
H-L transition time	t_{QHL}	$C_{ch} = 50$ pF				100			ns
L-H transition time	t_{QLH}	$C_{ch} = 50$ pF				100			ns
H-L delay time	t_{dQHL}	ref. to f_I				35			ns
L-H delay time	t_{dQLH}	ref. to f_I				35			ns

*) B = lower limit
A = upper limit

Block diagram



Schematic circuit diagram

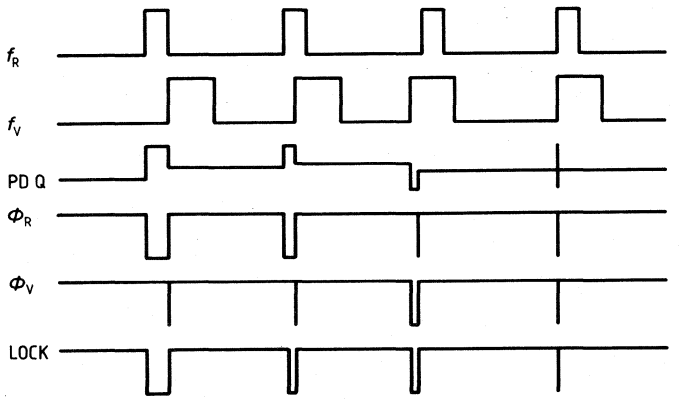


Programming table

Address inputs			Selected latch	Divider	Data inputs			
A 2	A 1	A 0			D 0	D 1	D 2	D 3
0	0	0	0	*A*	0	1	2	3
0	0	1	1	*A*	4	5	6	—
0	1	0	2	*N*	0	1	2	3
0	1	1	3	*N*	4	5	6	7
1	0	0	4	*N*	8	9	10	11
1	0	1	5	*R*	0	1	2	3
1	1	0	6	*R*	4	5	6	7
1	1	1	7	*R*	8	9	10	11

The input data is transferred by the strobe signal (ST = H).

Pulse scheme, phase and lock detector



Bipolar IC

Type	Ordering code	Package	Fig. No.
S 89	Q67000-H1694	DIP 14	7

Frequency divider with the preselectable divider ratios 50/51, 100/101, 100/102, 200/202.

Maximum input frequency is 500 MHz for divider ratios 100/102 and 200/202, or 250 MHz for divider ratios 50/51 and 100101. The S 89 is particularly intended as prescaler for the S 187 B.

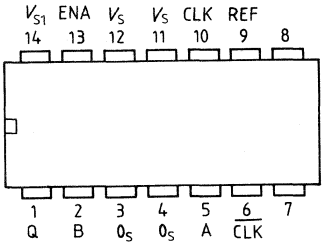
Main application: Prescaler in dual-modulus frequency dividers.

Maximum ratings

		Lower limit B	Upper limit A	
Supply voltage	V_S	−0.3	7	V
Input voltage ENA	V_I	−0.3	15	V
Input voltage A, B	V_I	−0.3	7	V
Input voltage CLK	V_I	−0.3	V_S+0.3	V
Output voltage Q1, output disabled	V_{Q1}	−0.3	12	V
External voltage at REF	V_I	−0.3	V_S+0.3	V
Output current at Q1, output conducting, V_{S1} open	I_{Q1}		4	mA
Junction temperature	T_j		125	°C
Storage temperature	T_{stg}	−55	125	°C
Ambient temperature during operation	T_{amb}	−30	80	°C
Thermal resistance (system-air)	$R_{th\,SA}$		75	K/W

Operating range		Conditions	Lower limit B	Upper limit A	
Supply voltage	V_S		4.5	5.5	V
Input frequency	f_{CLK}	ratios 50/51, 100/101		300[1]	MHz
Input frequency	f_{CLK}	ratios 100/102, 200/202		500[1]	MHz
Input frequency, sinusoidal	f_{CLK}	ratios 50/51, 100/101	20[1]		MHz
Input frequency, sinusoidal	f_{CLK}	ratios 100/102, 200/202	20[1]		MHz

Pin configuration
top view



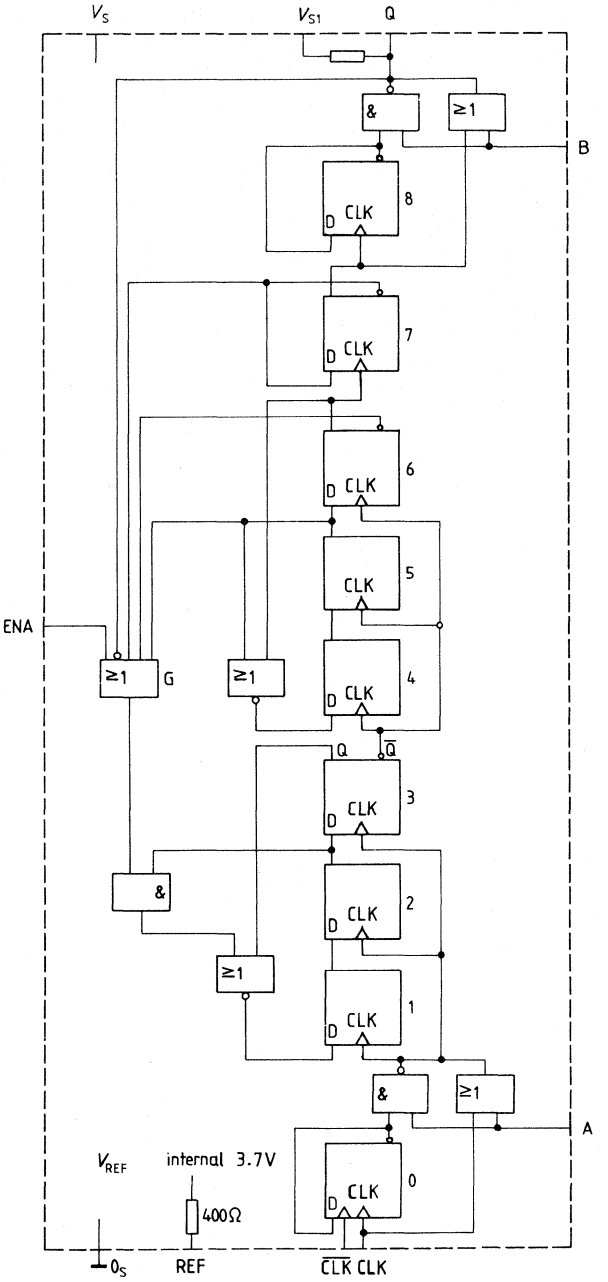
1) Amplitude (peak-to-peak) at CLK: 250 mV ≤ V_{CLKpp} ≤ 400 mV; V_S 4.75 ≤ V_S ≤ 5.5 V.

Characteristics $V_S = 5$ V; $T_{amb} = -30$ °C to 80 °C		Test conditions	Lower limit B	typ	Upper limit A	
Supply voltage	V_S		4.75	5	5.25	V
Supply current	I_S	inputs and outputs open		55	85	mA
L input voltage at ENA	V_{IL}				1	V
H input voltage at ENA	V_{IH}	$T_{amb} = -30$ °C	3.2			V
H input voltage at ENA	V_{IH}	$T_{amb} = 25$ °C	3.0			V
H input voltage at ENA	V_{IH}	$T_{amb} = 80$ °C	2.8			V
H input current at ENA	I_{IH}	$V_{ENA} = V_{ENA\,H}$ versus T_{amb}		0.17	0.3	mA
H input current at ENA	I_{IH}	$V_{ENA} = 9$ V		1.7	3	mA
L input voltage at A or B	V_{IL}				1.5	V
H input voltage at A or B	V_{IH}		$V_S-0.1$		$V_S+0.1$	V
H input current at A or B	I_{IH}	$V_{AB} = V_S$		0.5	1	mA
Threshold voltage at CLK	V_{CLK}	$V_S = 5$ V		3.7		V
Switching voltage deviation at CLK, static (CLK and REF connected)	$V_{CLK\,pp}$		250		1600	mV
Switching voltage deviation at CLK 500 MHz (CLK and REF connected)	$V_{CLK\,pp}$	$V_S = 5$ V	250		400	mV
Output voltage at Q	V_Q	$I_{Q1} = 3.2$ mA			0.5	V
	V_Q	$V_{S1} = 11.5$ V $I_{S1} < 100$ µA			2	V
R between Q and V_{S1}	R_Q	$T_{amb} = 25$ °C	2.0	2.5	3.2	kΩ

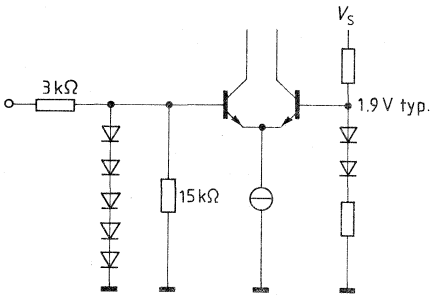
Truth table

A	B	ENA	f_{CLK}/f_Q	Input frequency MHz min	max
H	H	H	200	40	500
H	H	L	202		
H	L	H	100		
H	L	L	102		
L	H	H	100	20	250
L	H	L	101		
L	L	H	50		
L	L	L	51		

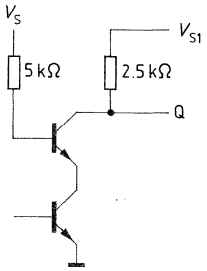
Block diagram



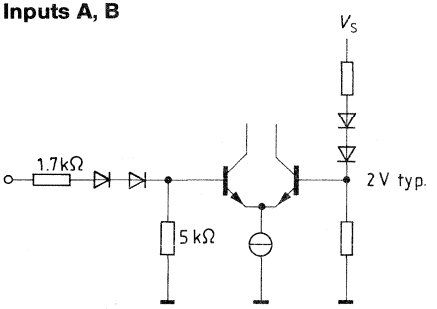
Input ENA



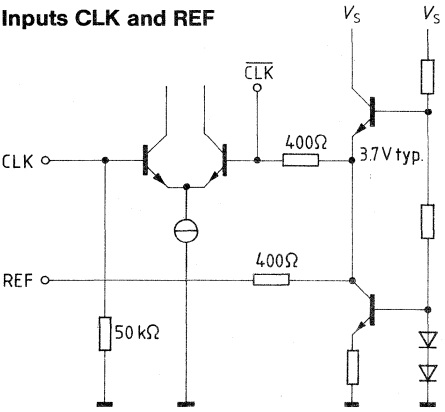
Outputs Q and V_{S1}



Inputs A, B

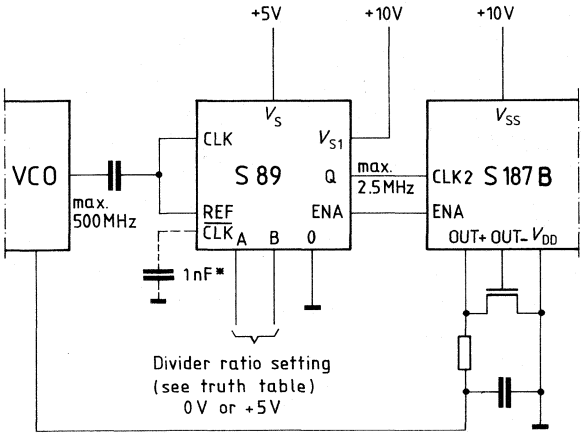


Inputs CLK and REF



Typical application

Prescaler for PLL circuits S 187 B/C



*) Capacitor is only necessary for operation close to the maximum frequency and maximum input sensitivity

MOS IC

Type	Ordering code	Package	Fig. No.
S 187 B S 187 C	Q67100-Y199 Q67100-Y868	DIP 28	16

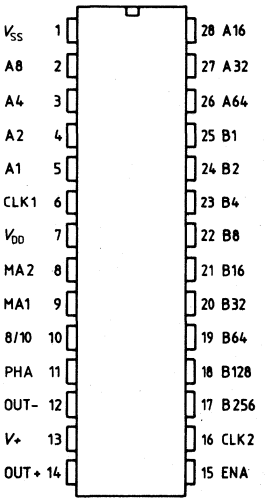
The S 187 is a MOS circuit using p-channel metal-gate technology with enhancement and depletion transistors, featuring the following special characteristics:

- More than 500 000 different frequencies presettable
- 8 different reference frequencies presettable
- High degree of flexibility by appropriate coding
- High reference input frequency
- Integrated phase comparator
- Simple 10 V supply
- Low power dissipation even at high frequencies
- Programmable diode matrix S 353 particularly suitable to set the frequency
- Prescaler S 89 particularly suitable for extension up to 500 MHz.

Possible applications

- Multichannel equipment
- Navigation equipment
- Citizen band radio
- Scanning receiver
- Signal generators

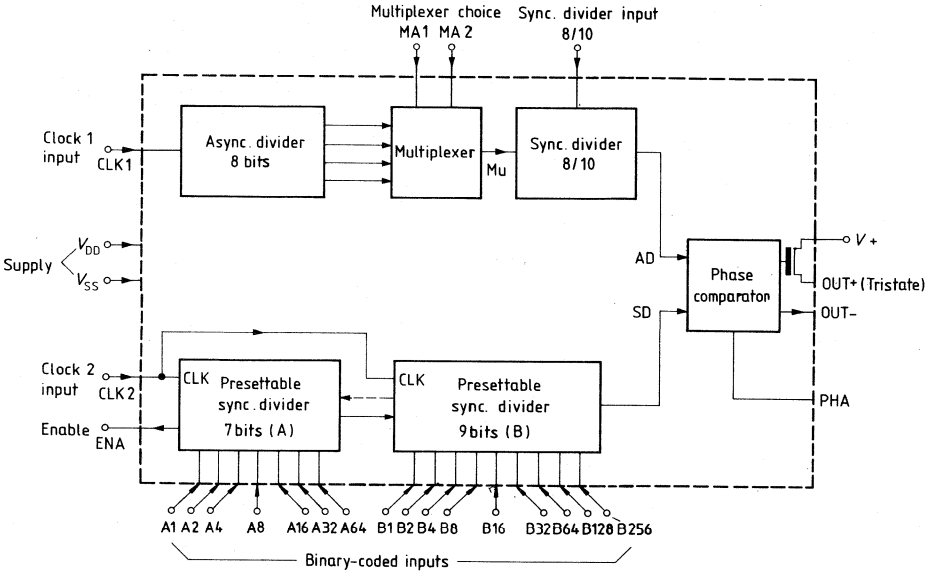
Pin configuration
top view



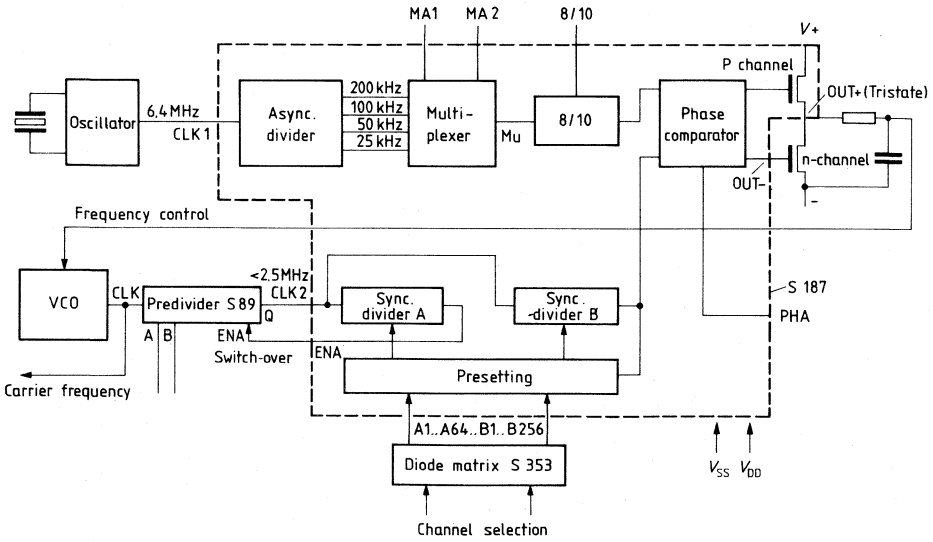
Pin configuration

Inputs			Outputs		
Abbrev.	Pin		Abbrev.	Pin	
A 1	5	Binary-coded inputs for presettable sync divider (A) 7 bits	ENA	15	Enable output
A 2	4		PHA	11	Phase comparator output
A 4	3				
A 8	2				
A 16	28				
A 32	27				
A 64	26				
B 1	25	Binary-coded inputs for presettable sync divider (B) 9 bits			
B 2	24				
B 4	23				
B 8	22				
B 16	21				
B 32	20				
B 64	19				
B 128	18				
B 256	17		OUT +	14	Drain connection of an external enhancement n-channel MOS transistor to form a tristate stage
CLK 1	6	Clock input 1 for async divider (max. 6.4 MHz)			
CLK 2	16	Clock input 2 for sync divider (max. 2.5 MHz)			
8/10	10	Divider setting 8 or 10 for async divider	OUT −	12	Gate connection for external n-channel MOS FET
MA 1	9	Multiplexer choice 1 and 2			
MA 2	8		*V*+	13	Source connection of the internal p-channel MOS FET Connection of an additionally filtered voltage to reduce noise at the low pass
V_{SS}	1	Supply voltages			
V_{DD}	7				

Block diagram



Block diagram of a carrier frequency generator with S 89, S 187 B and S 353



Maximum ratings		Test conditions	Lower limit B	Upper limit A	
Supply voltage	V_{DD}	referred to $V_{SS}=0$ V	−15	0.3	V
Voltage at all pins	V	referred to $V_{SS}=0$ V	−15	0.3	V
Junction temperature	T_j			125	°C
Storage temperature	T_{stg}		−40	125	°C
Ambient temperature					
S 187 B	T_{amb}		−20	70	°C
S 187 C	T_{amb}		−30	80	°C
Thermal resistance (system-air)	$R_{th\,SA}$			55	K/W

Electrical characteristics $V_{SS}=10$ V in temperature range		Test conditions	Lower limit B	typ	Upper limit A	
Supply voltage $V_{SS\,typ}=10$ V	V_{SS}	$V_{DD}=0$ V used as grounding pin and reference voltage	9	10	11	V
Supply current	I_{SS}			8	35	mA
Inputs						
A 1 to A 64						
B 1 to B 256, 8/10						
L resistance	R_{IL}	$C_{in}=10$ pF to V_{SS}	0		3	kΩ
H resistance	R_{IH}		100		∞	kΩ
Input current	I_{IL}	(short circuit to V_{DD} at $V_{SS}=10$ V)			500	µA
Input CLK 1						
L input voltage	V_{IL}		V_{DD}		$V_{SS}-8$	V
H input voltage	V_{IH}		$V_{SS}-0.5$		V_{SS}	V
Input CLK 2						
L input voltage	V_{IL}		V_{DD}		$V_{SS}-8$	V
H input voltage	V_{IH}		$V_{SS}-0.5$		V_{SS}	V
Inputs MA 1, MA 2						
L input voltage	V_{IL}	$C_{in}=10$ pF	V_{DD}		$V_{SS}-8$	V
H input voltage	V_{IH}	to V_{SS}	$V_{SS}-0.5$		V_{SS}	V
Outputs OUT+, OUT−						
L output voltage	V_{QL}	$I_{QL}=1$ mA, $V_{SS}=10$ V	9			V
H output voltage	V_{QH}	$I_{QH}=-1$ mA, $V_{SS}=10$ V			4	V
L/H output current	I_Q	$T_{amb}=70$ °C			1	µA
Output PHA						
L output voltage	V_{QL}	$I_{QL}=100$ µA, $V_{SS}=10$ V			6.5	V
H output voltage	V_{QH}	$I_{QH}=-1$ mA, $V_{SS}=10$ V	6.5			V
Output ENA (open drain)						
Leakage current	I_{QR}	output low			20	µA
H output voltage	V_{QH}	$I_{QH}=3.5$ mA, $V_{SS}=10$ V	5			V

Dynamic characteristics $V_{SS} = 10$ V; $T_{amb} = -20$ °C to 70 °C		Test conditions	Lower limit B	Upper limit A	
Input frequency	f				
at CLK 1				6.5	MHz
at CLK 2				2.5	MHz
Input pulses	t_I				
at CLK 1		$C_{in} = 15$ pF	50		ns
at CLK 2		to V_{SS}	150		ns
Signal transition time	t_T				
at CLK 1			25		ns
at CLK 2			150		ns
Propagation delay ENA to falling edge of CLK 2	t_P			300	ns

Basic function

The frequency synthesizer S 187 is used for channel selection in the carrier frequency generator. The carrier frequency is generated by a voltage-controlled oscillator (VCO) and after a **preset division** (depending on channel) compared with a crystal-stabilized reference frequency. The output voltage of the frequency comparator controls the VCO.

By appropriate choice of the division rate, the carrier frequency can be set to a particular multiple of the reference frequency.

Construction and functions

Refer to the block diagram of a carrier frequency generator, specifying the unit integrated in the S 187.

The following functions are included:

1. 8-stage async divider, input frequency 6.4 MHz max., output frequency selectable 200, 100, 50, 25 kHz.
2. switchable 8/10 divider.
   1) and 2) together supply the crystal-stabilized reference frequency (8 possibilities).
3. fully programmable sync divider consisting of two interconnected dividers A and B; input frequency ≤ 2.5 MHz;

3.1 7-stage divider A, presettable from 0 to 127 division. After completion of the process, this divider is stopped. It is reset and triggered by divider B. Consequently, it generates the switching signal for a predivider which causes a nonius kind of division; thereby enabling the comparator frequency to be adjusted to a higher value. The switching signal (output ENA) must, therefore, be synchronized with the input clock (delay < 300 ns). The switching signal ENA, for this reason, has the same frequency as the output fo divider B, while the divider ratio is determined by the division at A (ENA = L) and by the difference between the division at B and the division at A (ENA = H). If the division at A = 0, ENA is always H.

3.2 9-stage divider B, presettable from 2 to 513 division. At the end of the process, this divider resets itself and divider A. It supplies the divided carrier frequency for the phase comparator.

4. The phase comparator (see figure) performs the frequency comparison. It possesses 3 possible output combinations (see truth table 1) between which it switches, initiated by 0 → 1 transitions at the inputs (see truth table 2).

   In case of different input frequencies, the leading signal switches the output at its side (AD out+, SD out−) to "1"; it remains at this level until the other signal switches it back to "zero".

   If both frequencies are equal in behavior but different in phase, an output pulse with the width of the phase difference is generated at the leading side with each clock pulse. Should both 0 → 1 transitions at the input lie within the dead time, the phase comparator will remain in the "0" state.

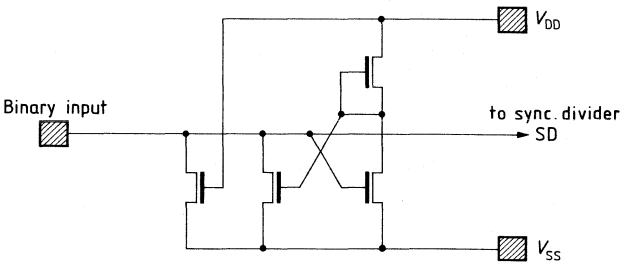
The phase comparator drives a complementary tristate gate, whereby the internal p-channel transistor is driven by the positive output and the external n-channel transistor by the inverted negative output. Consequently, the integration capacitor is charged during an H level, discharged during an L level. During 0 level its output is connected to a high resistance. Therefore, the capacitor voltage – and with it the frequency of the VCO – varies until the $0 \longrightarrow 1$ transitions are within one dead time of the phase comparator at both inputs.

5. Active p-function of the programming inputs. The assignment of individual frequencies to particular speech channels can be done externally by using a 10 x 16 diode matrix. It connects the selected programming inputs low-resistively to a negative potential (L), and loads the non-selected ones only with leakage currents (H).

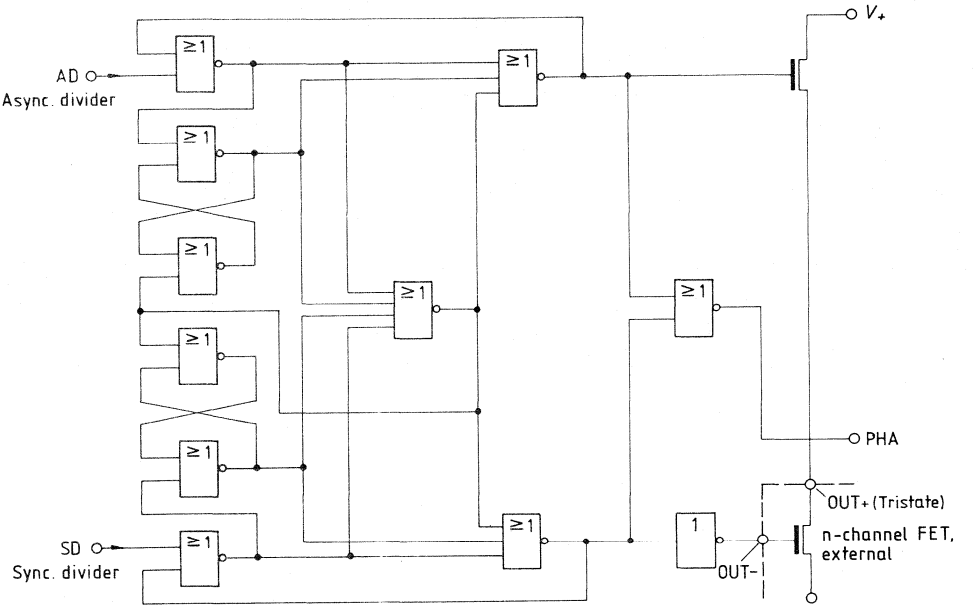
   The equivalent worst case values are: 5 kΩ to V_{DD} (L) or 100 kΩ to V_{DD} (H).

   The programming inputs have, therefore, been provided with an active p-circuitry (see figure) creating an input voltage of $> V_{SS}-1$ V in the H condition and input voltage of $< V_{DD}+1$ V in the L condition. In this way, various kinds of driving the inputs are made possible.

Active p-connection of the programming inputs



Phase comparator



Truth table 1 Phase comparator

State of phase comparator	Output +	Output −	Notes
H	1	0	internal p-channel MOS FET, on-state
L	0	1	external n-channel MOS FET, on-state
0	0	0	both transistors are off-state

Truth table 2 Phase comparator

Output state of phase comparator	New state after 0→1 transition at input	
	AD Async. divider	SD Sync. divider
H	H	0
0	H	L
L	0	L

Truth table 3 Reference frequency divider

Inputs MA1	MA2	8/10	Divider ratio
L	L	L	2048
H	L	L	1024
L	H	L	512
H	H	L	256
L	L	H	2560
H	L	H	1280
L	H	H	640
H	H	H	320

Truth table 4 VCO frequency divider

Divider A Inputs A1	A2	A4	A8	A16	A32	A64	Divider ratio[1])
L	L	L	L	L	L	L	0
H	L	L	L	L	L	L	1
L	H	L	L	L	L	L	2
.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.
H	H	H	H	H	H	L	126
H	H	H	H	H	H	H	127

Divider B Inputs B1	B2	B4	B8	B16	B32	B64	B128	B265	Divider ratio
L	L	L	L	L	L	L	L	L	512[2])
H	L	L	L	L	L	L	L	L	513
L	H	L	L	L	L	L	L	L	2
H	H	L	L	L	L	L	L	L	3
.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.
H	H	H	H	H	H	H	H	L	510
H	H	H	H	H	H	H	H	H	511

1) Output ENA remains in the L state for the programmed number of CLK 2 input pulses, then goes H.

2) If the contents of counter B equals zero, the preselected binary information at the A and B inputs is accepted into counters A and B with the next CLK 2 input pulse. The counters then count down from these values. If divider A reaches zero, it will stop until it is reloaded. ENA = L as long as divider A is running.

MOS IC

Type	Ordering code	Package	Fig. No.
S 353	Q67000-R109	DIP 28	16

This S 353 contains 160 diodes arranged in a 10 x 16 matrix. For programming, an NiCr fuse is connected in series with the diode.

The matrix is primarily suitable:

1. to replace the extensive wiring in preselection switches. Instead of the multipole wired switch, a single-pole model can be used. Switch and matrix are connected in series.
2. to be used as encoder, decoder, and recoder. The matrix is connected before or behind the appropriate components, or connected between them. The electrical level is only changed by the value of one diode voltage. The electrical connection remains.
3. The component requires MOS handling to avoid undesired programming.
   One of the most important applications is e.g., to enable the programming of frequencies or line numbers, respectively, in conjunction with the PLL component S 187 and the video pulse generator S 178 A.

Maximum ratings of the individual diodes including fuse

		Lower limit B	Upper limit A	
Reverse voltage	V_R	20		V
Forward current	I_F		2	mA
Programming current	I_{prog}		70	mA
Junction temperature	T_j		125	°C
Storage temperature	T_{stg}	−40	125	°C
Ambient temperature during operation	T_{amb}	−25	70	°C

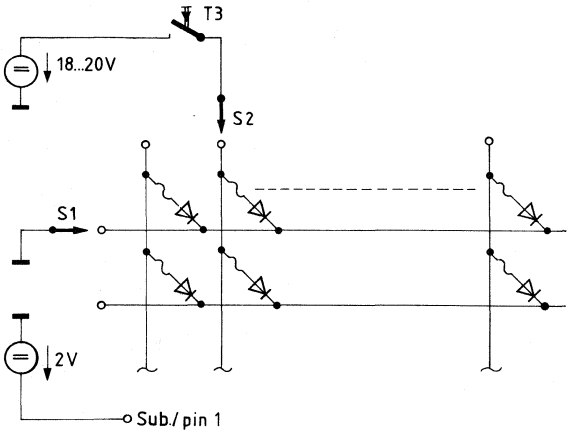
Characteristics of the individual diodes including fuse
$T_{amb} = 25\ °C$

		Test conditions	Lower limit B	typ	Upper limit A	
Reverse voltage	V_R	$I_R = 100\ \mu A$	20			V
Forward voltage	V_F	$I_F = 1\ mA$		1	1.5	V
Reverse current	I_R	$V_R = 10\ V$		10	100	nA
Reverse current output[1]	I_{RQ}	$V_I = 10\ V$ $V_Q = 9.5\ V$			10	µA
Programming current	I_{prog}	$V_Q = 20\ V$ $V_I = 0\ V$ $0_S = -2\ V$		50	70	mA
Resistance of the programmable fuse	R		1	2		MΩ
Capacitance I – Q	C	$V_R = 10\ V$		6	8	pF
Recovery time						

Programming conditions and simple programming circuit

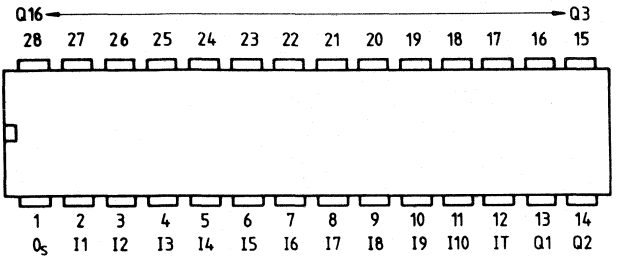
Using the circuit shown, the matrix can be programmed in the following manner:

1. observe MOS handling
2. connect pin 1 (substrate) to ground via a 2 V voltage source
3. connect desired input (I 1 to I 10) to ground using switch S 1
4. select desired output (Q 1 to Q 16) with switch S 2
5. trigger programming process with button T 3
6. the specified voltage source with 18 V to 20 V must be suited for a load of at least 300 Ω (fuse resistance), and must have a rise time from 0 V to 20 V of a least 1 µs
7. only one fuse may be programmed at a time
8. a current pulse duration of 5 ms to 10 ms is sufficient for programming.

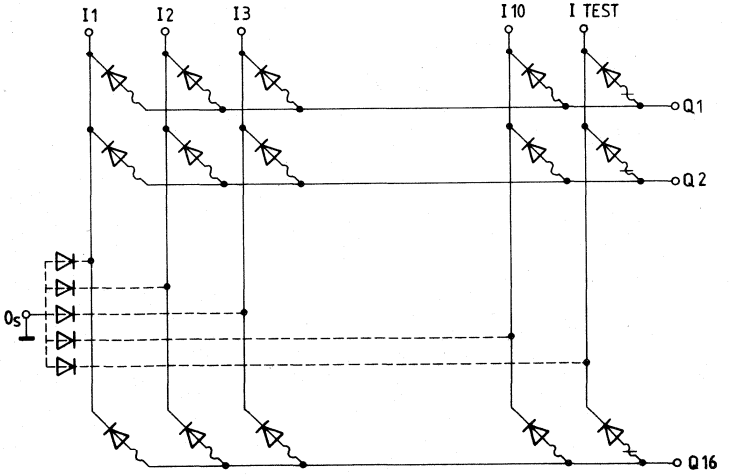


1) Reverse current at the output when all diodes are present and all inputs are interconnected.

Pin configuration
top view



Circuit



Note: Inputs must not be open $V_I < V_Q$

DC Motor Drivers

Bipolar IC

Type	Ordering code	Package	Fig. No.
TCA 955	Q67000-A983	DIP 16	5
TCA 955 K	Q67000-A983 K	MICROPACK 16 pins	30

The TCA 955 is suited for the speed control of dc motors. The principle corresponds to a clocked control. Outstanding features are its high control accuracy, its large supply voltage range, and the possible current saving. Additionally, the IC features a battery voltage indicator.

Typical applications

Speed control in

- tape recorders
- cassette recorders
- record players
- movie cameras
- control system drivers

Maximum ratings

Supply voltage	V_S	16	V
Supply voltage (pin 11 and pin 15 connected)	V_S	6	V
Output current pin 16	I_Q	200	mA
Output current pin 12 (LED output)	$I_{Q\,LED}$	15	mA
Power dissipation, LED output	$P_{Q\,LED}$	150	mW
Junction temperature	T_j	125	°C
Storage temperature range	T_{stg}	−55 to 125	°C
Thermal resistance (system-air)	$R_{th\,SA}$	85	K/W

Operating range

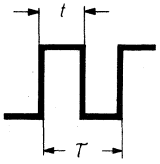
With internal short-circuit stabilization (pin 11 and pin 15 connected)	V_S	2 to 6	V
With internal stabilization (V_S to pin 15)	V_S	4.8 to 16.0	V
Ambient temperature range	T_{amb}	−25 to 85	°C

Characteristics

$T_{amb} = 25\,°C$; $V_S = 2.2$ V to 16.0 V

		min	typ	max	
Controller					
Current consumption $V_S = 4.8$ V	I_S		8.3	12.0	mA
$V_S = 16$ V	I_S		15.5	24.0	mA
Stabilized voltage	V_{stab}	2.75	3.00	3.30	V
$V_S = 4.8$ V to 16 V					
Input threshold (pin 3)					
to ground	V_I	0.46 x V_{11}	0.485 x V_{11}	0.51 x V_{11}	V
Hysteresis of input threshold	ΔV_I		0.015 x V_{11}	0.03 x V_{11}	V
Offset voltage (pin 3 to pin 2)	V_{offset}		11	20	mV
Input current (pin 3)	I_I			1	µA
Output transistor saturation voltage					
$I_Q = 50$ mA	$V_{Q\,sat}$		0.84	1.00	V
$I_Q = 100$ mA	$V_{Q\,sat}$		0.92	1.25	V
Output transistor cutoff current	$I_{Q\,H}$			30	µA
Duty cycle – control range[1]	ν	0		1	
Rated rpm[2]	n	$\frac{12{,}55}{p \cdot R_1 \cdot C_2}$	$\frac{14{,}85}{p \cdot R_1 \cdot C_2}$	$\frac{17{,}64}{p \cdot R_1 \cdot C_2}$	rpm
Error in rpm with duty cycle contrl[3] from 0 to 1				$\frac{0{,}224}{N \cdot p \cdot C_3}$	%
Switching oscillator					
Frequency	f		$\frac{1}{0{,}4 \cdot R_2 \cdot C_4}$		Hz
Average voltage pin 10	$V_{Q\,OSC}$		0.48 x V_{11}		V
Voltage pin 11 peak to peak	$V_{Q\,OSC}$		0.18 x V_{11}		V

1) Duty cycle



$\nu = \frac{t}{T}$

2) p = number of pole pairs of the tachometer generator.

3) in applications without switching oscillator.

Battery voltage indicator		min	typ	max	
Threshold voltage	$V_{I\,on}$			1.5	V
	$V_{I\,off}$	1.0			V
Hysteresis	V_{hy}		220		mV
Input current	I_I			0.2	µA
Saturation voltage LED output[1]	$V_{Q\,LED}$			$0.5 + 500 \times I_{LED}$	V

Formulae:

Rate rpm $n = \dfrac{14{,}85}{p \cdot R_1 \cdot C_2}$ [rpm]

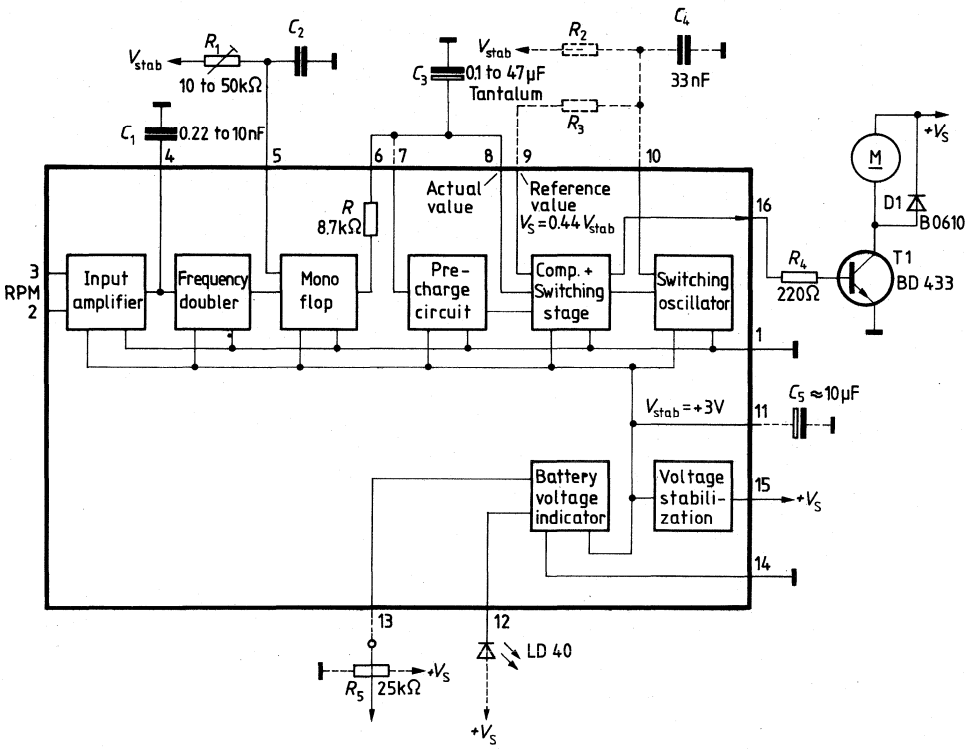
Switching frequency $f = \dfrac{n \cdot p}{30}$ [Hz]

in operation without switching oscillator.

Reference value $V_{ref} = 0.44 \times V_{11}$ [V]
Precharging voltage at C_3 (pin 6 and pin 7 connected) $V_F = 0.87 \times V_{ref}$ [V]

1) A protective resistor of 500 Ω ± 20% is integrated inside the IC.

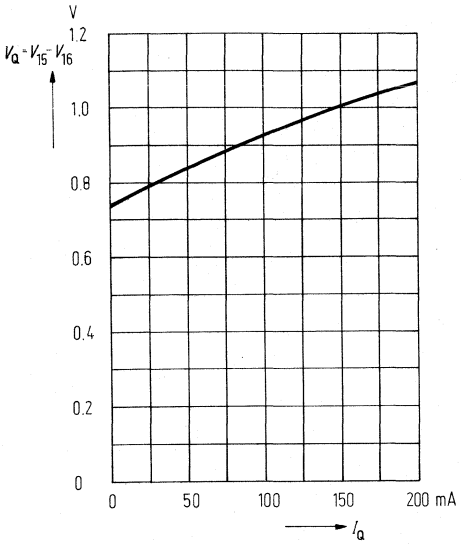
Block diagram for speed control with TCA 955



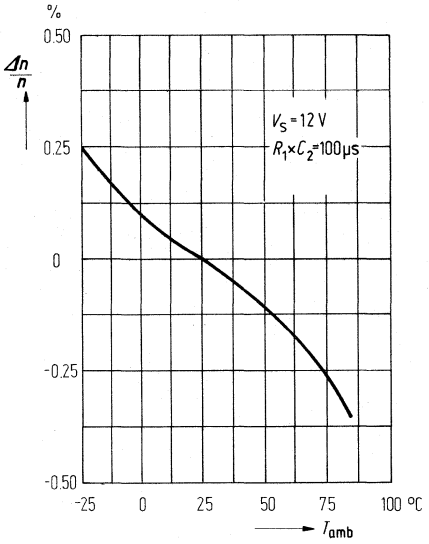
Dimensioning notes

1. The internal voltage stabilization offers the following advantages:
   — operation with highly varying supply voltage,
   — wide range of supply voltage.
2. In order to receive pulses with a steady duty cycle at the output, symmetrical pulses must be applied to the input.
3. It is recommended to use multipole tachometer generators as this improves the accuracy of control and possibly the power consumption.
4. The power consumption can considerably be reduced by means of the switching frequency oscillator at low electric motor time constants.
5. Higher accuracy can be obtained by using a second-order filter instead of C_3.
6. When using rapidly starting motors, the precharge circuitry reduces overshoots.

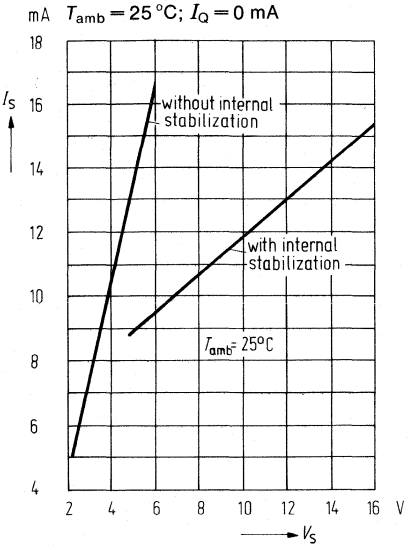
Saturation voltage of output transistor
Output voltage versus output current



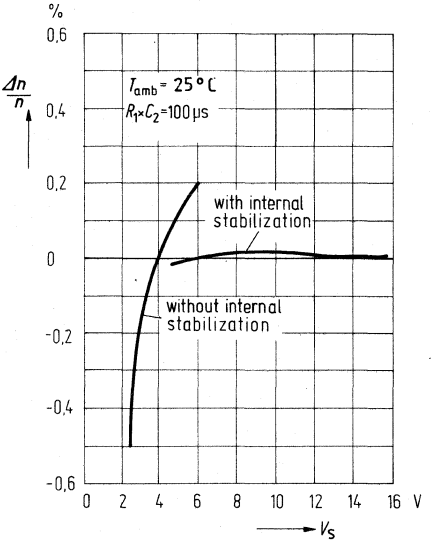
Rpm versus ambient temperature
$V_S = 12$ V; $R_1 \times C_2 = 100$ µs



Current consumption
versus supply voltage
$T_{amb} = 25$ °C; $I_Q = 0$ mA



Rpm versus supply voltage
$T_{amb} = 25$ °C; $R_1 \times C_2 = 100$ µs



Bipolar IC

Type	Ordering code	Package	Fig. No.
TLE 4201 A	Q67000-A2113	DIP 18-L 9	11
TLE 4201 S	Q67000-A2114	SIP 9	21

The TLE 4201 IC is a dual comparator that is particularly suitable as a driver for reversible dc motors and may also be used as a versatile power driver.

The push-pull power-output stages work in a switch mode and can be combined into a full bridge configuration.

The driving of the comparators may be analog in the form of a window discriminator, or it can be accomplished very simply with digital logic.

Typical applications are follow-up controls, servo drives, servo motors, drive mechanisms, etc.

Features

- Max. output current 2.5 A
- Open-loop gain 80 dB typ.
- PNP input stages
- Large common-mode input-voltage range
- Wide control range
- Low saturation voltages
- SOA protective circuit
- Temperature protection

The TLE 4201 IC comes in two different packages: with the SIP 9 package it is possible to remove the heat by way of a cooling fin to a suitable heatsink, whereas with the DIP 18-L9 package the pins 10 through 18 are thermally linked to the chip and provide for heat dissipation by way of the circuit board.

Block diagram

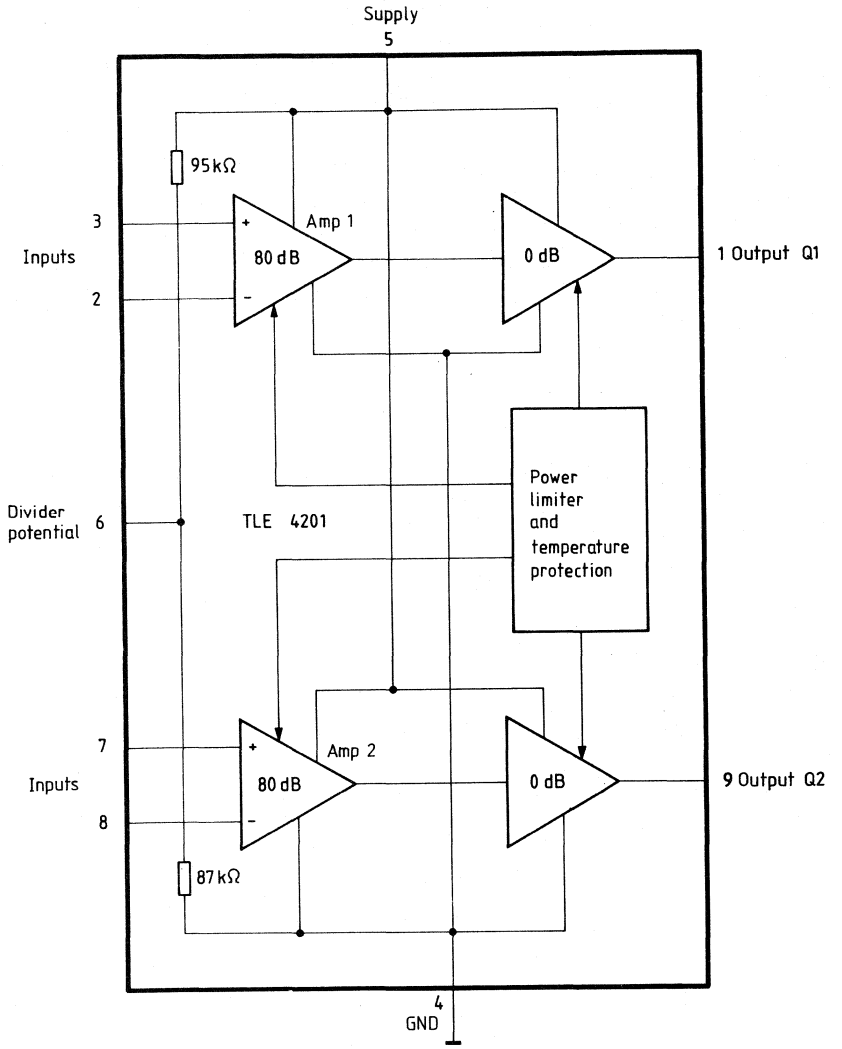


Figure 1

Pin configuration

TLE 4201 A Pin No.	TLE 4201 S Pin No.	Function
1	1	Output of 1st amplifier
2	2	Inverting input of 1st amplifier
3	3	Non-inverting input of 1st amplifier
4	4	Ground
5	5	Supply voltage
6	6	Divider potential
7	7	Non-inverting input of 2nd amplifier
8	8	Inverting input of 2nd amplifier
9	9	Output of 2nd amplifier
10 to 18	—	Ground; to be connected to pin 4

Circuit description

The IC contains two amplifiers featuring a typical open-loop voltage gain of 80 dB at 500 Hz. The input stages are PNP differential amplifiers. This results in a common-mode input voltage range from 0 V to almost the value of V_S, and in a maximum input differential voltage of I V_S I. To obtain low saturation voltages, the sink transistor (lower transistor) of the push-pull AB output stage is internally bootstrapped. An SON protective circuit protects the IC against motor short circuits and ground short circuits. An internal overtemperature protection protects the IC against overheating in case of failure due to insufficient cooling or overload.

For logic control, a divider potential of approx. $V_S/2$ is available at pin 6 (see application circuit 2). This makes the IC particularly suitable for digital circuits, as power driver.

Application

Figure 2 shows a window discriminator operation with the control voltage V_I.
The window within which the motor is to stop is set by R_2.

Figure 3 shows driving by logic inputs A and B. The motor is controlled according to the following truth table.

A	B	Output
L	L	Motor stopped (slowed down)
L	H	Motor turns right
H	L	Motor turns left
H	H	Motor stopped (slowed down)

Application circuits

Operated as window discriminator

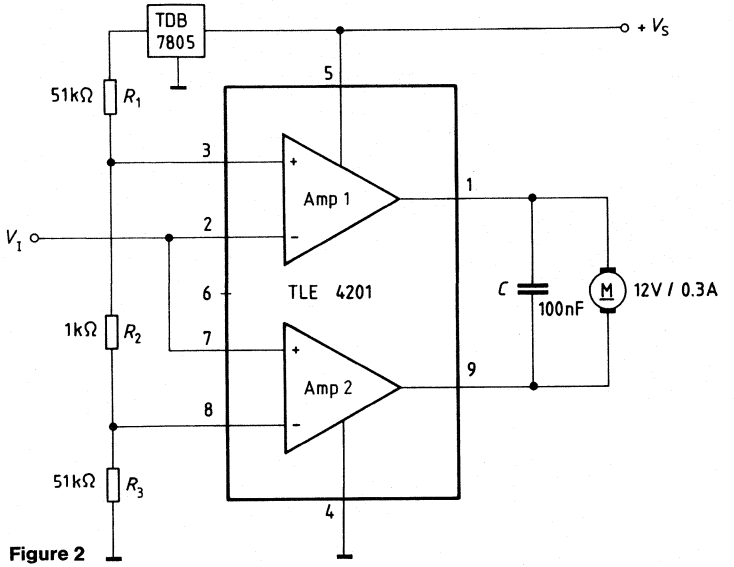


Figure 2

Digital control

for input signals applies: H ≥ 0.6 V_S
L ≤ 0.3 V_S

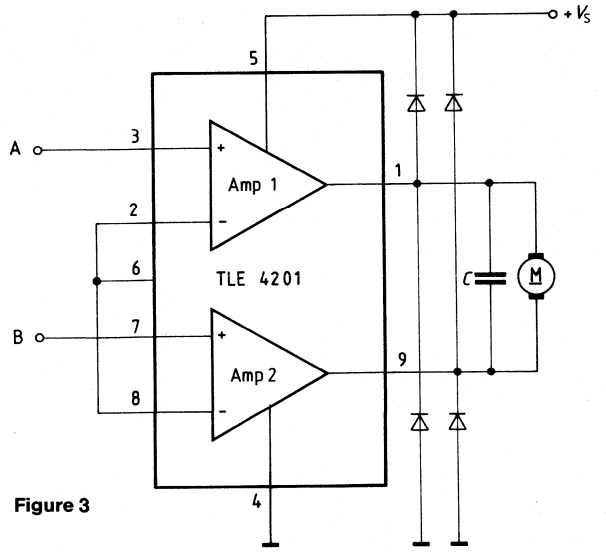


Figure 3

Maximum ratings

$T_{case} = -35$ °C to 85 °C

		Lower limit B	Upper limit A	
Supply voltage	V_S		25	V
Supply voltage ($t \leq 50$ ms)	V_S		36	V
Output current	I_Q		2.5	A
Voltage of pins 2, 3, 6, 7, 8	V	−0.3	V_S	V
Voltage of pins 1, 9	V	−0.3		V
Junction temperature	T_j		150	°C
Storage temperature	T_{stg}	−55	125	°C
Thermal resistance				
TLE 4201 S: system-air	$R_{th\,JA}$		65	K/W
system-case	$R_{th\,JC}$		8	K/W
TLE 4201 A: system-air[1)]	$R_{th\,JA}$		60	K/W
system-PC board[1)]	$R_{th\,JA1}$		44[1)]	K/W

Operating range

Supply voltage	V_S	3.5	17	V
Case temperature	T_{case}	−35	85	°C
Voltage gain (at negative feedback with external components)	G_V	25		dB

Characteristics

$V_S = 13$ V, $T_{case} = 25$ °C

		Test conditions		Lower limit B	typ	Upper limit A	
Supply current	I_S	Figure 4: S = 1			20	30	mA
Open-loop voltage gain	G_{V0}	$f = 500$ Hz			80		dB
Input resistance	R_I	$f = 1$ kHz		1	5		MΩ
Saturation voltages,		Figure 5:	S1				
source operation	$V_{Q\,10}$	$I_Q = 0.3$ A	1		1.0	1.1	V
		$I_Q = 1.0$ A	1		1.2	1.6	V
sink operation	$V_{Q\,20}$	$I_Q = -0.3$ A	2		0.35	0.5	V
		$I_Q = -1.0$ A	2		0.7	1.0	V
Rise time of V_Q	t_r	Figure 4 and 6			1.5		µs
Fall time of V_Q	t_f	Figure 4 and 6			1.5		µs
Turn-on delay time	t_{on}	Figure 4 and 6			3.0		µs
Turn-off delay time	t_{off}	Figure 4 and 6			1.5		µs
Input current (pins 2, 3, 7, 8)	I_I	Figure 5 $V_{2,3,7,8} = 0$			1.5	3.0	µA
Input offset voltage	V_{IO}	Figure 7		−20		20	mV

1) see figure 8

Test circuits

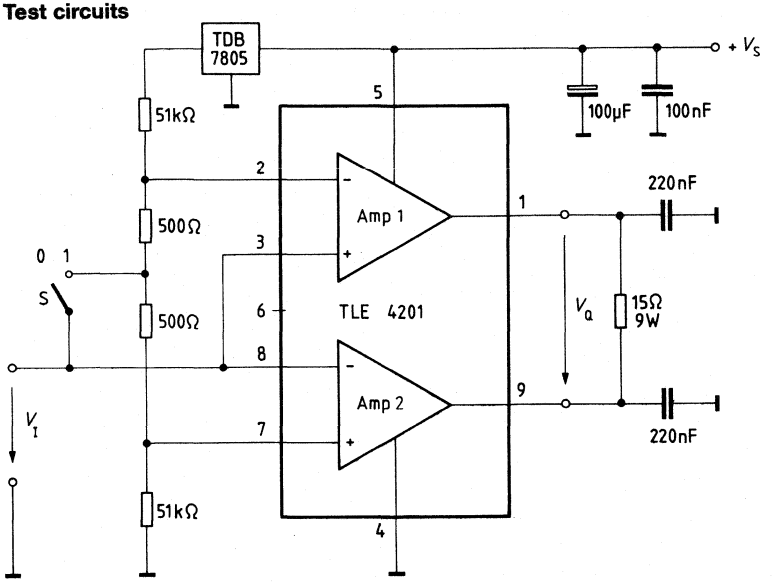


Figure 4

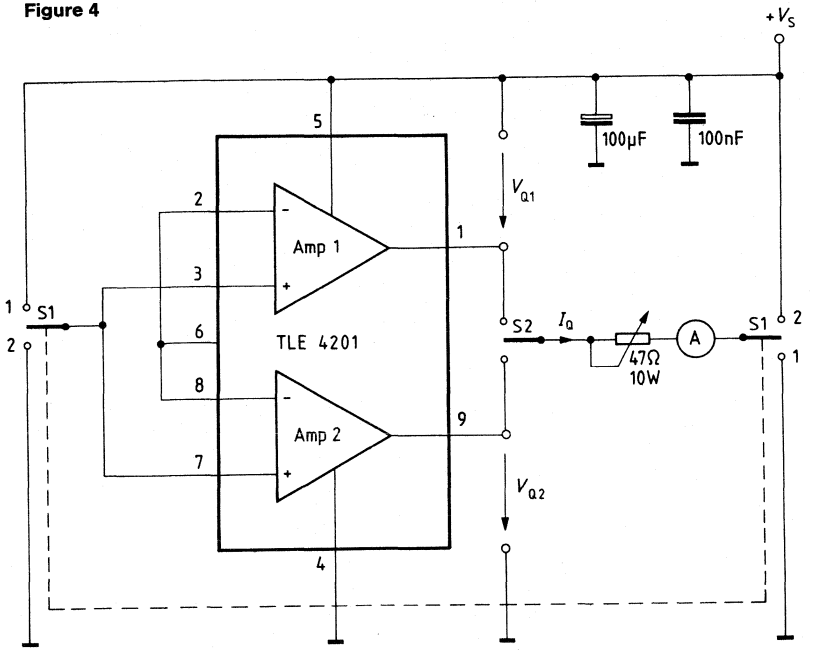


Figure 5

Pulse diagram

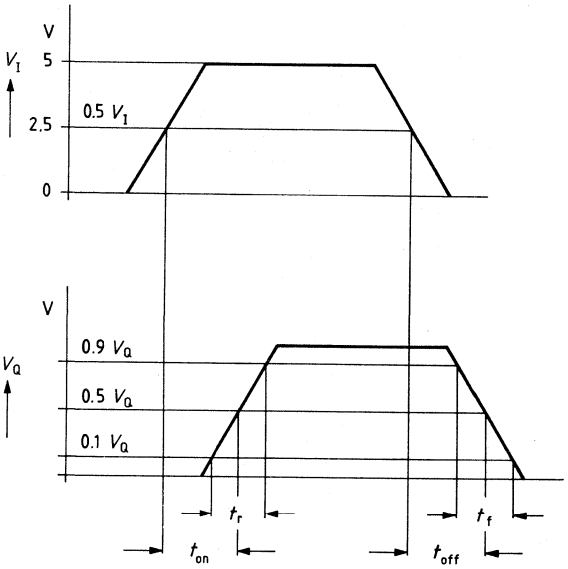


Figure 6

Test and measurement circuit

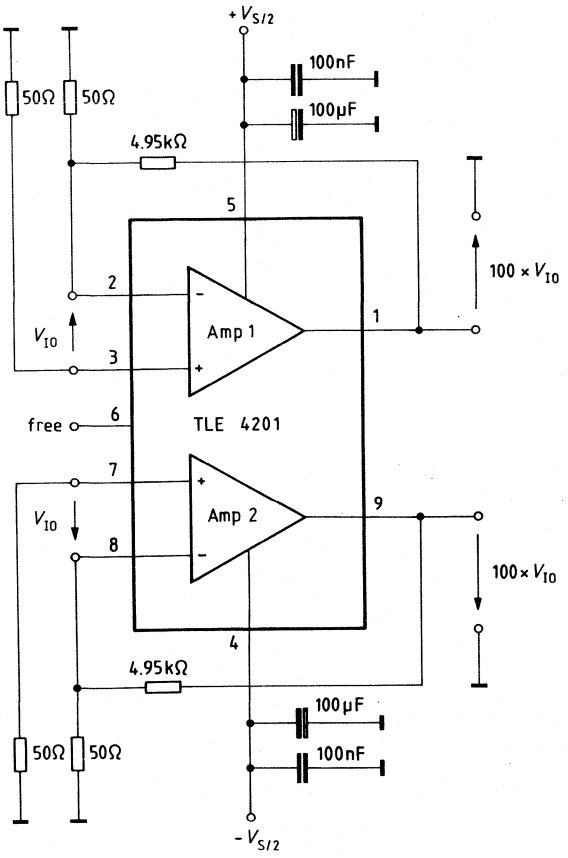


Figure 7

Thermal resistance of TLE 4201 A

Thermal resistance, junction-air, $R_{th\ JA\ 1}$ (standard) versus side length l of a square copper-clad cooling surface (35 µm copper plate)

$R_{th\ JA}$ $(l = 0) = 60$ K/W
$T_{amb} \leq 70$ °C
$P_V = 1$ W
substrate vertical
circuit vertical
static air

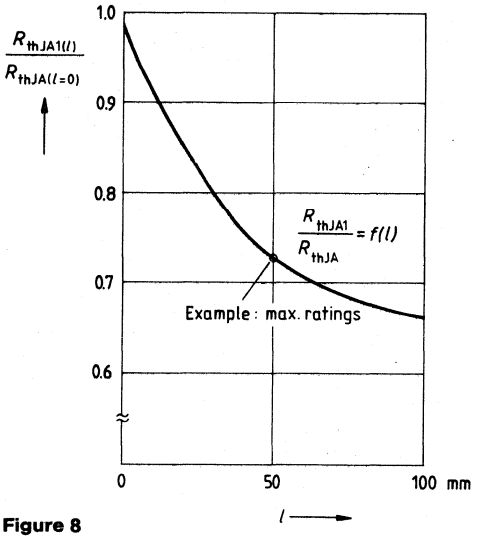


Figure 8

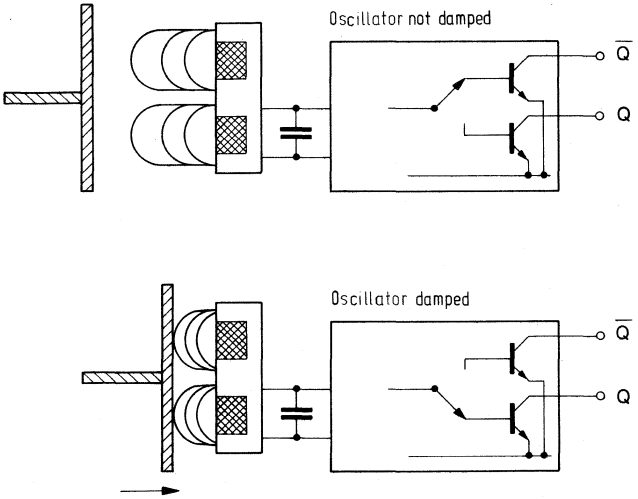
ICs for Sensors, Proximity Switches, Hall-Effect Devices, Light Sensors

Type	Ordering code	Package	Fig. No.
■ TCA 205 A	Q67000-A1034	DIP 14	7
■ TCA 205 K	Q67000-A1034-K	MICROPACK, 14 connections	29

For new design, the ICs TCA 305/TCA 355 are recommended.

This IC is intended for applications in inductive proximity switches. The outputs switch when the oscillation is damped, e.g. by the approach of a metal object.

Operation schematic



Features

- Large supply voltage range
- High output current
- Antivalent outputs
- Adjustable switching distance
- Adjustable hysteresis
- Turn-on delay

■ Not for new design

Maximum ratings

Supply voltage	V_S	30	V
Output voltage	V_Q	30	V
Output current	I_Q	50	mA
Junction temperature	T_j	125	°C
Storage temperature range	T_{stg}	−55 to 125	°C
Thermal resistance (system-air) TCA 205 A	$R_{th\,SA}$	85	K/W

Operating range

Supply voltage range	V_S	4.75 to 30	V
Ambient temperature range	T_{amb}	−25 to 85	°C

Characteristics

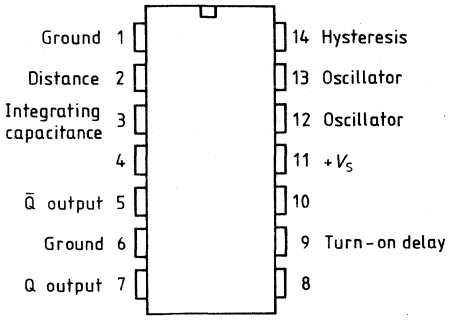
$V_S = 12$ V; $T_{amb} = 25$ °C

		Test conditions	Lower limit B	typ	Upper limit A	
Open-loop supply current consumption	I_S	open pins		1	2	mA
L output voltage per output	V_{QL}	$I_{QL} = 5$ mA		0.8	1	V
	V_{QL}	$I_{QL} = 50$ mA		1.25	1.5	V
H output current per output	I_{QH}	$V_{QH} = 30$ V			10	µA
Integrating capacitance	C_I			10		nF
Internal resistance at 3	R_{i3}		200	350	660	kΩ
Threshold voltage at 3	V_{S3}			1.3	1.5	VΩ
Distance adjustment (circuit 1)	R_{di}		6			kΩ
Hysteresis adjustment (circuit 1)	R_{hy}		0			kΩ
Distance adjustment (circuit 2)	R_{di}	$R_{hy} \rightarrow \infty$	6[1]			kΩ
Hysteresis adjustment (circuit 2)	R_{hy}	$R_{di} \rightarrow \infty$	6[1]			kΩ
Turn-on delay	t_{don}			200		ms/µF
Oscillating frequency	f_{OSC}		0.015		1.5	MHz
Switching frequency without C_I	f_s				5	kHz

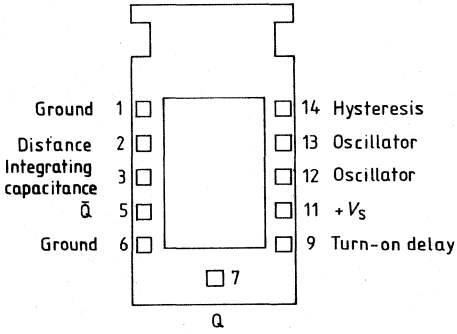
1) Parallel connection of R_{hy} to R_{di} may at least amount to 6 kΩ

Pin configurations

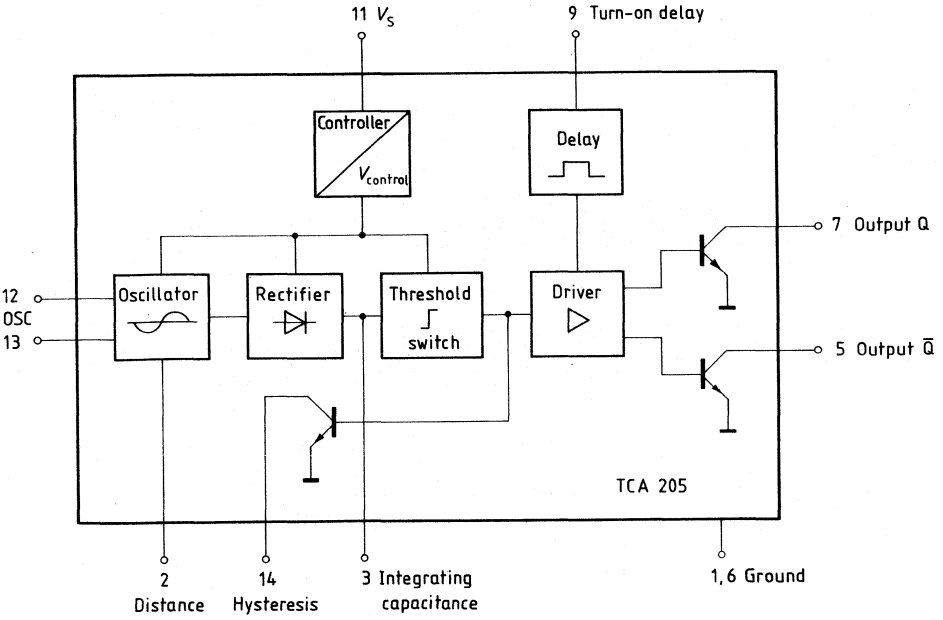
TCA 205 A



TCA 205 K

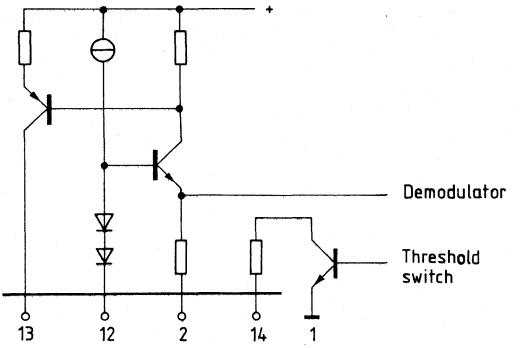


Block diagram

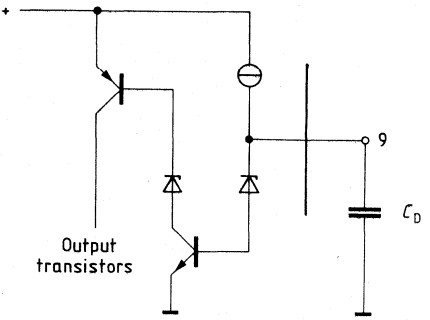


Schematic circuit diagrams

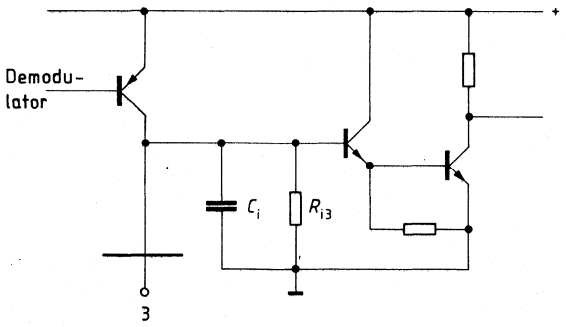
Oscillator



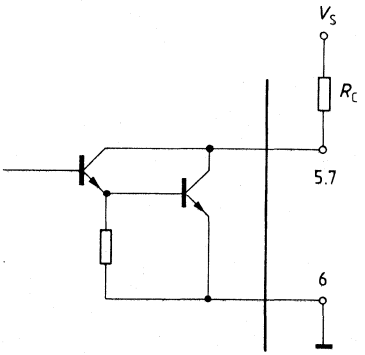
Turn-on delay



Integrating capacitor

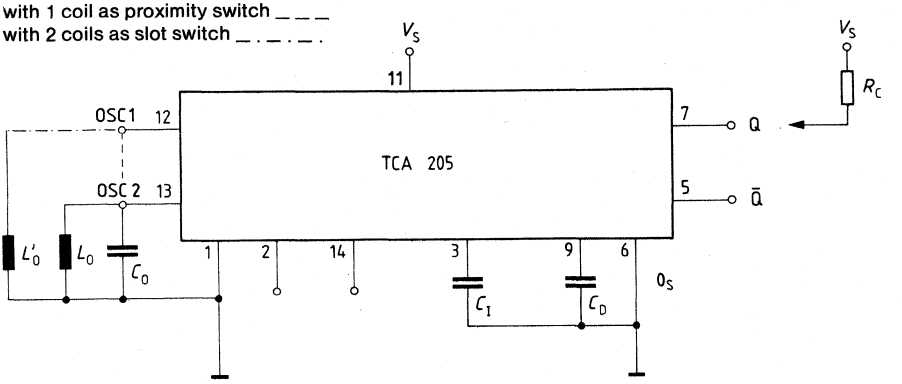


Outputs



Application circuit

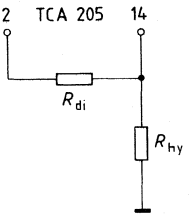
with 1 coil as proximity switch _ _ _
with 2 coils as slot switch _ . _ . _ .



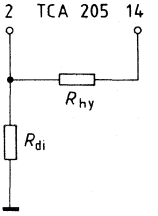
L_0, C_0	oscillator
R_{di}	distance adjustment
R_{hy}	hysteresis adjustment
C_I	integrating capacitor
C_D	delay capacitor

The resistance of distance and hysteresis R_{di} and R_{hy}, for proximity switch TCA 205 A; K may be applied as follows:

1. Series hysteresis



2. Parallel hysteresis

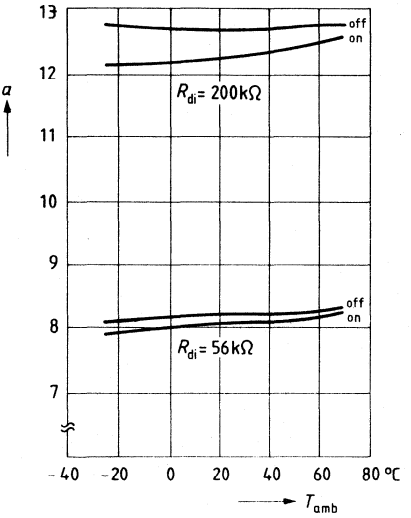


Circuit 1 is more suitable for proximity switches with oscillator frequencies of $f > 200$ kHz to 300 kHz, and small distance. Circuit 2 is more favorable for AF proximity switches having larger distance. This is due to the lower R_{hy} values enabled by circuit 1 (min. 0 Ω) compared with circuit 2 (min. 6 kΩ). Starting at frequencies of 200 kHz, high R_{hy} values effect in addition to the hysteresis also the oscillator phase. Practical applications, however, require little phase response to receive a clear evaluation.

Application example for a proximity switch

Coil data	pot core B65939-A-X22 coil former B65940-A-M1 Ø = 25 mm x 8.9 mm L = 642 µH n = 100 CuLS 30 x 0.05	
Measuring plate	30 mm x 30 mm x 1 mm, Fe	
Circuitry	R_{di} = 56 to 200 kΩ, metal layer R_{hy} = ∞ C_0 = 1500 pF, STYROFLEX f = 162 kHz	circuit 2

Switching distance versus ambient temperature

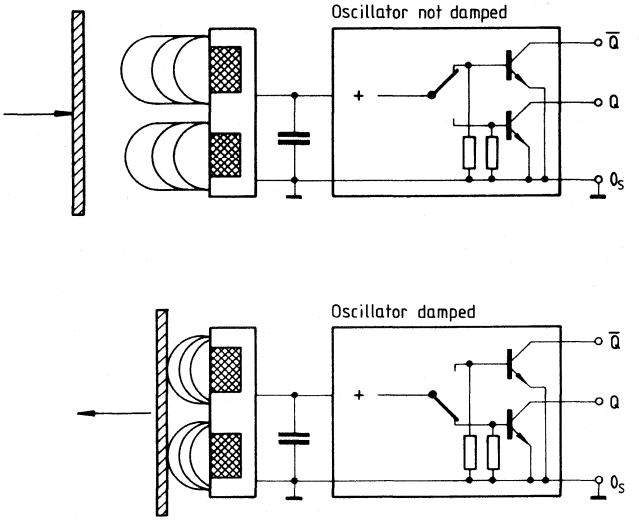


Preliminary data

Type	Ordering code	Package	Fig. No.
TCA 305 A	Q67000-A2291	DIP 14	7
TCA 305 G	Q67000-A2305	SO 14	27
TCA 355 B	Q67000-A2443	DIP 8	6
TCA 355 G	Q67000-A2444	similar to SO 8	26

The devices TCA 305 and TCA 355 contain all the functions necessary to design inductive proximity switches. Their operating principle is illustrated in the following figure. By approaching a standard metal plate to the coil, the resonant circuit is damped and the outputs are switched.

Operation schematic



Logic functions

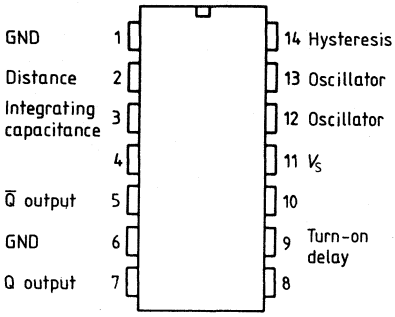
Oscillator	Outputs Q	Q
not damped	H	L
damped	L	H

Outstanding features

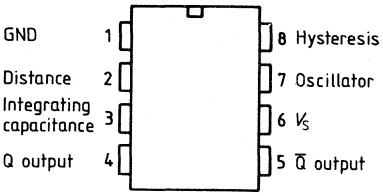
- Open-loop current consumption $I_S < 1$ mA
- Output saturation voltage $V_Q < 0.4$ V
- Adjustable turn-on delay at pin 9 of TCA 305
- Small distance resistors
- High switching frequency
- Integrating capacitor generally unnecessary
- Internal hysteresis with low temperature and supply voltage dependence
- Miniature packages

Pin configuration

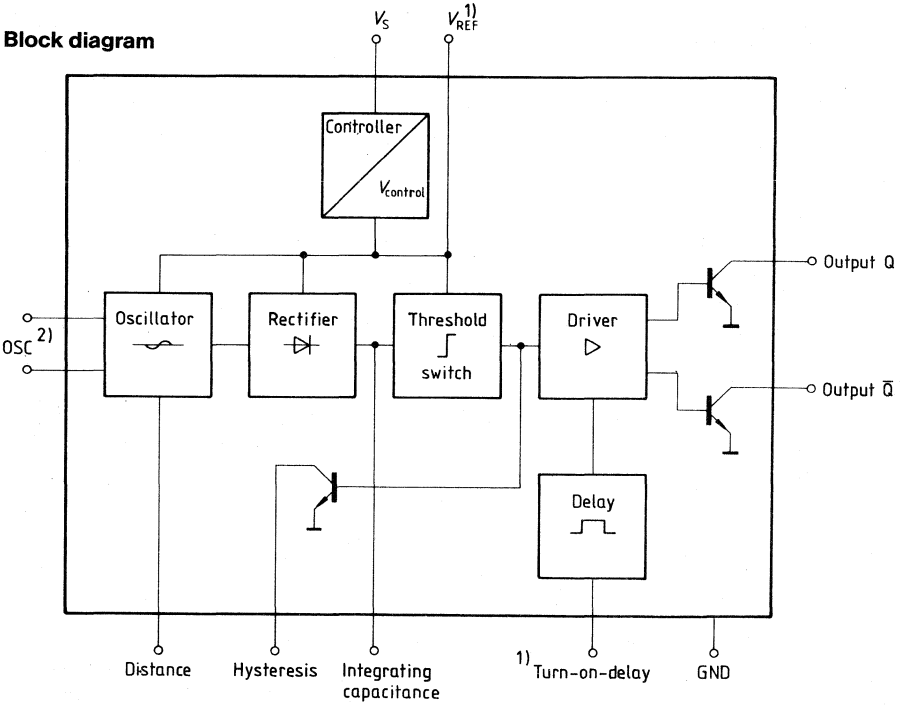
TCA 305 A, G



TCA 355 B, G



Block diagram



1) TCA 305 only
2) Connected internally in case of TCA 355

Maximum ratings

Supply voltage	V_S	30	V
Output voltage	V_Q	30	V
Output current	I_Q	25	mA
Distance, hysteresis resistance	R_{di}, R_{hy}	0	Ω
Capacitances	C_I, C_a	5	µF
Junction temperature	T_j	125	°C
Storage temperature range	T_{stg}	−55 to 125	°C
Thermal resistance (system-air)	$R_{th\,SA}$	85	K/W

Operating range

Supply voltage range	V_S	5 to 30	V
Oscillator frequency range	f_{OSC}	0.015 to 1.5	MHz
Ambient temperature range	T_{amb}	−25 to 85	°C

Characteristics

$V_S = 12$ V, $T_{amb} = -25$ °C to 85 °C

		Test conditions	Lower limit B	typ	Upper limit A	
Open-loop current consumption	I_S	outputs open		0.6	1.0	mA
Reference voltage	V_{ref}	$I_{ref} < 10$ µA		3.2		V
L output voltage	V_{QL}	$I_{QL} = 5$ mA		0.15	0.25	V
per output	V_{QL}	$I_{QL} = 25$ mA			0.4	V
H output current per output	I_{QH}	$V_{QH} = 30$ V			10	µA
Threshold at 3	V_{S3}			2.1		V
Hysteresis at 3	V_{hy}		0.4	0.5	0.6	V
Turn-on delay	$t_{d\,on}$	$T_{amb} = 25$ °C	−25%	600	−25%	ms/µF
Switching frequency w/o C_I	f_s				5	kHz

Maximum ratings

Supply voltage		V_S	30	V
Output voltage		V_Q	30	V
Output current		I_Q	25	mA
Distance, hysteresis resistance		R_A, R_4	0	Ω
Junction temperature		T_j	125	°C
Storage temperature range		T_{stg}	−55 to 125	°C
Thermal resistance (system-air)	TCA 355 B	$R_{th\,SA}$	135	K/W
	TCA 355 G	$R_{th\,SA}$	200	K/W

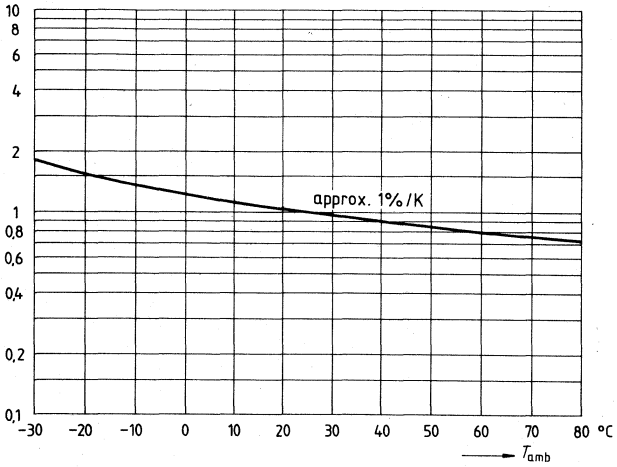
Operating range

Supply voltage range	V_S	5 to 30	V
Oscillator frequency range	f_{OSC}	0.015 to 1.5	MHz
Ambient temperature range	T_{amb}	−25 to 85	°C

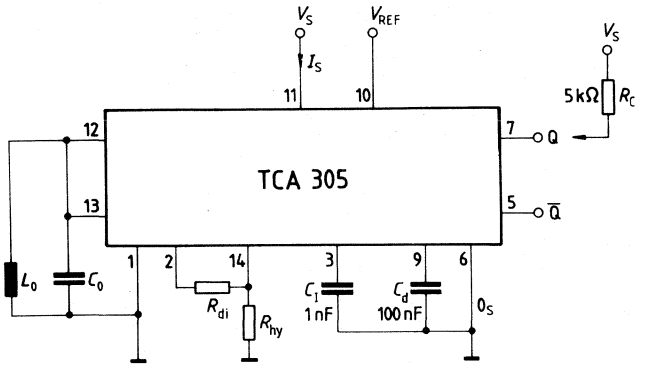
Characteristics
(V_S = 12 V; T_{amb} = −25 to 85 °C)

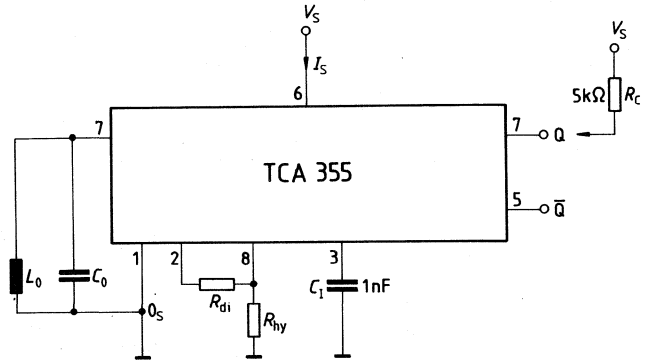
		Test conditions	Lower limit B	typ	Upper limit A	
Open-loop current consumption	I_S	outputs open		0.6	1.0	mA
L output voltage	V_{QL}	I_{QL} = 5 mA		0.15	0.25	V
per output	V_{QL}	I_{QL} = 25 mA			0.4	V
H reverse current	I_{QH}	V_{QH} = 30 V			10	µA
per output						
Threshold at 3	V_{S3}			2.1		V
Hysteresis at 3	V_{hy}		0.4	0.5	0.6	V
Switching frequency w/o C_I	f_s				5	kHz

Standard turn-on delay referred to T_{amb} = 25 °C



Test circuits





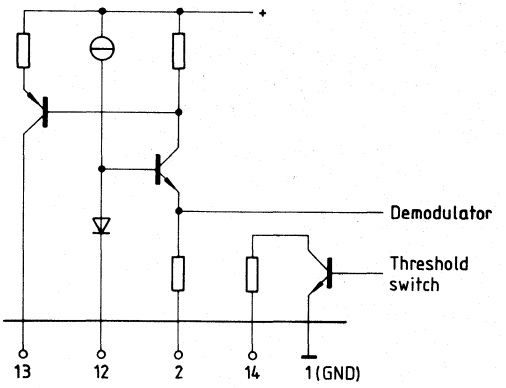
L_0, C_0	resonant circuit
R_{di}	distance adjustment
R_{hy}	hysteresis adjustment
C_I	integrating capacitor
C_d	delay capacitor (with TCA 305 only)

Dimensioning example

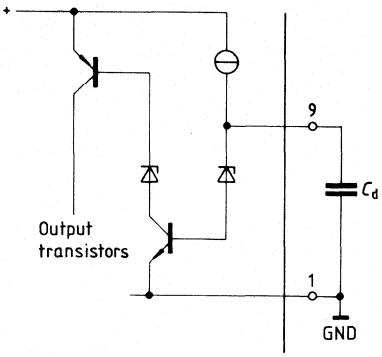
L_0 = 585 µH on SIFERRIT pot core N 22 (25 x 8.9 mm)
n = 100 CuL 10 x 0.1
C_0 = 3.3 nF, STYROFLEX
R_{di} = 25 kΩ, metal film
R_{hy} = 3.3 kΩ, metal film

Schematic circuit diagrams

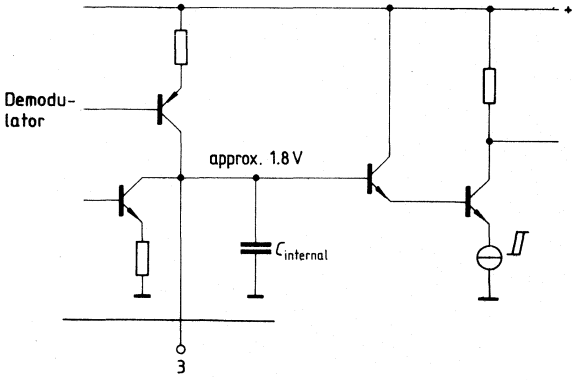
Oscillator



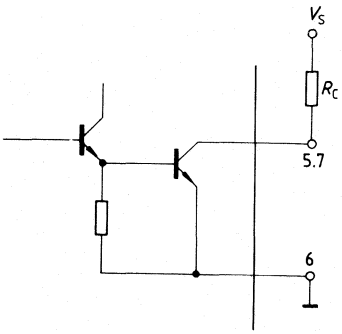
Turn-on delay for TCA 305



Integrating capacitor



Outputs



Bipolar IC

Type	Ordering code	Package	Fig. No.
TFA 1001 W	Q67000-A1357	Transparent miniature plastic package, 6 pins	3

The bipolar IC TFA 1001 W contains a photodiode and an amplifier. At its output (open NPN collector), the TFA 1001 W supplies a current directly proportional to the illuminance. Another pin permits a linearized characteristic curve at low illuminances and can be used to inhibit the output.

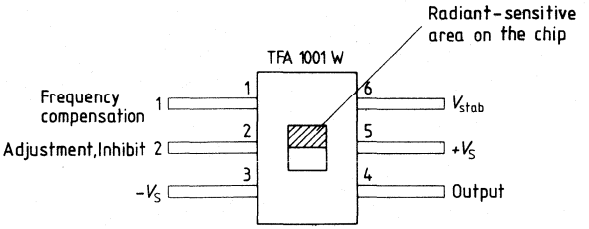
Application

- Exposure meters
- Exposure control systems
- Electronic flashes
- Optical follow-up control
- Smoke detectors
- Linear optocouplers
- Color identification

Features

- High sensitivity
- High output current linearity
- Good spectral sensitivity
- Low current consumption
- Wide modulation range
- Large operating voltage range

Pin configuration



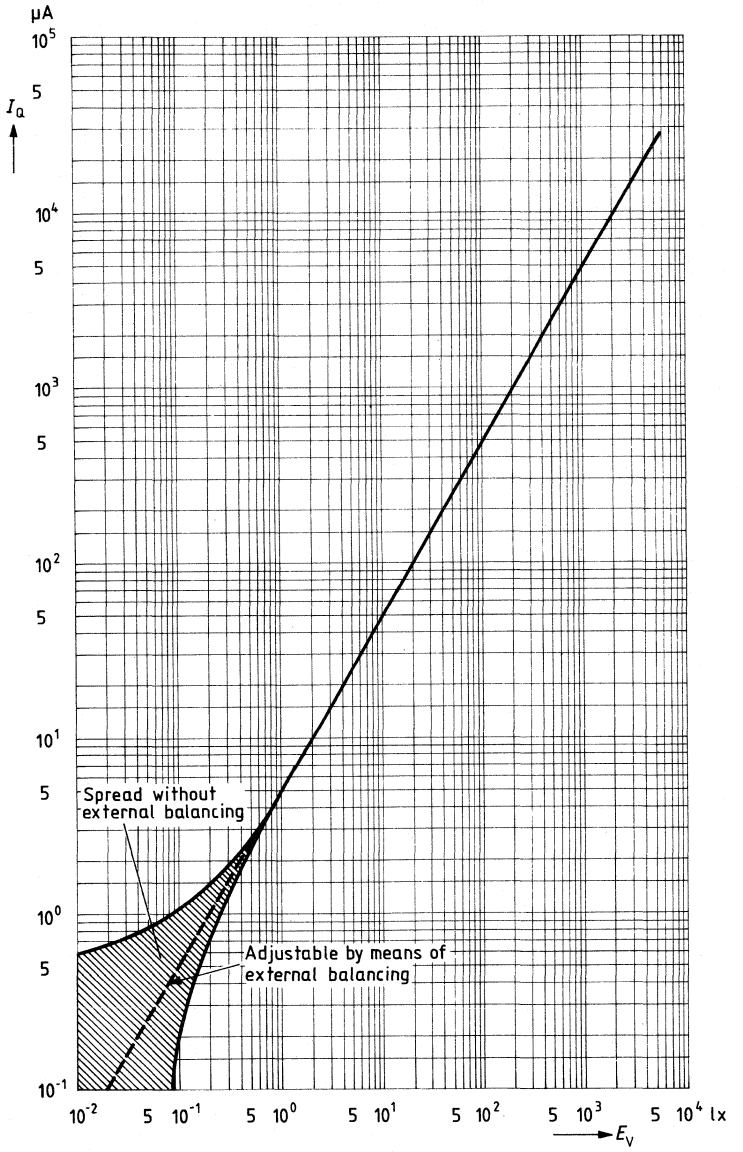
Maximum ratings

		Lower limit B	Upper limit A	
Supply voltage	V_S		15	V
Output current	I_Q		50	mA
Power dissipation	P_{tot}		200	mW
Junction temperature	T_j		100	°C
Storage temperature	T_{stg}	−40	85	°C
Thermal resistance (system-air)	$R_{th\,SA}$		250	K/W

Characteristics at $T_{amb} = 25$ °C, supply voltage applied to pin 5

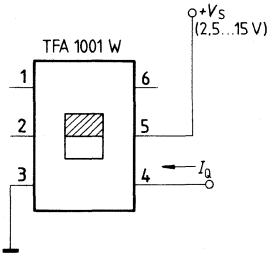
		Lower limit B	typ	Upper limit A	
Supply voltage	V_S	2.5		15	V
Current consumption at $E_v = 0$ lx	I_S	−10		1	mA
Ambient temperature (during operation)	T_{amb}			70	°C
Illuminance	E_v	0		5000	lx
Sensitivity in range					
$E_v = 1$ lx to 1000 lx	S	2.5	5	7.5	µA/lx
Output current at					
$E_v = 0.05$ lx	I_Q		0.25		µA
$E_v = 1$ lx	I_Q	2.5	5	7.5	µA
$E_v = 1000$ lx	I_Q	2.5	5	7.5	mA
$E_v = 5000$ lx	I_Q		25		mA
Stabilized voltage at pin 6	V_{stab}	1.2	1.35	1.5	V
Supply voltage dependence of stabilized voltage V_{stab}	$\Delta V_{stab}/\Delta V_S$		2		mV/V
Temperature dependence of stabilized voltage V_{stab}	$\Delta V_{stab}/\Delta T_{amb}$		−0.3		mV/°C

Photocurrent versus illuminance

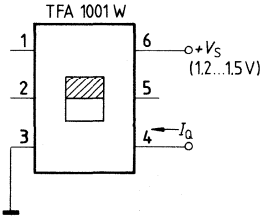


Possible applications of TFA 1001 W as light/current transducer

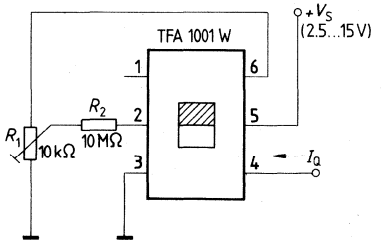
1) for operating voltage 2.5 to 15 V



2) for low operating voltage 1.2 to 1.5 V

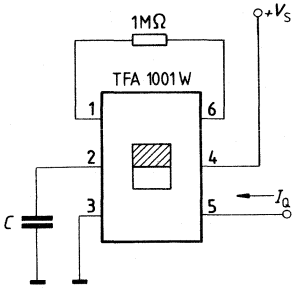


3) for especially low illuminance down to 0.01 lx

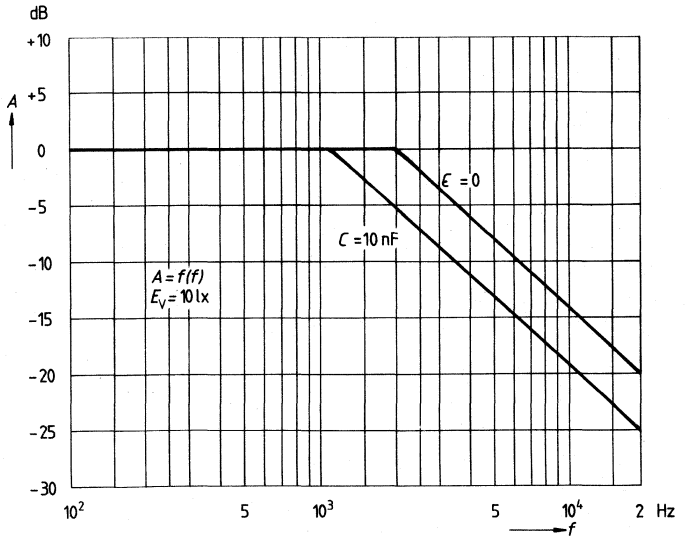


In case of low illuminance (see characteristic: output current versus illuminance), the output current can be balanced by means of the adjustment control R_1. The lower range of the output characteristic can be linearized even more by setting a dark current of about 5 nA.

Dynamic behavior

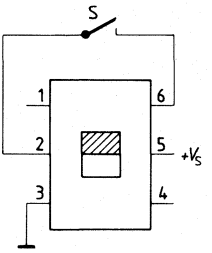


The dynamic behavior can be influenced at connection 2 by connecting capacitors.



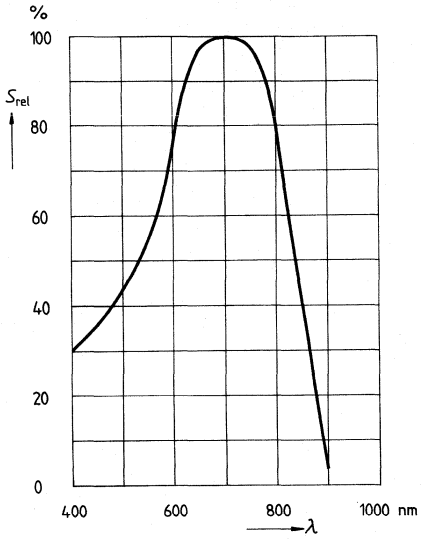
Attenuation $A = \frac{I_Q(f)}{I_Q(f=0)}$

Inhibiting the output

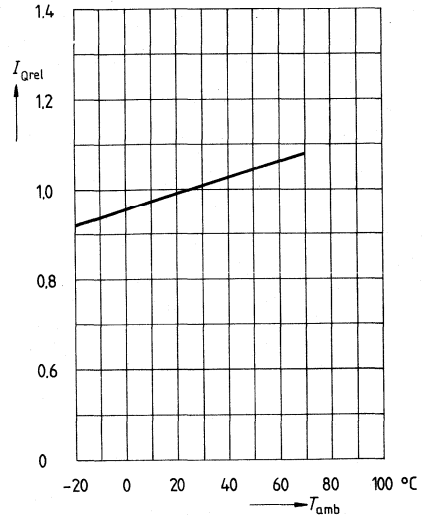


The output can be inhibited by connecting the balancing input with the stabilized voltage (switch, PNP transistor, FET).

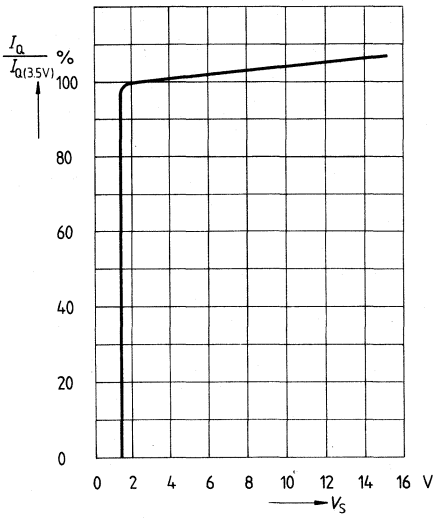
Relative spectral sensitivity versus wavelength



Relative output current versus ambient temperature
in range $E_v = 1$ lx to 1000 lx

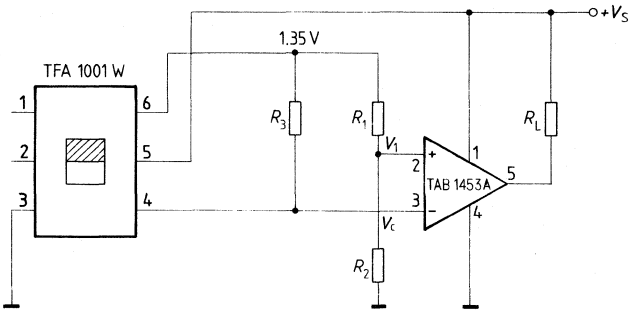


Output current versus supply voltage



Application examples

Simple threshold switch with TAB 1453 A op amp

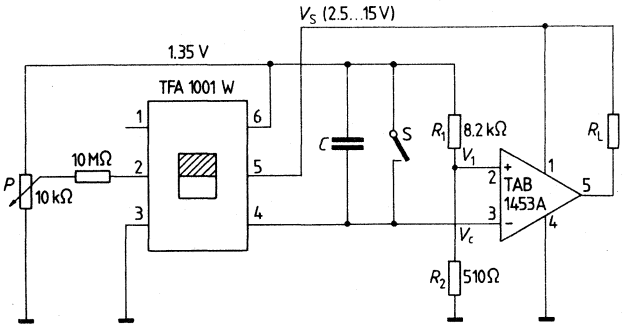


The illustration shows a simple threshold switch as can, for example, be used in cameras to change the aperture or indicate the illuminance. Operational amplifier TAB 1453 A serves as comparator. It has a PNP input and is able to operate at very low supply voltage.

The output is an open collector which can switch currents up to 70 mA.

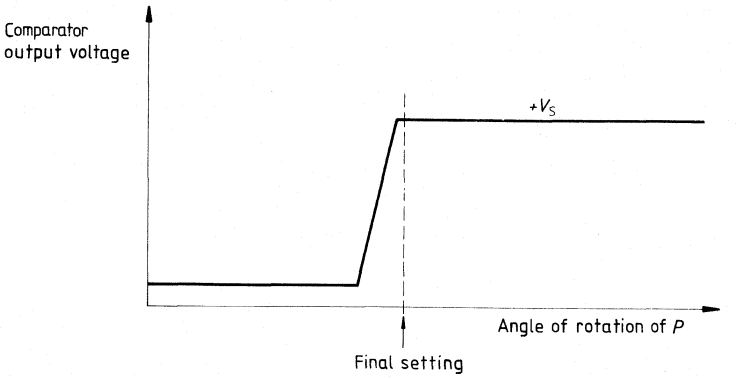
Since the stabilized voltage at pin 6 is used as reference voltage, the circuit is highly independent of the supply voltage.

Shutter speed or exposure control

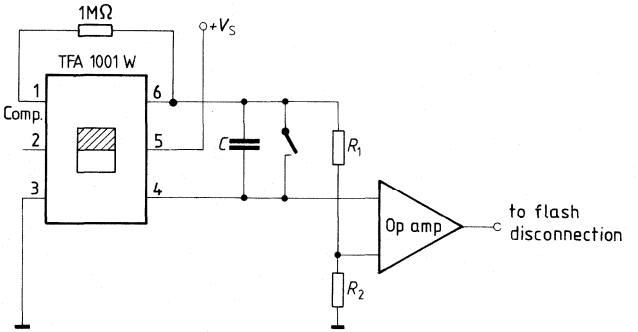


The illustration above shows a light/time control which can, e.g. be used to control the shutter speed in cameras or for exposure time control in enlargers. This circuit operates also largely independently of the supply voltage. A further essential advantage is, that for the major part of the exposure time the comparator input current is insignificant as the corresponding input transistor remains fully off-state. By means of potentiometer P, the operating range can be extended to lower illuminance values. Opening the switch starts the exposure, and capacitor C is charged from pin 4 of the photo IC. The comparator switches if the voltage V_C falls below the reference voltage determined by resistors R_1 and R_2. The relationship between illuminance and time is defined by capacitor C and precision adjustment is possible by means of V_1; V_1, however, must not become less than 0.4 V.

The dark current may be set in the circuit by means of potentiometer *P*. For this purpose, capacitor *C* is removed. *P* is then adjusted in darkness such that the output of the comparator is just blocked. Capacitor *C* is then inserted. (See illustration below).

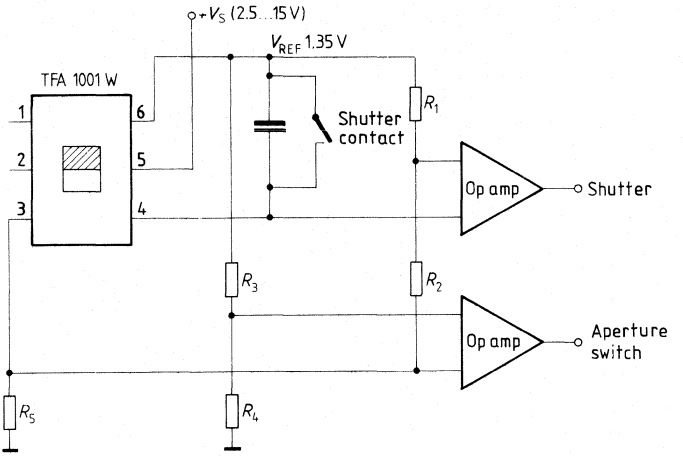


Schematic circuit diagram for an electronic flash control



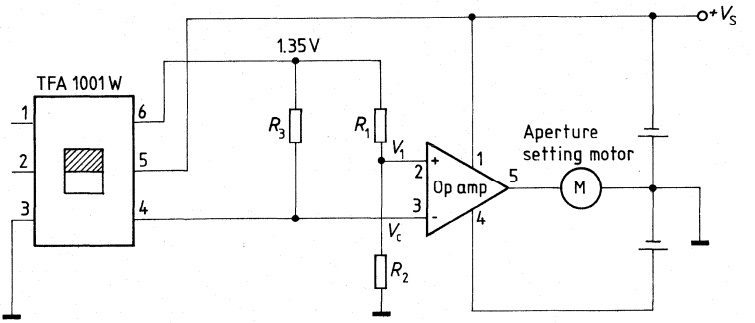
TFA 1001 W can also be used for electronic flash control. It must, however, be ensured that the illuminance does not exceed 5 klx; use a grey filter if necessary. To be able to control very short times, it is useful to connect an additional capacitor to pin 1.

Combined aperture and exposure control



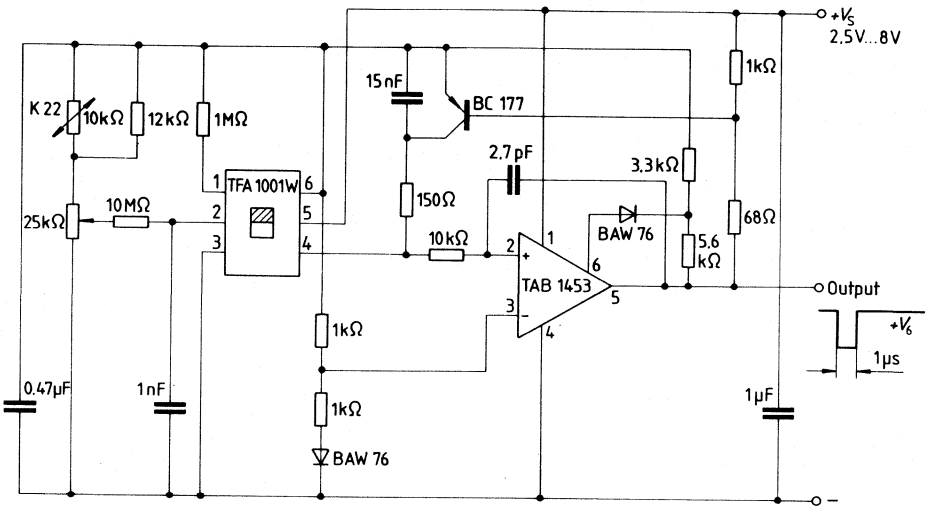
The aperture and exposure control may be combined, with the information for aperture switching being taken from the total current of the photo IC (voltage drop at R_5).

Aperture follow-up control for cine cameras



The op amp compares the voltage drop at R_3, generated by the photoelectric current, with a reference voltage derived from the stabilized voltage, and controls the aperture via motor M.

Light/frequency transducer



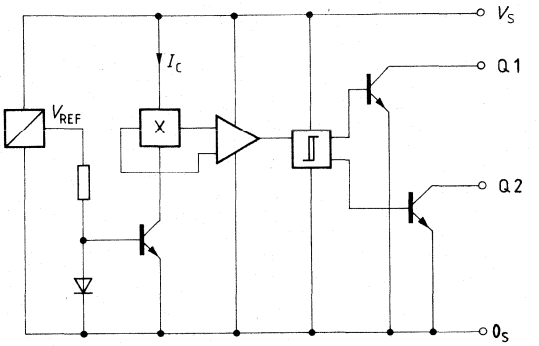
Sensitivity: approx. 600 Hz/lx
Range: 4 Hz to 400 000 Hz

- High resolution
- Fully temperature-compensated
- Wide operating voltage range
- High operating voltage suppression
- Wide dynamic range (5 decades)

Particularly suitable for digital processing.

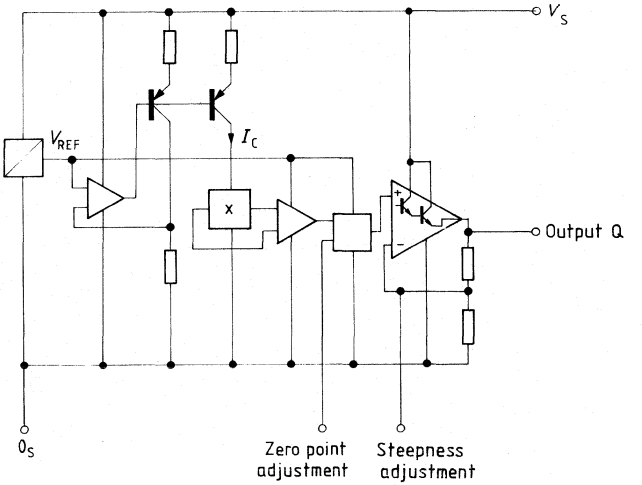
Block diagrams

Digital Hall-effect IC



The contactless, magnetically controlled switches contain on a semiconductor crystal, a constant voltage regulator, a regulated voltage source for the Hall generator, a differential amplifier, a Schmitt trigger, two driver stages, and end transistors with open collector. Their use is of advantage when high reliability, no bounce pulses, no affects by dirt and corosion, and a long service life are required.

Linear Hall-effect IC



The hall generator is fed from a constant voltage source which uses a regulated voltage as reference. The Hall generator is followed by a differential amplifier. In the subsequent stage, the differential signal is converted into a ground-referenced signal.

At this point, the offset can be changed in a manner that is simple and not prone to interference, by the subtraction or addition of a current.

The inverted amplifier input has been brought out, so that the steepness of the output characterististc (amplification) can be varied within a wide range by means of external components.

The ICs SAS 241, SAS 250, SAS 251, SAS 261 are magnetically operated, contactless switches with the following operating modes:

Type	Code	Supply voltage range	Function
SAS 241	SAS 241	4.75 to 18 V	Switch; dynamic
SAS 241 S4	white	4.75 to 5.25 V	open collector outputs
SAS 250	SAS 250	4.5 to 27 V	
SAS 251	SAS 251	4.75 to 27 V	Switch; static
SAS 251 S4	SAS 251 S4	4.75 to 5.25 V	open collector outputs
SAS 251 S5	orange	4.75 to 18 V	
SAS 261	blue	4.75 to 18 V	Switch; static
SAS 261 S4	green	4.75 to 5.25 V	open collector output and enable input

All ICs are available in a four-pin flat package. SAS 241 and SAS 251 are, upon request, also available as film-mounted version in a MICROPACK.

The IC SAS 231 supplies a voltage proportional to the magnetic flux density. Due to its MICROPACK design, it is particularly suitable for operation in very small air gaps.

Type	Code	Supply voltage range	Function
SAS 231 L	–	4.75 to 15 V	Hall IC with output voltage proportional to magnetic field; MICROPACK
SAS 231 W	blue/green	4.75 to 15 V	Hall IC with output voltage proportional to magnetic field; miniature plastic package

Hall-Effect IC with Output Voltage Proportional to Magnetic Field

■SAS 231 L
■SAS 231 W

Bipolar IC

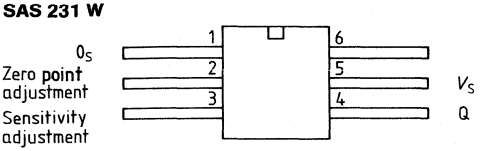
Type	Ordering code	Package	Fig. No.
■SAS 231 L	Q67000-A1468-L	MICROPACK	31
■SAS 231 W	Q67000-A1468-W	Miniature plastic package, 6 pins	23

The IC SAS 231 generates an output voltage proportional to the magnetic flux density. The output voltage increases when the south pole of a magnet approaches the top surface of the chip. The zero point is adjusted by external components. The steepness of the characteristic curve V_Q as a function of B can be varied by external components.

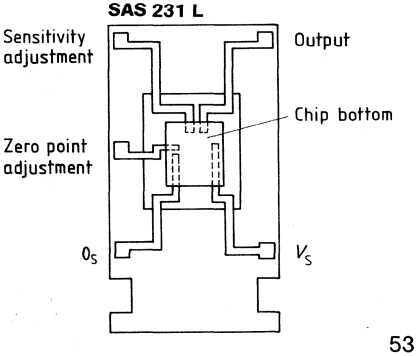
Maximum ratings		Test conditions	Lower limit B	typ	Upper limit A	
Supply voltage	V_S		0		18	V
Output current	I_Q				10	mA
Storage temperature	T_{stg}		−40		125	°C
Operating range						
Supply voltage	V_S		4.75		15	V
Output current	I_Q				5	mA
Ambient temperature	T_{amb}		0		70	°C
Electrical characteristics						
$V_S = 10$ V, $T_{amb} = 25$ °C, unless otherwise specified						
Open-loop supply current consumption	I_S	$R_L = \infty$		6	10	mA
Output voltage	V_Q	$R_L = 10$ kΩ	0.05		V_S-2	V
Steepness (without adjustment)	S		60	100	140	mV/mT
"Zero" component	B_0	$V_Q = 0.5$ V	−35		35	mT
Linearity error (referred to $V_Q = \frac{V_S}{2}$)				2		%
Temperature coefficient	α	T_{amb}=0°C to 70°C		0.4		mT/K

Pin configurations

SAS 231 W

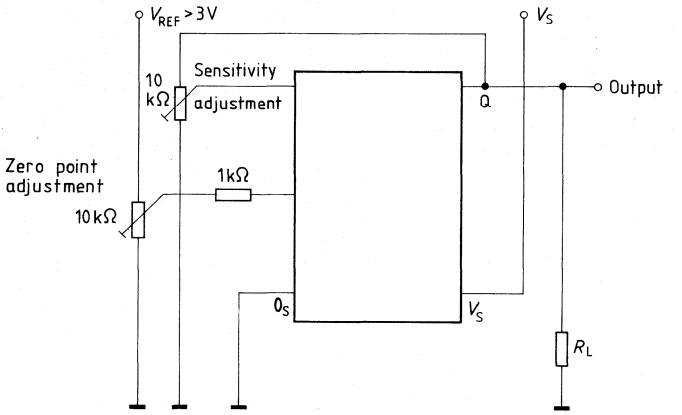


SAS 231 L



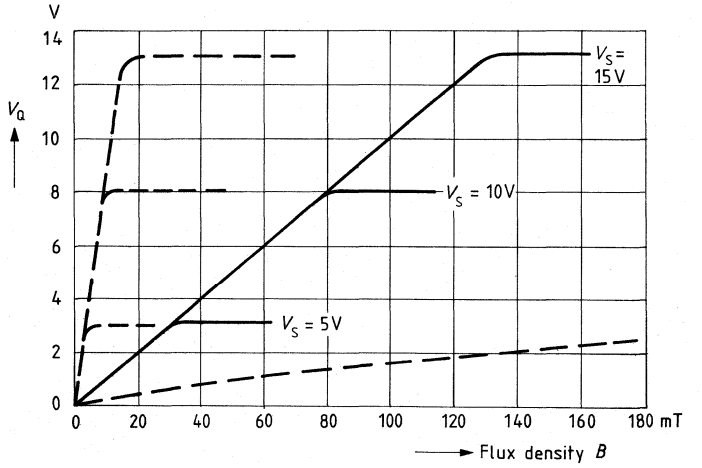
■ not for new design

Application circuit



Output characteristic without adjustment

Output voltage versus flux density



Magnetically Operated, Contactless Switch with Dynamic Outputs

■ SAS 241
■ SAS 241 S4

Bipolar IC

Type	Ordering code	Package	Fig. No.
■ SAS 241	Q67000-S50	Plastic flat-pack, 4 pins	19
■ SAS 241 S4	Q67000-S50-S4		

The ICs SAS 241 and SAS 241 S4 are contactless switches which are operated by a magnetic field. The outputs with open collectors permit wired AND connections for the generation of encoded signals. The outputs Q1 and Q2 generate signals of identical phase which are independent of the duration of action of the magnetic field. The south pole of the magnetic field must act vertically on the surface marked by the notch.

Maximum ratings

		Test conditions	Lower limit B	typ	Upper limit A	
Supply voltage	V_S		−0.5		20	V
Output current	I_{Q1}, I_{Q2}				30	mA
Junction temperature	T_j				150	°C
Storage temperature	T_{stg}		−40		125	°C
Thermal resistance (system-air)	$R_{th\,SA}$				170	K/W

Operating range

Supply voltage						
SAS 241	V_S		4.75		18	V
SAS 241 S4	V_S		4.75		5.25	V
Ambient temperature	T_{amb}		0		70	°C

Electrical characteristics

$V_S = 5$ V, $T_{amb} = 0$ °C to 70 °C, unless otherwise specified

Supply current	I_S	$B < B_{OFF}$	1		3	mA
	I_S	$B > B_{ON}$, Q1, Q2=H			3.5	mA
	I_S	$B > B_{ON}$, Q1, Q2=L	1.5		6	mA
Flux density for "ON"	B_{ON}				65	mT
Flux density for "OFF"						
SAS 241	B_{OFF}		10			mT
	B_{OFF}	$V_S = 18$ V	5			mT
SAS 241 S4	B_{OFF}		5			mT
Maximum temperature deviation referred to 25 °C	$\Delta B_{ON}/B_{OFF}$		−5		5	mT
Hysteresis	B_{hy}		4	10	15	mT
Output current	I_{Q1}, I_{Q2}	$B \leq B_{OFF}$			10	µA
Output voltage	V_{Q1}, V_{Q2}	$I_{Q1} = I_{Q2} = 16$ mA			0.4	V

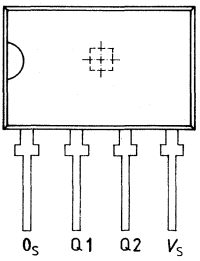
Delay times

$V_S = 5$ V; $T_{amb} = 25$ °C

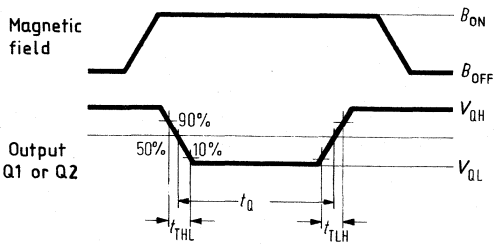
Transition time	t_{THL}	betw. 90 and 10%			1	µs
	t_{TLH}	betw. 10 and 90%			2	µs
Output pulse width	t_Q	betw. 50 and 50%	15	20	40	µs

■ not for new design

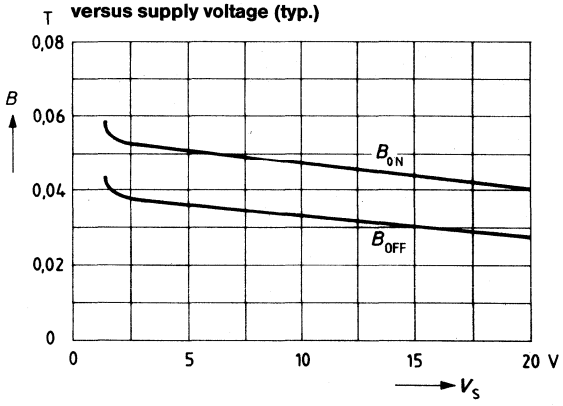
Pin configuration



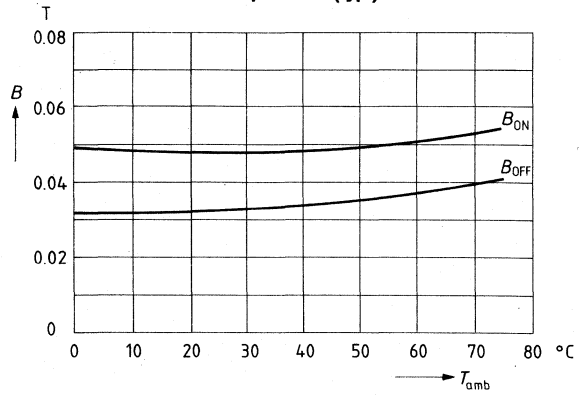
Pulse diagram



Flux density for ON and OFF versus supply voltage (typ.)



Flux density for ON and OFF versus ambient temperature (typ.)



Magnetically Operated, Contactless Switch for Extended Ambient Temperature

■ SAS 250

Bipolar IC

Type	Ordering code	Package	Fig. No.
■ SAS 250	Q67000-S46	Plastic flat-pack, 4 pins	19

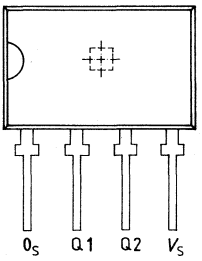
The IC SAS 250 is a contactless switch operated by a magnetic field. The outputs with open collectors permit wired AND connections for the generation of encoded signals. Outputs Q 1 and Q2 generate signals of identical phase. The south pole of the magnetic field must act vertically on the surface marked by a notch.

Maximum ratings		Test conditions	Lower limit B	typ	Upper limit A	
Supply voltage	V_S		0		30	V
Output current	I_{Q1}, I_{Q2}		0		30	mA
Junction temperature	T_j				150	°C
Storage temperature	T_{stg}		−40		125	°C
Thermal resistance (system-air)	$R_{th\,SA}$				170	K/W
Operating range						
Ambient temperature	T_{amb}		−40		125	°C
Supply voltage	V_S		4.5		27	V
Electrical characteristics $V_S = 5$ V, $T_{amb} = 25$ °C						
Supply current	I_S	$B < B_{OFF}$			3	mA
		$B > B_{ON}$			6	mA
Flux density for "ON"[1]	B_{ON}				65	mT
Flux density for "OFF"[1]	B_{OFF}		10			mT
Hysteresis	B_{hy}		4	10	15	mT
Output current	$-I_{Q1}$, $-I_{Q2}$	$B < B_{OFF}$			10	µA
Output voltage	V_{Q1}, V_{Q2}	$I_{Q1} = I_{Q2} = 16$ mA			0.4	V
Delay times						
Transition time	t_{HL}	betw. 10 and 90%			1	µs
	t_{LH}	betw. 90 and 10%			2	µs

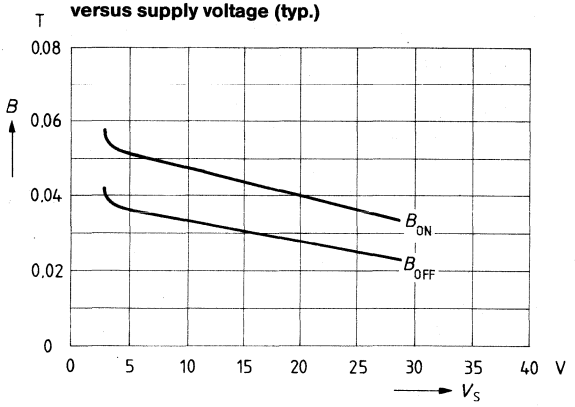
1) Temperature dependence: "ON" flux density B_{ON} and "OFF" flux density B_{OFF} referred to 25 °C within a temperature range between −40 °C and +125 °C ≤ ± 0.0075 T.

■ not for new design

Pin configuration



Flux density for ON and OFF versus supply voltage (typ.)



Magnetically Operated, Contactless Switch with Static Outputs

SAS 251
SAS 251 S4
SAS 251 S5

Bipolar IC

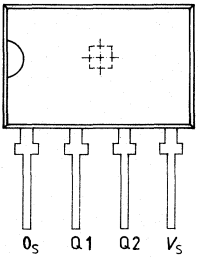
Type	Ordering code	Package	Fig. No.
SAS 251	Q67000-S47	Plastic flat-pack 4 pins	19
SAS 251 S4	Q67000-S47-S4		
SAS 251 S5	Q67000-S47-S5		

The ICs SAS 251, SAS 251 S4, and SAS 251 S5 are contactless switches which are operated by a magnetic field.

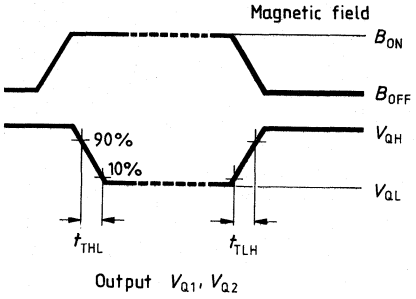
The outputs with open collectors permit wired AND connections for generation of encoded signals. The outputs Q1 and Q2 generate signals of identical phase. The south pole of the magnetic field must act vertically on the surface marked by the notch.

Maximum ratings		Test conditions	Lower limit B	typ	Upper limit A	
Supply voltage						
SAS 251	V_S		−0.5		30	V
SAS 251 S4, SAS 251 S5	V_S		−0.5		20	V
Output current	I_{Q1}, I_{Q2}				30	mA
Junction temperature	T_j				150	°C
Storage temperature	T_{stg}		−40		125	°C
Thermal resistance (system-air)	$R_{th\,SA}$				170	K/W
Operating range						
Supply voltage						
SAS 251	V_S		4.75		27	V
SAS 251 S4	V_S		4.75		5.25	V
SAS 251 S5	V_S		4.75		18	V
Ambient temperature	T_{amb}		0		70	°C
Electrical characteristics						
$V_S = 5$ V, $T_{amb} = 0$ °C to 70 °C, unless otherwise specified						
Supply current	I_S	$B < B_{OFF}$	1		3	mA
	I_S	$B > B_{ON}$	1.5		6	mA
Flux density for "ON"	B_{ON}				65	mT
Flux density for "OFF"						
SAS 251, SAS 251 S5	B_{OFF}		10			mT
SAS 251	B_{OFF}	$V_S = 27$ V	5			mT
SAS 251 S5	B_{OFF}	$V_S = 18$ V	5			mT
SAS 251 S4	B_{OFF}		5			mT
Maximum temperature deviation referred to 25 °C	$\Delta B_{ON}/B_{OFF}$		−5		5	mT
Hysteresis	B_{hy}		4	10	15	mT
Output leakage current	I_{Q1}, I_{Q2}	$B < B_{OFF}$			10	µA
Output voltage	V_{Q1}, V_{Q2}	$I_{Q1} = I_{Q2} = 16$ mA			0.4	V
Delay times						
$V_S = 5$ V; $T_{amb} = 25$ °C						
Transition time	t_{THL}	betw. 90 and 10%			1	µs
	t_{TLH}	betw. 10 and 90%			2	µs

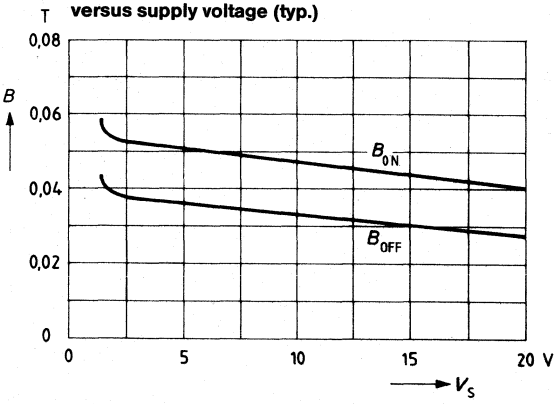
Pin configuration



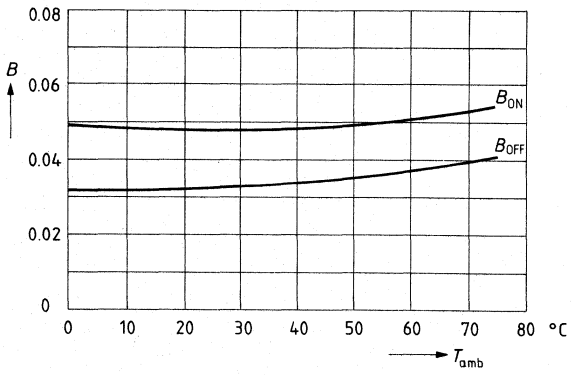
Pulse diagram



Flux density for ON and OFF versus supply voltage (typ.)



Flux density for ON and OFF versus ambient temperature (typ.)



Magnetically Operated, Contactless Switch with Enable Input

■ SAS 261
■ SAS 261 S4

Bipolar IC

Type	Ordering code	Package	Fig. No.
■ SAS 261	Q67000-S59	Plastic flat-pack, 4 pins	19
■ SAS 261 S4	Q67000-S59-S4		

The ICs SAS 261 and SAS 261 S4 are contactless switches which are operated by a magnetic field. If a sufficiently high flux density is available ($B = B_{ON}$) and an H signal is present at the enable input, the open collector output Q switches from H to L. The south pole of the magnetic field must act vertically on the surface marked by the notch.

Maximum ratings		Test conditions	Lower limit B	typ	Upper limit A	
Supply voltage	V_S		−0.5		20	V
Output current	I_Q				30	mA
Input voltage at E	V_E		−0.5		5	V
Junction temperature	T_j				150	°C
Storage temperature	T_{stg}		−40		125	°C
Thermal resistance (system-air)	$R_{th\,SA}$				170	K/W
Operating range						
Supply voltage						
SAS 261	V_S		4.75		18	V
SAS 261 S4	V_S		4.75		5.25	V
Ambient temperature	T_{amb}		0		70	°C
Electrical characteristics						
$V_S = 5$ V, $T_{amb} = 0$ °C to 70 °C, unless otherwise specified						
Supply current	I_S	V_E=0.4V, B any val.			500	µA
	I_S	V_E=2.4 V, $B > B_{ON}$	1.5		5	mA
	I_S	V_E=2.4 V, $B < B_{OFF}$	1		3	mA
Flux density for "ON"	B_{ON}				65	mT
Flux density for "OFF"						
SAS 261	B_{OFF}		10			mT
	B_{OFF}	$V_S = 18$ V	5			mT
SAS 261 S4	B_{OFF}		5			mT
Maximum temperature deviation referred to 25 °C	$\Delta B_{ON}/B_{OFF}$		−5		5	mT
Hysteresis	B_{hy}		4	10	15	mT
H input voltage at E	V_{IH}		2.4			V
L input voltage at E	V_{IL}				0.8	V
H input current at E	I_{IH}	$V_E = 2.4$ V			0.5	µA
L input current at E	I_{IL}	$V_E = 0.8$ V			5	µA
Output leakage current	I_Q	V_E=0.8V, B any val.			10	µA
		$V_E = 2.4$ V, $B < B_{OFF}$			10	µA
		$V_Q = V_S$				µA
Output voltage	V_Q	$V_E = 2.4$ V, $B > B_{ON}$			0.4	V
		$I_Q = 16$ mA				

■ not for new design

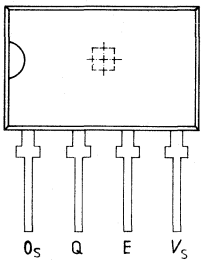
Delay times
$V_S = 5$ V; $T_{amb} = 25$ °C

		Test conditions	Lower limit B	typ	Upper limit A	
Propagation delay from E to Q	t_{PHL}	between 50 and 50%		0.4	3	µs
	t_{PLH}	between 50 and 50%		1	4	µs
Transition times	t_{THL}	between 90 and 10%			1	µs
at Q	t_{TLH}	between 10 and 90%			2	µs
at enable	t_T	between 10 and 90%	1			V/µs

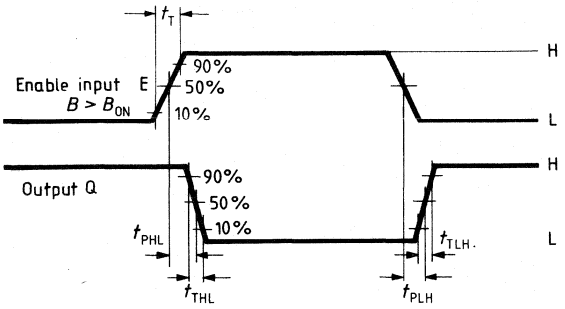
Truth table

Enable input	$B > B_{ON}$	$B < B_{OFF}$	Output Q
L	X		H
L		X	H
H	X		L
H		X	H

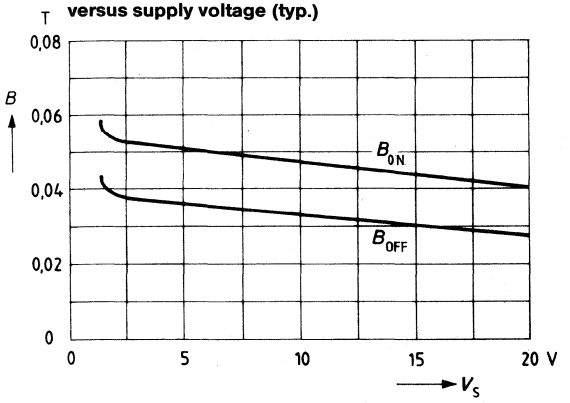
Pin configuration



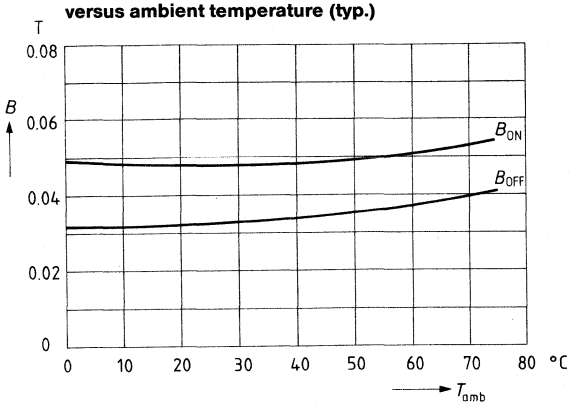
Pulse diagram



Flux density for ON and OFF versus supply voltage (typ.)



Flux density for ON and OFF versus ambient temperature (typ.)



Type	Ordering code	Package	Fig. No.
HKZ 101	Q67000-S64	Special package	20
HKZ 101 S[1)]	Q67000-S65-E10		

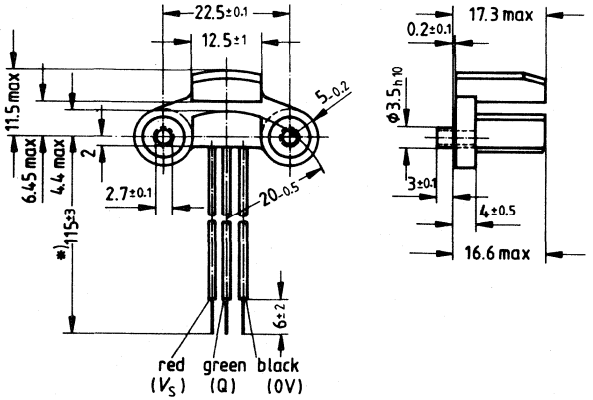
The Hall-effect vane switch HKZ 101 is a contactless switch consisting of a monolithic integrated Hall-effect circuit and a special magnetic circuit hermetically sealed in a plastic package. The switch is actuated by a shoft-iron vane which is passed through the air gap between magnet and Hall sensor.

The main application field is in cars, i.e. as a breakerless trigger in electronic ignition systems. Numerous industrial applications can be found in control engineering, especially in those areas where switches must operate maintenance-free under harsh environmetal conditions (e.g. rpm sensor, limit switch, position sensor, speed measurement, shaft encoder, scanning of coding disks, etc.).

Features

- Contactless switch with open collector output (40 mA)
- Static switching
- High switching frequency
- Hermetically sealed with plastic
- Unaffected by dirt, light, vibration
- Large temperature and voltage range
- Integrated overvoltage protection
- High interference immunity

Special package



*) Change to 130±3 mm in preparation

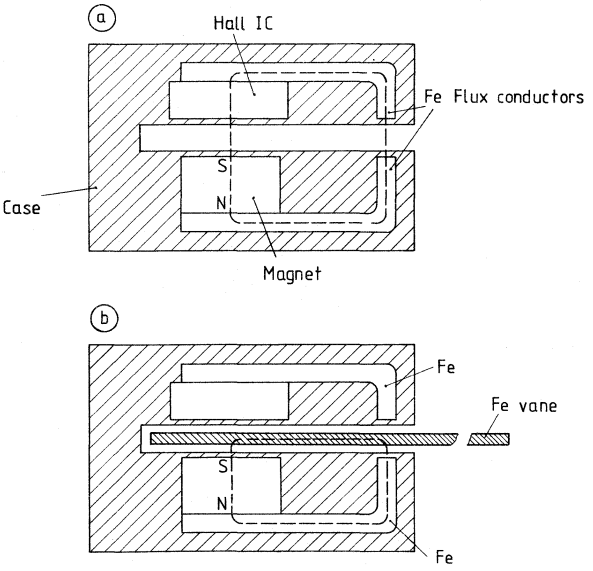
1) The temperature range of the HKZ 101S has been extended to between −40 °C and 130 °C (previously 0 °C to 70 °C), and the switching-point characteristics have been adapted accordingly.

Function

The Hall-effect switch is actuated by a soft-iron vane that passes through the air gap between magnet and Hall-effect sensor. The vane short-circuits the magnetic flux before the Hall-effect sensor, as shown in figure 1. The open collector output is conductive (LOW) when the vane is outside the air gap, and blocks (HIGH) when the vane is introduced into the air gap. The output remains HIGH as long as the vane remains in the air gap. This static function does not require a minimum operating frequency. The output signal shape is independent of the operating frequency.

The circuit features integrated overvoltage protection against most of the voltage peaks occurring in automotive and industrial applications. The output stage has a Schmitt trigger characteristic. Most electronic circuits can be driven directly due to the open collector output current of max. 40 mA.

Principle of operation



a) Magnetic flux through the Hall-effect switch with no vane in the gap

b) Magnetic flux short-circuited by the soft-iron vane

Figure 1

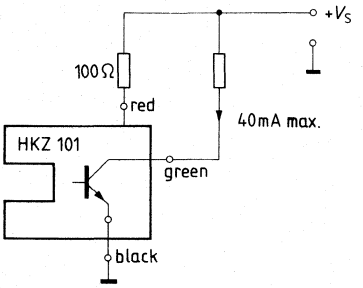
Mechanical characteristics

The Hall-effect vane switch is hermetically sealed in a special plastic, so that it can also be used under harsh environmental conditions. The package is waterproof, vibration-resistant and resistant to gasoline, oil and salt. Two tubular rivets are incorporated in the package to mount the sensor on its carrier plate. The circuit has three flexible leads for power supply and output.

Application notes

The output current of the "open collector" must be limited to the maximum permissible value by a load resistor adapted to the application.

For optimum efficiency of the integrated overvoltage protection, it is suggested that a resistor of approx. 100 Ω be provided in the component's power supply to limit the current.



Maximum ratings		Test conditions	Lower limit B	Upper limit A	
Supply voltage	V_S		−1.2	24	V
		$T_{amb} = 25\,°C$		30	V
Output voltage in OFF-state	V_Q		−0.8	30	V
Inverse supply current (limited externally)	$-I_S$	$T_{amb} \leq 80\,°C$ $t \leq 1$ h		200	mA
Output current	I_Q	without vane		40	mA
Inverse output current	$-I_Q$			30	mA
Ambient temperature during operation	T_{amb}		−40	135	°C
Storage temperature	T_{stg}		−40	150	°C
Thermal resistance (system-air)	$R_{th\,SA}$			170	K/W

Operating range					
Ambient temperature	T_{amb}		−40	130	°C
Supply voltage	V_S		4.5	24	V
Vane[1]: thickness	a		0.5		mm
width	b		8		mm
gap length	c		8		mm
immersion depth	h		4.6	9	mm
gap height	d		17.3−h		mm

1) see figure 3

Characteristics $V_S = 5$ V to 18 V; $T_{amb} = -30$ °C to 130 °C		Test conditions	Lower limit B	Upper limit A	
Output saturation voltage	$V_{Q\,sat}$	without vane $I_Q = 40$ mA			
		$T_{amb} = -30$ to 110 °C		0.4	V
		$T_{amb} = 110$ to 130 °C		0.6	V
Output reverse current	I_{QR}	with vane		10	µA
Supply current	I_S	without vane		12	mA
Delay time	t_{LH}, t_{HL}	$I_Q = 40$ mA		1	µs
Overvoltage protection					
– Supply voltage (V_S)	V_{SZ}	$I_S = 16$ mA	32	42	V
– Output (V_Q)	V_{SO}	$I_S = 16$ mA	32	42	V

Switching point characteristics

Definitions

In most applications, the switching point is set exactly by mechanical adjustment, thus compensating all mechanical tolerances in the system including the scatter of the Hall-effect vane switch. For the function of the device in operation, only the deviations of those characteristics depending on temperature and operating voltage are important.

The characteristic values of the switching points are, therefore, not directly referred to the mechanical dimensions of the vane switch, but to an electrically defined symmetry B_0 according to formula 1):

1) $B_0 = (ON_{left} + OFF_{left} + ON_{right} + OFF_{right}) : 4$
$B_0 = A_0 \pm 0.3$ mm

The definition of the operate and release points is shown in figure 2.

Operate point f_{ON} is obtained by subtracting the measured ON operate value from the reference point B_0:

2) $f_{ON} = ON_{right} - B_0 = B_0 - ON_{left}$

The release point f_{OFF} is calculated from the difference between the appropriate ON and OFF points:

3) $f_{OFF} = ON_{right} - OFF_{right} = OFF_{left} - ON_{left}$

$f_{ON\,0}$ and $f_{OFF\,0}$ are the switching points measured for the individual component under normal conditions ($V_S = 12$ V, $T_{amb} = 25$ °C) within the characteristic device deviation.

The deviations of the operate and release points are defined according to 4):

4) $\Delta f_{ON} = f_{ON} - f_{ON\,0}$
$\Delta f_{OFF} = f_{OFF} - f_{OFF\,0}$

Switching point definitions

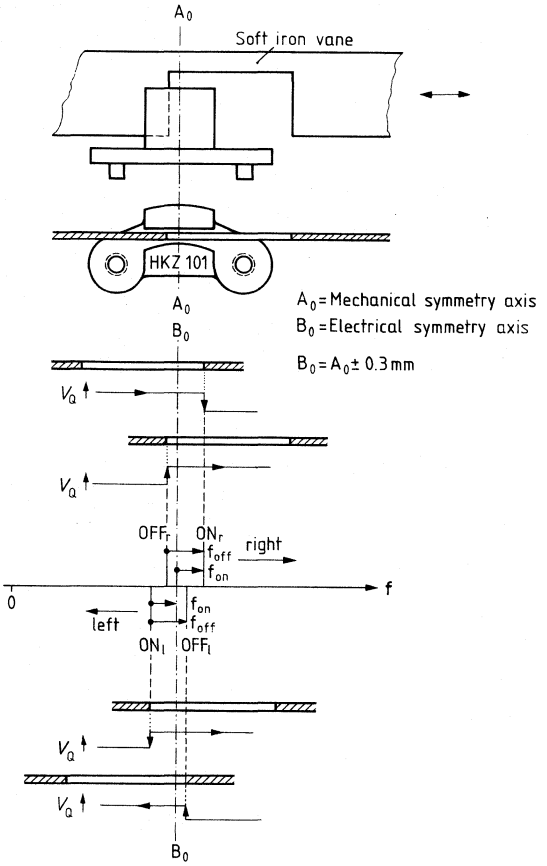


Figure 2

Mechanical measurement conditions

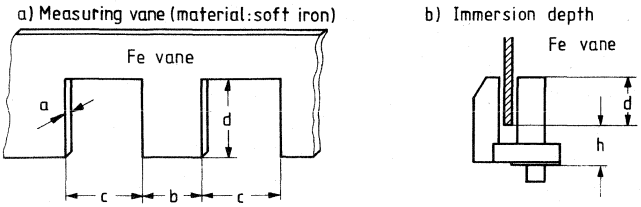


Figure 3

Switching point characteristics

Vane: a = 0.75 mm, b = 8 mm, c = 10 mm
Position: center of air gap
V_S = 5 V to 18 V

		Test conditions	Lower limit B	typ	Upper limit A	
HKZ 101						
Operate point	$f_{ON\,0}$	V_S = 12 V, T_{amb} = 25 °C	0.85	1.45	2.05	mm
Deviations	Δf_{ON}	T_{amb} = −30 to 25 °C	−0.4	+0.15	+0.7	mm
		T_{amb} = 25 to 80 °C	−0.2	+0.15	+0.4	mm
		T_{amb} = 80 to 130 °C	−0.4	+0.2	+0.7	mm
Release point	$f_{OFF\,0}$	V_S = 12 V, T_{amb} = 25 °C	1.54	2.54	3.54	mm
Deviations	Δf_{OFF}	T_{amb} = −30 to 25 °C	−0.8	+0.3	1.4	mm
		T_{amb} = 25 to 80 °C	−0.4	+0.3	0.8	mm
		T_{amb} = 80 to 130 °C	−0.8	+0.4	1.4	mm
HKZ 101 S[1)]						
Operate point	$f_{ON\,0}$	V_S = 12 V, T_{amb} = 25 °C	0.65		2.3	mm
Deviations	Δf_{ON}	T_{amb} = −30 to 130 °C	−0.4		0.75	mm
Release point	$f_{OFF\,0}$	V_S = 12 V, T_{amb} = 25 °C	0.8		4.9	mm
Deviations	Δf_{OFF}	T_{amb} = −30 to 130 °C	−0.4		1.5	mm

1) The switching-point characteristics of the HKZ 101 S have been adapted to the extended temperature range.

Nonvolatile Memories

MOS IC

Type	Ordering code	Package	Fig. No.
SDA 2006	Q67100-Q264	DIP 18	11

Features

- Nonvolatile memory of electrical, word-organized reprogrammability, in n channel floating gate technology
- 512-bit storage capacity (32 words of 16 bits, each)
- Serial word address, chip select, and instruction input via an 8-bit or 12-bit control word (switchable by means of external components)
- Erase and write duration determined with the aid of chip-internal control
- Signal outputs with open-drain stages
  active signal inputs and outputs can be inverted by terminal wiring
- Number of reprogrammings $> 10^4$
- Unlimited number of read-out procedures without refresh
- Min. 10 years storage time

Maximum ratings

Supply voltage	$V_{DD\ 2\text{-}1}$	22	V
Supply voltage	$V_{PI\ 18\text{-}1}$	22	V
Supply voltage	$V_{PP\ 3\text{-}1}$	41	V
Input voltage	$V_{i\text{-}17}$	16	V
Total power dissipation	P_{tot}	400	mW
Storage temperatur range	T_{stg}	−40 to 125	°C
Thermal resistance (system-air)	$R_{th\ SA}$	90	K/W

Operating range

referred to $V_{SS} = 0$ V

Supply voltage range	$V_{DD\ 2}$	14 to 16	V
Ambient temperature range	T_{amb}	0 to 70	°C

Static characteristics (all voltages are referred to $V_{SS} = 0$ V)

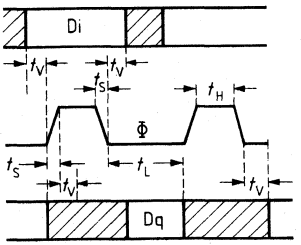
		min	typ	max	
Supply current	I_{DD2}		10	20	mA
Substrate bias	$-V_{BB1}$	4		6	V
Substrate current					
Substrate current, average current	$-I_{BB1a}$ [1]		0.5	2	mA
Substrate current, peak pulse current	$-I_{BB1p}$ [1]			10	mA
Programming voltage	V_{PP3} [1]		33	35	V
Programming current, quiescent current	I_{PP3}		0.1		mA
Programming current, average current	I_{PP3a}		2	5	mA
Programming current, peak pulse current	I_{PP3p}		5	10	mA
Write voltage	V_{PI18} [1]		15	16	V
Write current, quiescent current	I_{PI18}		0.1		mA
Write current, average current	I_{PI18a}		5	20	mA
Write current, peak pulse current	I_{PI18p}		15	50	mA
Inputs					
Di	$V_{L8,12,16}$	0		0.5	V
$\Phi/\overline{\Phi}$	$V_{H8,12,16}$	4		V_{DD}	V
REC/$\overline{\text{REC}}$	$I_{H8,12,16}$			10	µA
($V_H = V_{DD}$)					
STWL					
($-I_L = 100$ µA, pull-up resistors)	$V_{L4,15,9,11,10}$	0		0.5	V
INV	$V_{H4,15,9,11,10}$	4		V_{DD}	V
CS3	$I_{H4,15,9,11,10}$			10	µA
CS1, CS2					
(with a control word of 12 bits only; $V_H = V_{DD}$)	$I_{H4,15,9,11,10}$			10	µA
($V_L = 0$ V; $V_H = V_{DD}$)	$I_{L4,15,9,11,10}$			300	µA
$\overline{\text{RES}}$	V_{L6}	0		0.5	V
	V_{H6}	4		V_{DD}	V
($V_L = 0$ V)	$-I_L$			200	µA
($V_H = V_{DD}$)	I_H			200	µA
Outputs					
Dq/$\overline{\text{D}}_q$, $\overline{\text{L}}$/L	$V_{L14,13}$			0.5	V
($I_L = 1$ mA; open-drain stages)					
($V_H = V_{DD}$)	$I_{H14,13}$			10	µA

1) only necessary during programming

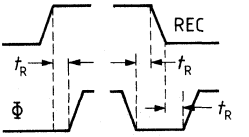
Dynamic characteristics

		min	typ	max	
Data bus					
Φ – clock	t_H	5			µs
INV on low	$-t_L$	10			µs
Φ – clock	t_H	10			µs
INV on high	t_L	5			µs
	t_V	5			µs
	t_S			2	µs
Signal edge distance	t_R	5			µs
INV on low or high					
Programming duration	t_{prog}		0.1	1	s
(V_{PP} = 33 V, V_{PI} = 15 V)					
Programming frequency	f_{prog}			1	Hz

INV on low



Signal edge distance



Circuit description

Data transfer

Data transfer with the SDA 2006 is performed serially via a 5-line bus, consisting of:

- Data input Di
- Data output Dq/$\overline{\text{Dq}}$
- Data input signal REC/$\overline{\text{REC}}$ (receive data)
- Clock input $\Phi/\overline{\Phi}$
- Programming output signal $\overline{\text{L}}$/L (load)

The active input or output levels, respectively, may be inverted via the input INV. They are switchable, as a group, in order to facilitate adaptation to different external circuits.

Terminal	Potential		Notes
INV	low (V_{SS})	high (V_{DD})	
Di/$\overline{\text{Dq}}$	Di = Dq	Di = $\overline{\text{Dq}}$	
REC/$\overline{\text{REC}}$	high	low	During data input
$\Phi/\overline{\Phi}$	high	low	Active shift pulse
$\overline{\text{L}}$/L	low	high	In the case of reprogramming

Chip control

The control information is entered via data input Di in the form of a control word, the length of which may be set via input STWL:

Terminal STWL	low	high (open or V_{DD})
Control word length	8 bits	12 bits

The control words contain information with respect to word address, chip address, and instruction, and have the following formats (A0 as LSB at first):

8-bit control word	A0 A1 A2 A3 A4 B1 B2 C3
12-bit control word	A0 A1 A2 A3 B0 B1 B2 B3 A4 C1 C2 C3

with A0.....A4 Word address bits
B0.....B3 Instruction bits
C1.....C3 Chip select bits

Instruction coding

12-bit control word				
B0	B1	B2	B3	Instruction
low	high	high	high	Read out, D9 as LSB
low	low	high	high	Read out, D1 as LSB
low	low	low	high	Programming
	8-bit control word			

Chip select

An instruction is only decoded in a memory, if the information of the chip select bits matches that of the chip select inputs.

Chip select – Terminal		Chip select – Bit	
	CS1 ◄⟶►	C1	
	CS2 ◄⟶►	C2	12-bit control word
8-bit control word	CS3 ◄⟶►	C3	

CS1 and CS2 remain unconnected in the case of the 8-bit control word.

Read-out (figure 1a and 1b)

Prior to the read operation of the memory the 8-bit or 12-bit control word must be serially clocked into the data input Di. 8 or 12 clock pulses, respectively, are necessary to enter the control word at the input $\Phi/\overline{\Phi}$. During input, the REC/$\overline{\text{REC}}$ input is active (active high for low at INV, active low for high at INV).

Information input is ended by means of the trailing edge of the REC/$\overline{\text{REC}}$ signal and the read-out instruction is decoded at chip select. As a result the data output Di/$\overline{\text{Dq}}$ changes into a low-ohmic state.

With the aid of a further clock pulse S, the read-out operation is initialized. The data is shifted with the trailing edge of additional clock pulses. The LSB arrives at the data output with the first of these pulses. During the read-out operation via the control word either the first data bit D1 or the ninth data bit D9 can be chosen as LSB. The read-out operation can be discontinued after any number of shift pulses. Thus, every stored 16-bit data word can also be read as two separated 8-bit data words.

Reprogramming (figure 2a and 2b)

Prior to programming, the 16-bit data word (D1 as LSB, first), then the 8-bit or 12-bit control word at the data input Di must be clocked in by means of the active REC/$\overline{\text{REC}}$ signal. The trailing edge of the REC/$\overline{\text{REC}}$ signal decodes the programming instruction at chip select. The reprogramming operation, however, only starts with the trailing edge of a further clock pulse and is forwarded to the memory controller via the $\overline{\text{L}}$/L signal.

The duration t_{prog} of the reprogramming mode is determined by chip-internal control. Independent of the external operating voltages V_{PP} and V_{PI}, erase and write operations are only completed after each memory has reached the desired state. During rewriting, the memory cannot be influenced externally, because the inputs REC/$\overline{\text{REC}}$, $\Phi/\overline{\Phi}$ and Di remain blocked. Premature termination of the operation can only be caused by zero level at the input $\overline{\text{RES}}$.

Reset function

A low level voltage at the input $\overline{\text{RES}}$ moves the memory into the reset state. A voltage divider is internally connected to the input and completes the reset state for $V_{DD} > 11$ V. In case of undefined signal and supply voltage levels during turn-on and turn-off, the input of the $\overline{\text{RES}}$ must be maintained on low during the entire turn-on and turn-off phase to avoid undesired decoding of a programming or read instruction. If the L status is not externally adjustable, it is advisable to connect the input $\overline{\text{RES}}$ (pin 6) via a 12 V diode to V_{DD} (pin 2) and via a 3 kΩ resistance to ground (pin 17).

Voltage supply

The SDA 2006 includes four extended voltage inputs V_{PP}, V_{PI}, V_{DD}, V_{BB} with respect to V_{SS} (ground). Normally, V_{DD} and V_{PI} are externally interconnected. The voltages V_{PP} and V_{PI} are only required during programming operations. During read out or in the quiescent state, they may also be open or grounded. The values of these voltages only influence the duration, but not the reliability of the nonvolatile storage operation. **Figure 3** shows an appropriate circuit configuration as tuning memory in TV sets.

Inverted level (input INV on high or open)

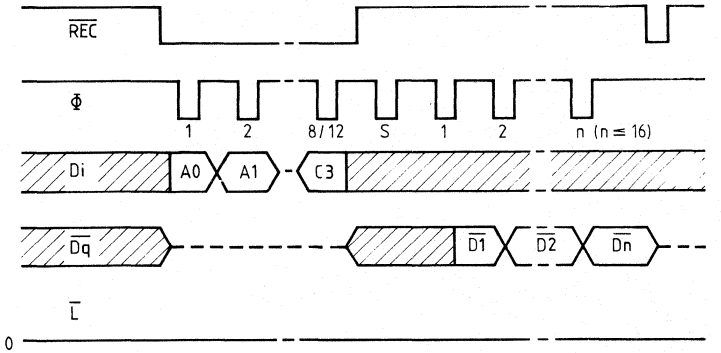


Figure 1a

Non-inverted level (input INV on low)

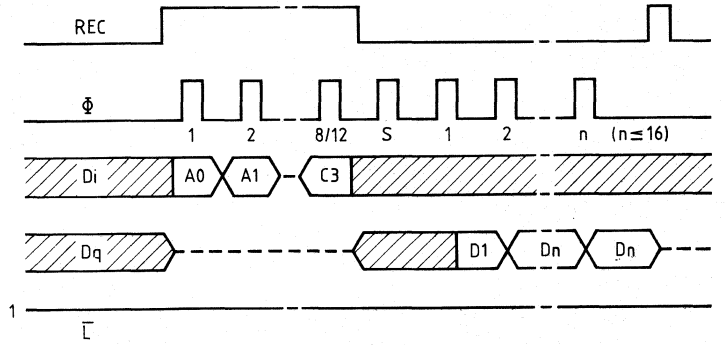


Figure 1b

Figures 1a and 1b **Read operation** (only pertinent active levels are indicated)

Inverted level (input INV on high or open)

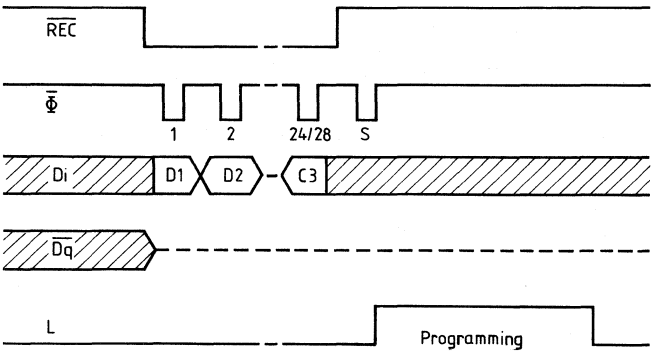


Figure 2a

Non-inverted level (input INV on low)

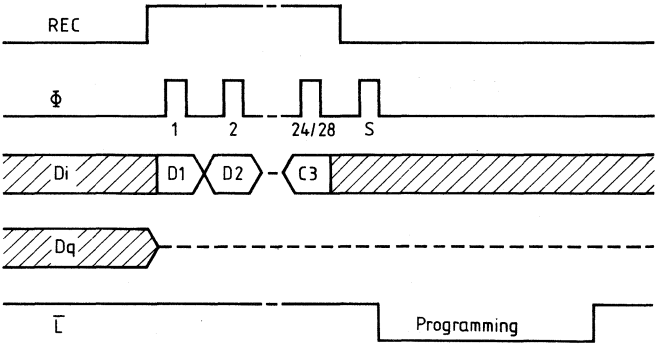


Figure 2b

Figures 2a and 2b Programming operation (only pertinent active levels are indicated)

Pin configuration

Pin No.	Symbol	Function
1	V_{BB}	Substrate bias
2	V_{DD}	Supply voltage
3	V_{PP}	Programming voltage
4	STWL	Control word length 12 or 8 bits (input) (12 bits for high or open)
5		Remains open
6	$\overline{RES}$	Reset input
7		Remains open
8	Di	Data input
9	CS3	Chip select input (8-bit or 12-bit control word)
10	CS2	Chip select input (12-bit control word)
11	CS1	Chip select input (12-bit control word)
12	$\Phi/\overline{\Phi}$	Clock input[1]
13	$\overline{L}/L$	Programming signal output (load)[1]
14	$Dq/\overline{Dq}$	Data output[1]
15	INV	Signal inverting (input)
16	$REC/\overline{REC}$	Data input control input (receive)[1]
17	V_{SS}	Ground
18	V_{PI}	Write voltage

1) First polarity for INV on low; second polarity for INV on high.

SDA 2006 as tuning memory in TV sets

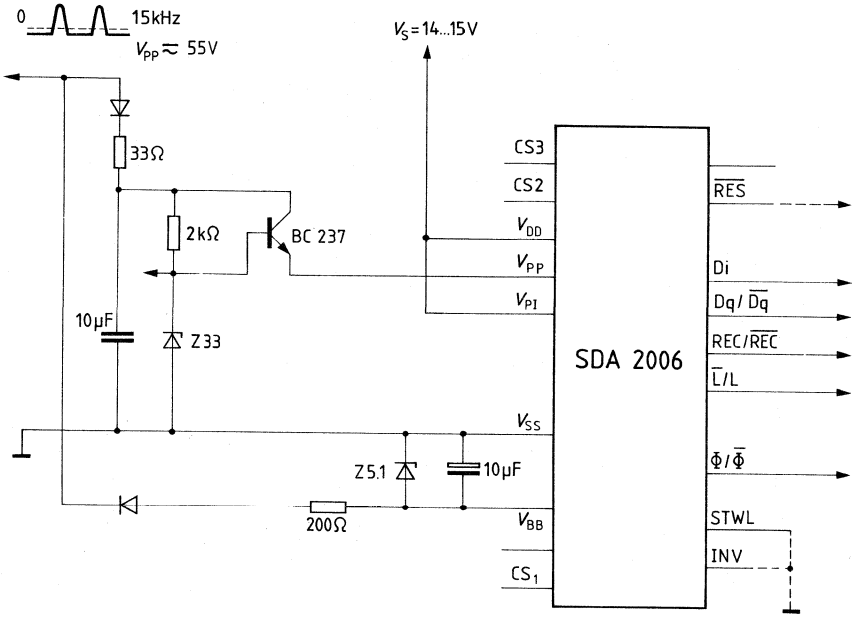


Figure 3

1Kbit Nonvolatile Memory (E^2 PROM) SDA 2116

Preliminary data **MOS IC**

Type	Ordering code	Package	Fig. No.
SDA 2116	Q67100-A2128	DIP 8	6

Features

- Electrically word-organized reprogrammable nonvolatile memory in n-channel floating-gate technology
- Organization 128 words by 8 bits each
- Supply voltage 5 V, programming voltage 24 V
- A total of 3 lines provides data transfer and chip control between processing unit and E^2PROM
- Data (8 bits), address (7 bits) and input of control information (1 bit) as well as serial data output
- Number of reprogramming cycles per address $>10^3$
- Data retention >10 years (within specified operating temperature range)
- Unlimited number of read-out procedures without refresh
- Erase and write cycle in 50 ms each

Maximum ratings

Supply voltage 1	V_{CC}	−0.3 to 6	V
Supply voltage 2	V_{pp}	−0.3 to 26	V
Input voltage range	V_i	−0.3 to 6	V
Storage temperature range	T_{stg}	−40 to 125	°C
Thermal resistance (system-air)	$R_{th\,SA}$	100	K/W

Operating range

Supply voltage range	V_{CC}	4.5 to 5.5	V
Ambient temperature range	T_{amb}	0 to 70	°C

Characteristics

		min.	typ.	max.	
Supply voltage 1	V_{CC}	4.5	5	5.5	V
Supply current 1	I_{CC}			5	mA
Supply voltage 2	V_{PP}	22.8[1)]	24[1)]	25.6[1)]	V
Supply current 2	I_{PP}			2	mA
Inputs	V_L			0.5	V
(D, Φ, $\overline{CE}$)	V_H	3.0			V
($V_H = 5.5$ V)	I_H			10	µA
Data output D (open drain)					
($V_L = 0.5$ V)	I_L			0.5	mA
($V_H = 5.5$ V)	I_H			10	µA
Clock pulse Φ					
High duration	Φ_H	2.5		60	µs
Low duration					
before/after Φ_H	Φ_L	5			µs
before/after $\overline{CE}$ alteration	Φ_L	5			µs
before/after D alteration	Φ_L	2.5			µs
Signal edge distance	Δt				
$\overline{CE}$ against D		2.5			µs
Erase time	t_{ET}	50			ms
Write time	t_{WR}	50			ms

1) Voltage peaks higher than the static value of V_{PP} must be avoided, e.g. by a 27 V diode between the inputs 6 and 1.

Data transfer and chip control

Total data transfer between processing unit and E^2PROM memory requires 3 lines, each of which controls several functions.

a) Data input D:
- bidirectional serial data transfer
- serial address input
- clocked input of control information
- control input directly

b) Clock input Φ:
- data, address, and control bit input
- data output
- start data output with data transfer from memory in shift register or start data change when reprogramming

c) Chip enable input $\overline{CE}$:
- chip reset and data input (active high)
- chip enabling (active low)

Prior to chip enabling the data address and control information will be clocked in via a bidirectional data bus. This data remains stored during reprogramming and during read until the 2nd clock pulse is generated. The following data formats have to be applied:

a) Memory read: one 8 bit control word, thereof
- 7 address bits A0 to A6 (A0 as LSB first)
- 1 control bit, SB = "0", after A6

b) Memory change (erase and/or write)
16-bit input information, thereof
- 8-bit D0 to D7 new memory information (D0 as LSB first)
- 7-bit A0 to A6 address information (A0 as LSB after D7 first)
- 1-bit control information, SB = "1", after A6

Read (figure 1)

After data input and with SB = "0" the read operation of the selected word address is started by the falling edge of $\overline{CE}$ from "1" to "0". The information on the data line is disregarded during chip activation.

With the aid of the first clock pulse after $\overline{CE}$ = "0" the data word is transferred out of the selected memory address into the shift register. After the first Φ-pulse has been terminated, the data output becomes low-ohmic and the first data bit D0 can be read. With each following clock pulse a further data bit will be passed to the output. The data line turns again high-ohmic at the rising edge of $\overline{CE}$ going from "0" to "1".

Reprogramming (figure 2)

A complete reprogramming operation normally consists of an erase cycle and a following write cycle. During erasing every bit of the selected word will be brought into the common "1" status, during writing the "0" states are generated depending on the information of the shift register.

A reprogramming cycle starts if, after the data input at chip enable, an information SB = "1" is set in the corresponding shift register location. Whether an erase or a write cycle is executed, depends again on the information of the data line D during chip activation.

Erasing into the "1" status requires a "1" at the data input during the falling edge $\overline{CE}$ to low. Should, however, a write cycle into "0" status be started, then a "0" must be on the data line during chip activation.

To start programming, a start pulse must be applied to clock input Φ, and the control information at D must remain stable until its rising edge. The active data change starts with the falling edge of this start pulse. The programming cycle will be terminated by a reset of the chip activation, i.e. by applying $\overline{CE}$ = "1".

The reprogramming of a word begins by starting and processing an erase cycle. $\overline{CE}$ = "1" ends the erase cycle. The control bit in the shift register SB = "1", which is also required for the write cycle, remains stable even after termination of the erase cycle. In order to write the selected word, the data line D has to be switched from "1" to "0" the chip must be activated again by $\overline{CE}$ = "0" and finally by means of the start pulse, the data change can be started.

The erase and write function can be performed separately. In order to obtain a stable "1" in all 8 bits of the selected memory address during erasing, a data word featuring 8 times "1" must be read in prior to the erasing process. In case a word is written into a previously not erased memory cell the "0" status of the previous and the new information will be added up.

RESET and supply voltages

A not addressed memory automatically remains in reset position through $\overline{CE}$ = "1". All flipflops in the process control section are reset. The information in the shift register, however, remains and will only be changed by shifting the data.

If the defined position of the signal levels (quiescent state $\overline{CE}$ = high, Φ = low) cannot be ensured at switching on or off the supply voltage, data losses upon unintended decoding of a programming instruction can be avoided by switching V_{PP} on after V_{CC} and off prior to V_{CC}.

Read cycle (1 Kbit E²PROM)

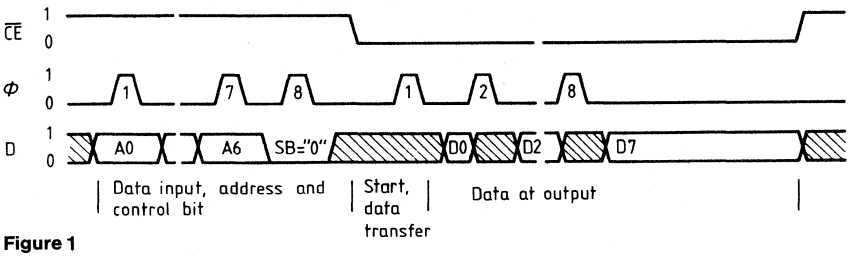


Figure 1

Reprogramming cycle (1 Kbit E²PROM)

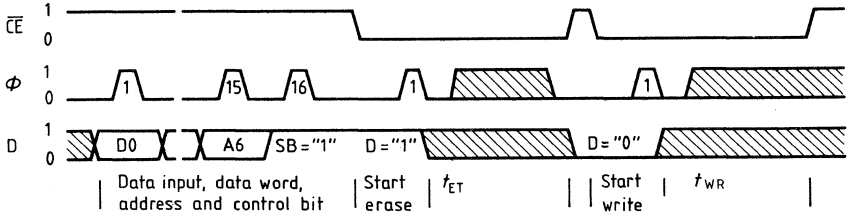


Figure 2

Pin configuration

Pin No.	Symbol	Function
1	V_{SS}	Ground
2	$\overline{CE}$	Chip enable
3	V_{CC}	Supply voltage 5 V
4	D	Data input/output
5	Φ	Clock input
6	V_{PP}	Programming voltage 25 V
7	TP	Test input, at V_{SS}
8	TG	Test input, remains open

Miscellaneous ICs

MOS IC

Type	Ordering code	Package	Fig. No.
S 178 A	Q67100-Z139	DIP 28	16

The S 178 A is an MOS circuit using p-channel metal-gate-technology with enhancement and depletion transistors, featuring the following technical characteristics:

The **video pulse generator** produces the sync, control, and erase signals required for the control of cameras, mixers, and other equipment.

The following signals are generated:

- Gating signal A
- Sync signal S
- Horizontal pulse H
- Vertical pulse V
- Terminal pulse K_t
- Horizontal gating pulse A (H)
- Double line frequency $H/_2$, half vertical frequency V_R → $H/_2 + V_R$ signal with external signal mixing
- Vidicon gating signal V_A

Features

All pulses are derived digitally from an input frequency corresponding to a pulse scheme, with a duty cycle of 1:1.

Pulse width according to latest CCIR and EIA standards.

The following 6 pulse schemes have been programmed permanently (by 3-bit coding and line number coding):

525 lines (60 Hz) required input frequency 1.008 MHz
625 lines (50 Hz) required input frequency 1.000 MHz
735 lines (60 Hz) required input frequency 1.4112 MHz
875 lines (50 Hz) required input frequency 1.400 MHz
1023 lines (60 Hz) required input frequency 1.96416 MHz
1249 lines (50 Hz) required input frequency 1.9984 MHz

Deviating from the above, any line number between 512 and 1535 lines may be programmed.

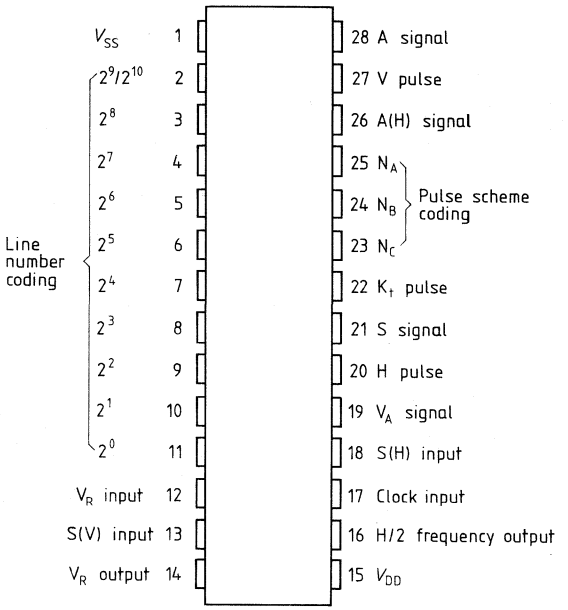
It should be noted, however, that a frame frequency of 50 Hz (partial picture duration 20 ms) or 60 Hz (16.66) is achieved.

Within the operating frequency it is, however, possible to mix any standard position with any line number.

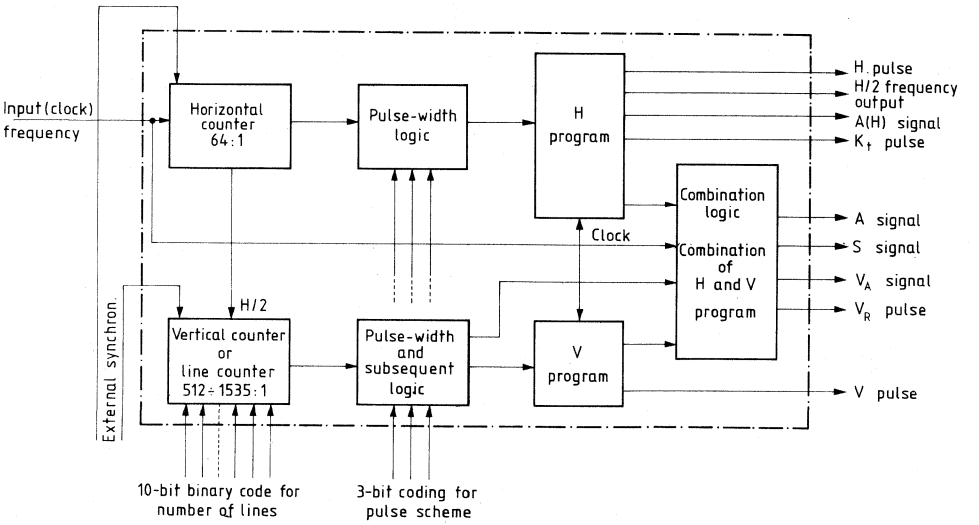
The following relation applies:

Input frequency f_I = 64: line period H
= 32: line number Z x frame frequency f_{fr}

Pin configuration
top view



Block diagram



Maximum ratings

		Lower limit B	Upper limit A	
Supply voltage } referred	V_{DD}	−12	0.3	V
Voltage at all inputs } to $V_{SS}=0$ V	V_I	−20	0.3	V
Input current ($V_I=0.3$ V; $V_{SS}=0$ V)	I_I		100	µA
Output current	I_{QH}		−100	µA
	I_{QL}		2	mA
Junction temperature	T_j		125	°C
Storage temperature	T_{stg}	−55	125	°C
Ambient temperature during operation	T_{amb}	−25	75	°C

Characteristics

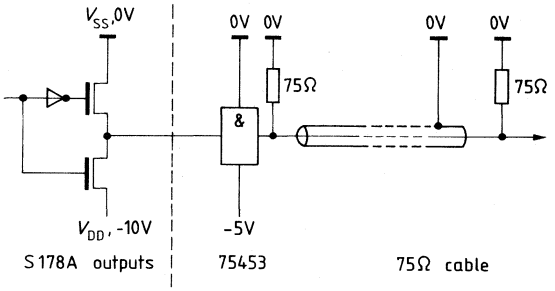
$T_{amb}=25$ °C

		Test conditions	Lower limit B	typ	Upper limit A	
Supply voltage	$-V_{DD}$		9.5	10	10.5	V
Supply current	I_{DD}			60	70	mA
Inputs		direct control with TTL output level				
H input voltage	V_{IH}		$V_{SS}-1.5$		V_{SS}	V
L input voltage	V_{IL}		$-V_{DD}$		$-V_{DD}+5.5$	V
Outputs		when loaded with one TTL input:				
H output voltage	V_{QH}	$I_{QH}=-40$ µA	$V_{SS}-2.6$			V
L output voltage	V_{QL}	$I_{QL}=1.6$ mA	TTL GND−0.7		TTL GND+0.4	V
		when loaded with 2 LPS inputs:				
H output voltage	V_{QH}	$I_{QH}=-40$ µA	$V_{SS}-2.6$			V
L output voltage	V_{QL}	$I_{QL}=0.8$ mA	LPS GND−0.7		LPS GND+0.4	V
		for capacitive load only:				
H output voltage	V_{QH}		$V_{SS}-2.6$			V
L output voltage	V_{QL}		V_{DD}		$V_{DD}+1$	V
Signal transition time of outputs	t_T	when loaded with 2 LPS inputs			100	ns
Input frequency	f_{CLK}		1		2	MHz
Propagation delay time	t_P	clock slope – signal output	0.2		0.4	µs

Interface to 75 Ω cable

A driver stage is required as the pulse generator outputs can be loaded with one TTL input, each. The circuit is to be designed according to the diagram below.

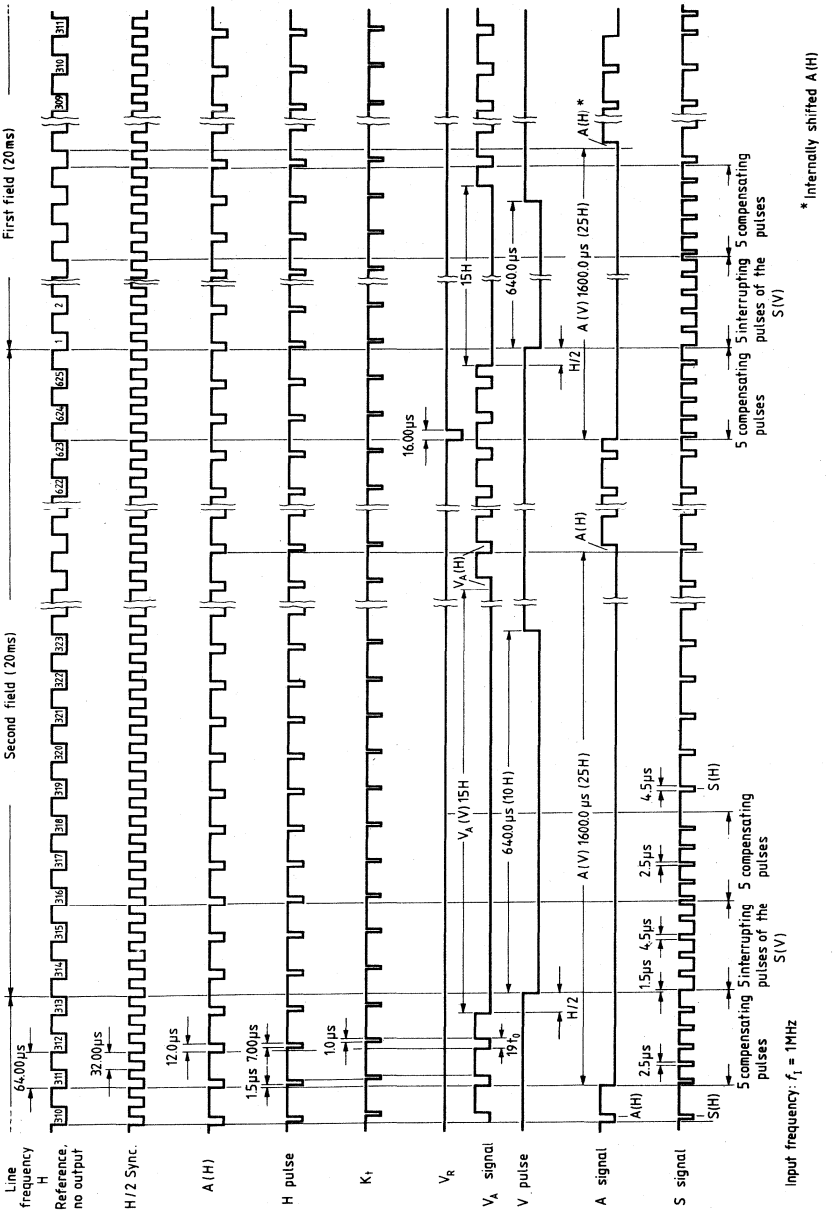
As a driver stage for the 75 Ω coaxial cable, the TTL circuit 75453 (maximum output current 300 mA; pulse delay 11 ns) is recommended.



Programming list for line number coding

Pin number	2	3	4	5	6	7	8	9	10	11	25	24	23
Line number	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	N_A	N_B	N_C
525	H	L	L	L	L	L	H	H	L	H	L	L	L
524	H	L	L	L	L	L	H	L	H	L			
625	H	L	L	H	H	H	L	L	L	H	L	L	H
624	H	L	L	H	H	L	H	H	H	L			
735	H	L	H	H	L	H	H	H	H	H	L	H	L
734	H	L	H	H	L	H	H	H	L	L			
875	H	H	L	H	H	L	H	L	H	H	L	H	H
874	H	H	L	H	H	L	H	L	L	L			
1023	H	H	H	H	H	H	H	H	H	H	H	L	L
1022	H	H	H	H	H	H	H	H	L	L			
1249	L	L	H	H	H	L	L	L	L	H	H	L	H
1248	L	L	H	H	L	H	H	H	H	L			

Pulse scheme for 625 lines



Pulse width table for the programmed line numbers

Pin No.		525 $f = 1.008$ MHz $t_0 = 0.49603\ \mu s$		625 $f = 1.000$ MHz $t_0 = 0.5\ \mu s$		735 $f = 1.4112$ MHz $t_0 = 0.3543\ \mu s$		875 $f = 1.400$ MHz $t_0 = 0.3514\ \mu s$		1023 $f = 1.96416$ MHz $t_0 = 0.25456\ \mu s$		1249 $f = 1.9984$ MHz $t_0 = 0.2502\ \mu s$	
		μs	t_0	μs	t_0	μs	t_0	μs	t_0	μs	t_0	μs	t_0
–	Line period H	63.492	128	64.00	128	45.3514	128	45.7142	128	32.583	128	32.0256	128
16	$H/_2$ synchronization	31.75	64	32.00	64	22.68	64	22.86	64	16.29	64	16.01	64
20	H pulse	6.45	13	7.0	14	4.96	14	4.99	14	2.54	10	2.5	10
26	Horizontal gating A (H)	10.91	22	12.0	24	7.08	20	8.57	24	7.13	28	6.0	24
21	Horizontal synchronization S (H)	4.46	9	4.5	9	2.83	7	2.85	7	2.54	10	2.5	10
20	Front porch	1.48	3	1.5	3	1.06	3	1.07	3	0.76	3	0.75	3
21	Equalizing pulses	2.48	5	2.5	5	1.414	4	1.42	4	1.02	4	1.00	4
21	Interruption of the V-synchronization pulse	4.46	9	4.5	9	2.48	7	2.5	7	1.78	7	1.75	7
22	Terminal pulse K_t	1.49	3	1	2	0.7	2	0.71	2	1.53	6	1.5	6
19	Vidicon gating V_A (H)	9.42	19	9.5	19	6.73	19	6.78	19	4.83	19	4.75	19
19	Vidicon gating V_A (V)	15 H +	$19t_0$	15 H +	$19t_0$	20 H +	$19t_0$	20 H +	$19t_0$	30 H +	$19t_0$	30 H +	$19t_0$
28	Vertical gating A (V)	20 H +	$22t_0$	25 H +	$24t_0$	30 H +	$20t_0$	30 H +	$24t_0$	40 H +	$28t_0$	40 H +	$24t_0$
14	V_R signal	15.87	32	16.0	32	11.34	32	11.43	32	8.15	32	8.01	32
27	V pulse	9.5 H		10 H		14.5 H		15 H		20 H		20 H	
21	Number of pre- and post equalizing pulses	6		5		6		5		6		6	

Duty cycle $f_1 = 50\% \frac{1}{f_1} = 2\ t_0$

Line programming

Any line number between 512 and 1535 lines is binary-programmable. A binary "1" is applied to the pins 2^0 to 2^9 with condition $V_{SS} \geq V_I \geq V_{SS} - 1.5$ V and a binary "0" with $V_{DD} \leq V_I \leq V_{SS} - 4.5$ V. The correct programming of the MSB 2^{10} is carried out automatically via pin 2^9 within the line number range of 512 to 1535.

Uneven line numbers (interlaced scanning method)

The binary form of the desired line number is switched to the corresponding pins.

Even line numbers

The desired line number is reduced by 1 and the binary form is switched to pins 2^0 to 2^9, the LSB (2^0) is switched invertedly.

Functional description

The principal units of the pulse generator are the horizontal and the vertical counter (see block diagram). The horizontal counter, divider ratio 64 :1, divides the input frequency down to twice the line frequency $H/_2$.

An additional logic ensures, that a defined condition of the switching stages is submitted to the counter after a maximum of one picture change. The vertical counter is externally programmable to a defined line number.

Due to the external 3-bit enconding, the desired pulse scheme is programmed internally; i.e. the appropriate switching units for realizing the H and V program, are enabled. The pulses are now fed either directly to the outside, or are logically mixed and masked in the combination logic. The pulse start or the pulse widths, respectively occur at $H/_2$ sync defined according to time. In the case of even line numbers, only the first field appears for all pulse schemes, preceded by a V_R pulse.

In the case of uneven line numbers with first and second fields (interlaced scanning), the V_R pulse precedes only the first field.

According to the CCIR standard, the first field starts, when the leading edge of the V pulse is synchronous with the leading edge of A (H).

External synchronization with $H/_2 + V_R$ or S signal

For video mixing and cross-fading, the BAS signals of the individual cameras or video recorders must be sycnrhonized, i.e. correspond in line and picture. In the case of external synchronization, these two components must be contained in the external signal: either the horizontal and vertical frequency in the case of the S signal: S (H) and S (V), or S (H), and half of the vertical frequency ($H/_2 + V_R$).

At the beginning of the leading edge, short pulses must be derived from these two H and V components, and thereby the defined setting of the horizontal and the vertical counter is accomplished.

(Standard value: H component 300 ns < clock period
V component 1 µs < $H/_2$)

Because of the time deviation of the front edges of the line frequency H and S (H), which is 1.5 periods of the input frequency, the horizontal counter would be set incorrectly. For this reason, an input S (H) has been selected for the horizontal component, which sets the counter to the correct position when activated.

The same is valid for the vertical components of $H/_2 + V_R$ and the S signal. The first frame frequency pulse follows 2.5 or 3 line periods behind the V_R pulse, depending on the scheme. The two inputs provided for the pulses from V_R or S (V), respectively, and the correspondingly encoded line scheme enable a proper setting of the vertical counter. Through the possibility of a defined setting of the counters it is ensured that a proper standard pulse scheme is obtained at the outputs even in the case of external synchronization involving different phase conditions of the synchronization signals.

Note:

At the time of setting the horizontal counter to a defined position, the phase relation of the input frequency is undefined and consequently the tolerance of the synchronization would be one clock period (i.e. ≤ 1 µs for 625 lines). By means of an external phase synchronization circuit with frequency multiplication, the input clock can be derived from the vertical component and, thereby, a defined phase relation of the reset pulse achieved relative to the input clock. Hence a common line deviation (jitter) of < 20 ns absolute value can be achieved.

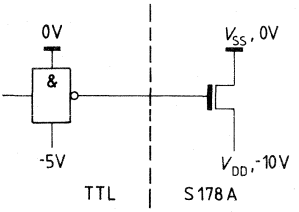
Control

The pulse generator derives the required pulses from the output frequency. As additionally half a clock period is used for the generation of the pulse widths, and as both the leading and trailing edges are used, an input duty cycle of 1 : 1 is required.

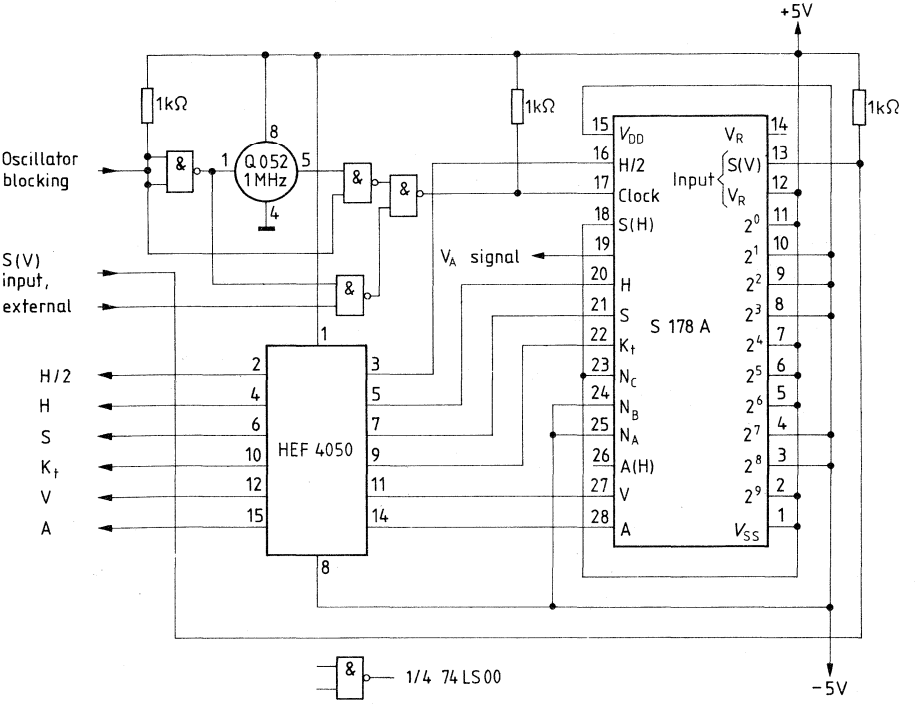
It is, therefore, recommended to operate the quartz oscillator at twice the input frequency and to divide it 2 : 1 by an external stage, thereby obtaining an accurate duty cycle of 1 : 1.

Inputs which are not used must be connected to V_{SS} (H level).

Control with TTL



A TV clock generator, externally synchronizable, using the integrated video pulse generator S 178 A.



Triple 16 Bit Up/Down Counter with 8 Bit Data Bus

S 360 B 110
S 360 B 110 C

Preliminary data

Bipolar IC

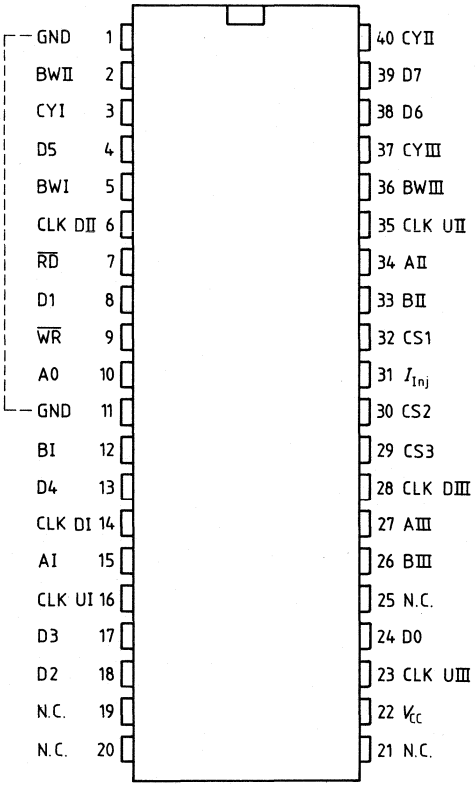
Type	Ordering code	Package	Fig. No.
S 360 B 110	Q67000-Y555-V110	DIP 40	17
S 360 B 110 C	Q67000-Y555-C110	DIC 40	18

Features

- 3 independent 16-bit up/down counters
- Counting frequency 3 MHz
- Directional decoder
- Supply voltage + 5 V
- Power dissipation 600 mW
- TTL-LS compatible

Pin configuration

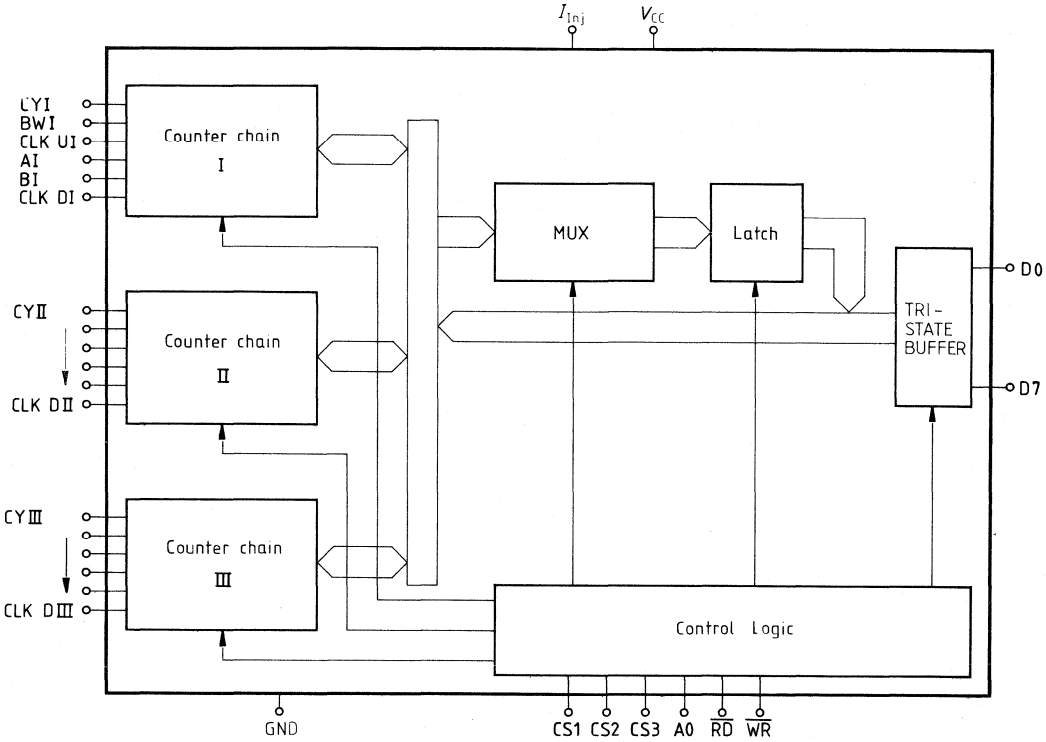
top view



Pin configuration

Symbol	Pin No.	Function
V_{CC}	22	Supply voltage
GND	1, 11	Ground 0 V
I_{inj}	31	Injector current
D 0	24	Data bus
D 1	8	
D 2	18	
D 3	17	
D 4	13	
D 5	4	
D 6	38	
D 7	39	
CLK UI	16	Clock up counter 1
CLK DI	14	Clock down counter 1
A I	15	Direction decoder input A counter 1
B I	12	Direction decoder input B counter 1
CY I	3	Carry up counter 1
BW I	5	Borrow counter 1
CLK UII	35	Clock up counter 2
CLK DII	6	Clock down counter 2
A II	34	Direction decoder input A counter 2
B II	33	Direction decoder input B counter 2
CY II	40	Carry up counter 2
BW II	2	Borrow counter 2
CLK UIII	23	Clock up counter 3
CLK DIII	28	Clock down counter 3
A III	27	Direction decoder input A counter 3
B III	26	Direction decoder input B counter 3
CY III	37	Carry up counter 3
BW III	36	Borrow counter 3
$\overline{RD}$	7	Read data bus
$\overline{WR}$	9	Write data bus
CS 1	32	Select counter 1
CS 2	30	Select counter 2
CS 3	29	Select counter 3
A 0	10	Byte select (A 0 = 1 = HB)

Block diagram



1 General component description

The S 360 B 110 LSI IC is constructed in I^2L 3 stack circuit technology and contains 1112 gates, as well as 159 transistors, 190 diodes and 388 resistors.

It therefore replaces approx. 60 TTL SSI/MSI components.

Externally, the IC is fully TTL compatible, i.e. it only requires one supply voltage (5 V). The I^2L logic, however, requires a (constant) current, that during normal operation is obtained from the supply voltage via a resistor. Voltage at pin 31 is approx. 2.7 V.

If the device also has a voltage of between 3 V and 5 V, this can also be used to generate the I^2L current, thus saving battery energy.

A series resistor is required in any case.

The value of the resistor can be calculated from the voltage difference between pin 31 and V_{batt} and the desired current. If the dynamic requirements are lower than specified, a lower current can be set (up to 40 mA). The specifications for these cases are available upon request.

2 Functional description

a) General

The component comprises three 16 bit counter chains operating independently.

Each counter chain is made up of four 4-bit counter components that are logically equivalent to the TTL MSI component 74193. This arrangement then results in a 16 bit up/down counter with a maximum count of $2^{16}-1 = 65{,}535$ (decimal) per chain. The counting process can use either the directional decoder inputs A and B or the direct count inputs CLKU, CLKD. Carry and borrow outputs CY, BW are routed out from each chain. The respective counter chain can be activated via the "chip select" inputs (CS 1, CS 2, CS 3, active H). If all CS inputs are L, data outputs D 0 to D 7 are switched to a high impedance state.

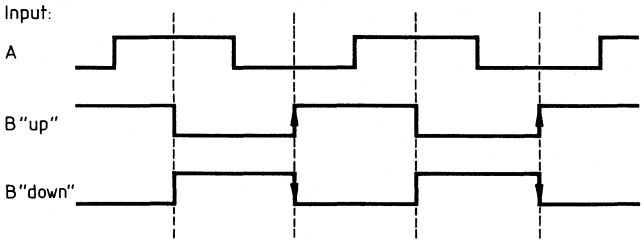
Address input A 0 serves to switch the bidirectional data connections to the low byte (LB, bits 0 to 7), or to the high byte (HB, bits 8 to 15) respectively.

Input "write" ($\overline{WR}$, active L) enables the setting of the counter chain, or the counter chains respectively.

In order to read the active counter chain, the "read" input ($\overline{RD}$, active L) must be switched to L. If $\overline{RD}$ is H, the data outputs are disabled.

b) **Direction decoder (inputs A, B)**

If a signal is routed to inputs A–B, that is phase-shifted by 90° (e.g. from two light barriers), this can be used to determine the direction of rotation, or the direction of counting respectively.



Signal A disables only the first edge of signal B. If the hole of the light barrier B comes from the right, only rising edges (L–H) are produced, if it comes from the left, only falling edges are produced (H–L).

The pulse edge is differentiated via a delay circuit, so that "up" and "down" produces different pulses. For both up as well as down pulses, this circuit becomes active at the same edge, thus eliminating the 1/2 bit error inherent in conventional solutions. All AB inputs are designed as Schmitt triggers to increase the resistance to interference.

c) **Direct count inputs** (CLKU, CLKD)

The direct count inputs are ANDed to the directional decoder inputs, so that the respective unused inputs must always have H level.

These CLKU, CLKD inputs directly affect the counters. In this manner, e.g. in conjunction with the carry and borrow outputs CY, BW, several counter chains, or several components can be cascaded.

d) **Setting the counters**

In order to set the counters, the following logical conditions must be met:

set LB:			set HB:		
	A0	= L		A0	= H
	$\overline{RD}$	= H		$\overline{RD}$	= H
	$\overline{WR}$	= L		$\overline{WR}$	= L
	CS	= H		CS	= H

CS = CS1, CS2, CS3; 2 or all 3 chains can be set simultaneously.

Reading the count

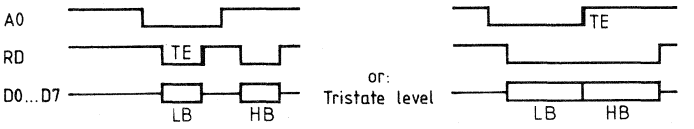
In principle, the following logical conditions must be met in order to read the counters:

read LB:			read HB:		
	A0	= L		A0	= H
	$\overline{RD}$	= L		$\overline{RD}$	= L
	$\overline{WR}$	= H		$\overline{WR}$	= H
	CS	= H		CS	= H

CS = CS1 or CS2 or CS3

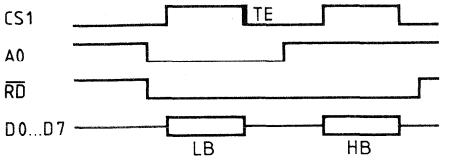
In position A0 = L, the LB is directly switched to outputs D0 to D7. The HB is buffered via edge triggered flip flops. The flip flops thus store data during each pos. edge of inputs A0 and $\overline{RD}$, or during the neg. edge of the CS inputs (chip select) respectively.

This condition for the trigger edge (TE) at the flip flops is RD · CS · $\overline{A0}$ (CS = CS1 + CS2 + CS3). This results in the following possible pulse diagrams for reading LB and HB:



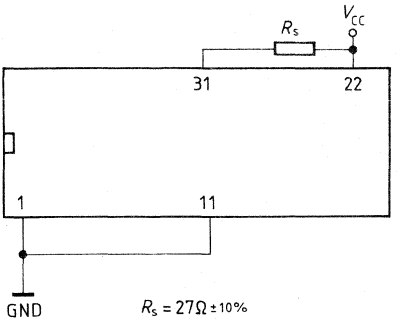
(CS1 e.g. static H, CS2 and CS3 L)

or via CS (if all CS inputs are L, the D outputs are switched to a high impedance state):



Characteristics $T_{amb} = 0$ °C to 70 °C		Test conditions	min	typ	max	
Power supply						
Supply voltage (pin 22)	V_{CC}		4.75		5.25	V
Supply current (pin 22)	I_{CC}	$V_{CC} = 5$ V Connection plan A for power supply		32		mA
Injector current (pin 31)	I_{INJ}			85		mA
Injector voltage (pin 31)	V_{INJ}			2.7		V
Power dissipation						
$I_{CC} \times V_{CC}$ (level converter)	P_{DCC}	$V_{CC} = 5.0$ V		160		mW
$+ I_I \times V_{CC}$ (I^2L logic)	P_{DI}	Connection plan A for power supply		425		mW
Total power dissipation	P_{Dtot}	Including P_D at the series resistor		585		mW
H output current	I_{QH}				−400	µA
L output current	I_{QL}				8	mA
H input voltage	V_{IH}		2			V
L input voltage A-B inputs (Schmitt trigger)	V_{IL1}				0.7	V
L input voltage remaining inputs	V_{IL2}				0.8	V
Input terminal voltage	V_{IK}	$V_{CC} = 4.75$ V, $I_I = 18$ mA			−2	V
H output voltage	V_{QH}	$V_{CC} = 4.75$ V, $I_{QH} = -400$ µA	2.4	3.3		V
L output voltage	V_{QL}	$V_{CC} = 4.75$ V, $I_{QL} = 4$ mA			0.4	V
Input current at max. voltage	I_I	$V_{CC} = 5.25$ V, $V_I = 5.25$ V			0.1	mA
H input current	I_{IH}	$V_{CC} = 5.25$ V, $V_{IH} = 2.7$ V			20	µA
L input current	I_{IL}	$V_{CC} = 5.25$ V, $V_{IL} = 0.4$ V			0.5	mA
Short-circuit output current	I_{QSC}	$V_{CC} = 5.25$ V	−20		−50	mA

Connection plan A for power supply

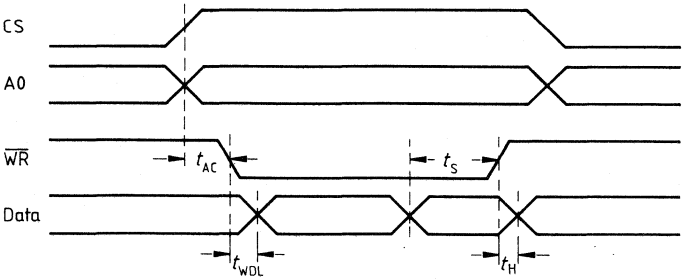


$V_{CC} = +5$ V; $T_{amb} = 25$ °C

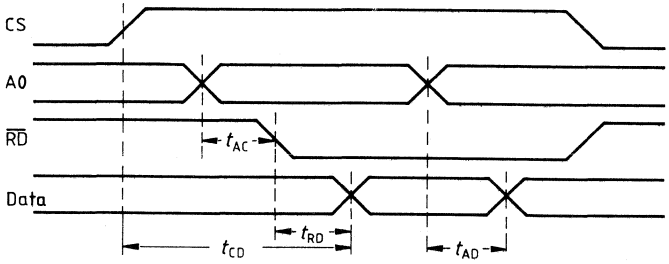
Symbol	Description	min	typ	max	unit
t_{CC}	Pulse width $\overline{RD}$, $\overline{WR}$, A 0, CS, CLK U, CLK D	150	200		ns
t_{AB}	Pulse width A, B	200	250		ns
t_{CD}	Delay time from CS = H until data is pending at the bus		250	300	ns
t_{AD}	Delay time from A 0 (H, L) until data is pending at the bus		180	200	ns
t_{AC}	Valid address before arrival of the $\overline{RD}/\overline{WR}$ signal	80	100		ns
t_{WDL}	Delay time from $\overline{WR}$ = L until data is valid		20	40	ns
t_S	Data set-up time	100	150		ns
t_H	Data hold time	−20	0		ns
t_{RD}	Delay time after $\overline{RD}$ = L until count is pending at the bus		80	100	ns
t_{TD}	Delay time from pos. clock edge (CLK U, CLK D) until data is pending at the bus		420	450	ns
t_{ABD}	Delay time from **pos.** clock edge B (count upwards) until data is pending at the bus		600	650	ns
t_{BAD}	Delay time from **neg.** clock edge B (count down) until data is pending at the bus		600	650	ns
t_P	Phase difference between A, B, up to which the count direction is still recognized	100	120		ns

Phase diagram

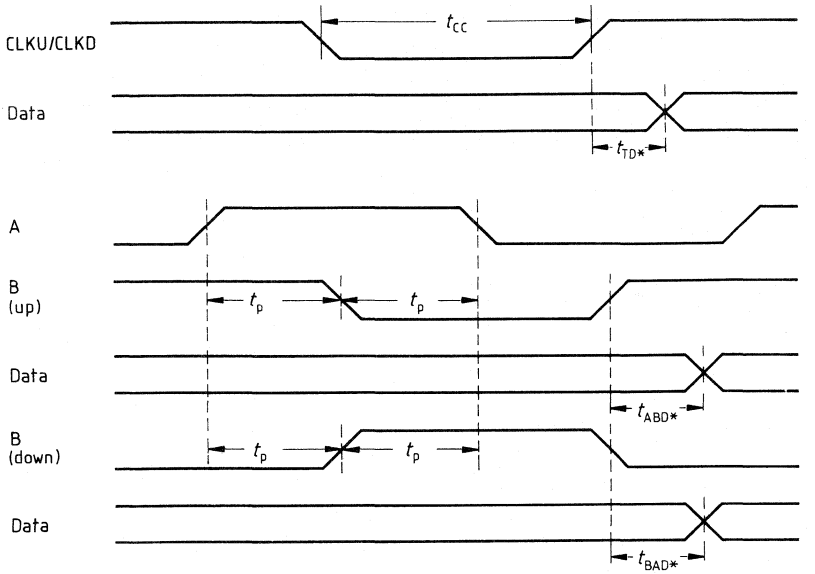
1 Setting the counter



2 Reading the counter



3 Counting



* after t_{ABD}, t_{BAD}, t_{TD} all outputs are valid

Universal Programmable Counter with Signal Edge Evaluation Circuit

S 360 B 114

Preliminary data **Bipolar IC**

Type	Ordering code	Package	Fig. No.
S 360 B 114	Q67000-Y555-V114	DIP 28 LS-TTL compatible inputs and outputs	16

General

The IC S 360 B 114 contains two independent, internally cascadable 16-bit counters, quad/double/single clock selection circuits, directional discriminators, hysteresis circuits, a 32-bit latch, as well as function and control logic.

The operating mode of the circuit is adjusted via a microprocessor with 8-bit data bus, 3-bit address bus, as well as µP control lines.

Technology

Standard, bipolar, low-loss I^2L circuit technology

Functional description

- Quad/double/single clock selection for two phase-shifted cycles; further processing in 32-bit loadable up/down counter (or a 16-bit counter each)
- Direction recognition for up/down counting
- Hysteresis circuit for suppression of 1st pulse after a reversal of rotation – disconnectable
- 32-bit data latch – strobe latch synchronized with counter clock
- 8-bit parallel data I/O via tristate bus
- Operating mode definition by internal code register loadable via data bus
- External clear and strobe possibility
- Interrupt indication after external strobe
- Pulse width and frequency measurement via direct inputs, up/down counting settable

Typical applications

- X, Y, Z controls
- Electronic "mouse"
- Electronic slide gauge
- Scales
- Pulse width and frequency measurements

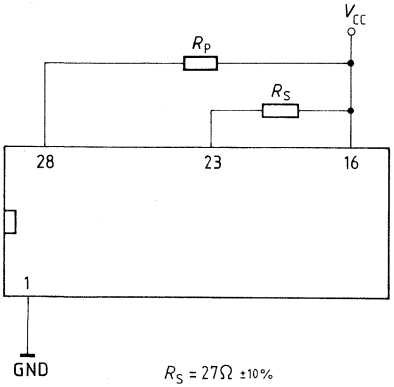
Maximum frequencies

CLK input	max.	3	MHz
A, B, C, D inputs in quad/double/single mode	max.	750	kHz
A, C inputs in direct mode	max.	3	MHz
Demands on microprocessor:			
data access time		300	ns
data hold time		40	ns

Power dissipation

at maximum frequency	approx.	400	mW
at low frequency requirements (1 to 1.5 MHz)	approx.	250	mW

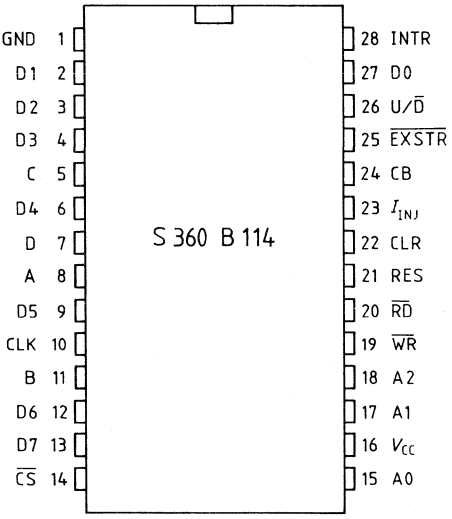
Connection plan for power supply



$R_S = 27\Omega \pm 10\%$
$R_P \geq 1.2\,k\Omega$

Pin configuration

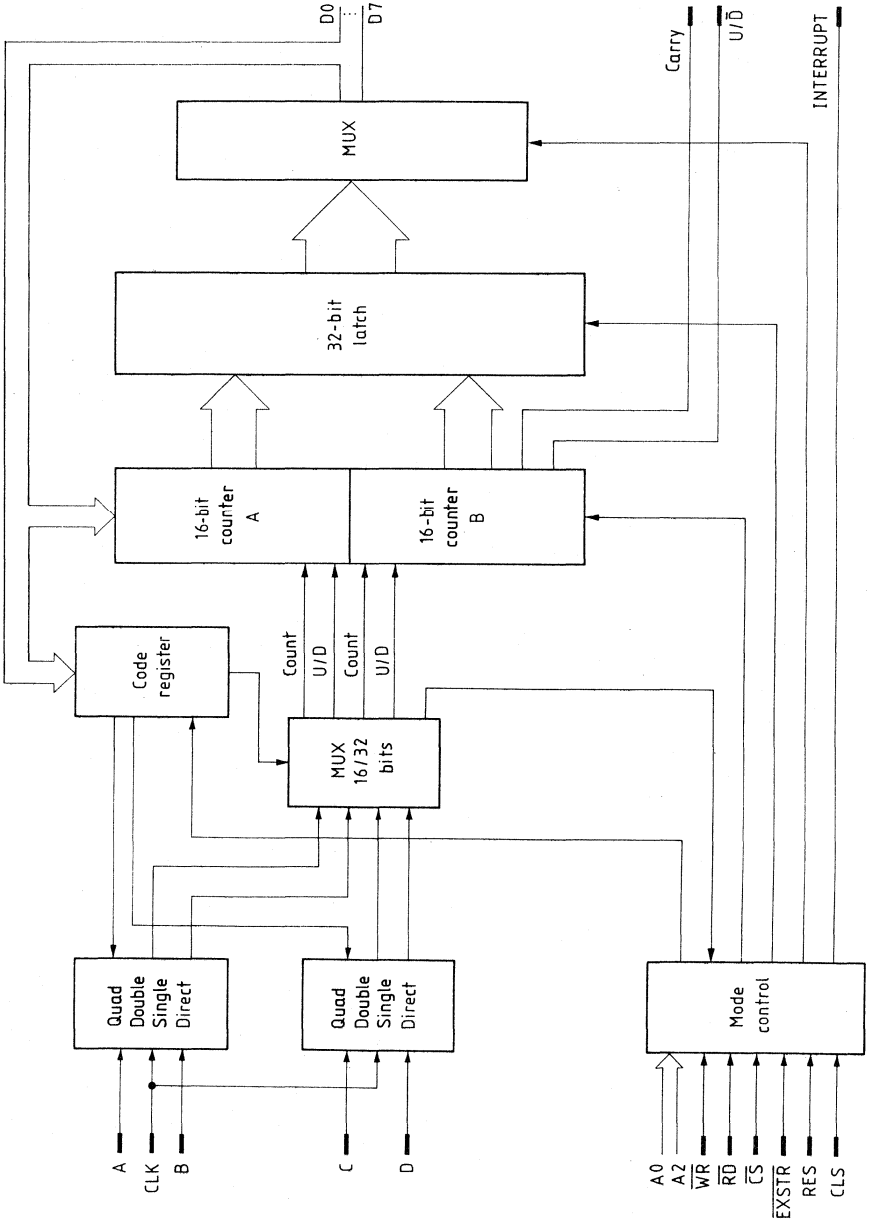
top view



Pin configuration

Pin No.	Symbol	Function
1	GND	Ground
27, 2, 3, 4, 6, 9, 12, 13	D 0 to D 7	Data bus
5	C	Signal input counter B
7	D	Signal input counter B
8	A	Signal input counter A
10	CLK	Strobe for quad/double/single clock selection circuits. Frequency must correspond to at least 4 times the frequency of signals at A, B, C or D. In direct mode, the CLK input is to be applied to L.
11	B	Signal input counter A
14	$\overline{CS}$	CHIP SELECT
15, 17, 18	A 0, A 1, A 2	ADDRESS BUS
16	V_{CC}	Supply voltage
19	$\overline{WR}$	WRITE ENABLE
20	$\overline{RD}$	READ ENABLE
21	RES	Sets the control logic to initial state.
22	CLR	Sets the 32-bit counter to 0.
23	I_{INJ}	Injector current
24	CB	CARRY, BORROW over 32 bits (32-bit mode) over 16 bits (16-bit mode)
25	$\overline{EXSTR}$	EXTERNAL STROBE enables an independent latch instruction and sets the INTERRUPT FLAG.
26	U/$\overline{D}$	UP/$\overline{DOWN}$ from quad/double/single clock selection circuit A (32-bit mode)
28	INTR	INTERRUPT (open collector output)

Block diagram



Maximum ratings

Supply voltage	V_{CC}	7.0	V
Injector current	I_{INJ}	300	mA
Input voltage	V_I	−0.5 to 5.5	V
Differential voltage between inputs	V_{ID}	5.5	V
Storage temperature range	T_{stg}	−55 to 125	°C
Ambient temperature range	T_{amb}	0 to 70	°C

Operating range

		min	typ	max	
Supply voltage	V_{CC}	4.75	5	5.25	V
Injector current[1]	I_{INJ}			120	mA
L output current	I_{QL}			4	mA
Ambient temperature	T_{amb}	0		70	°C

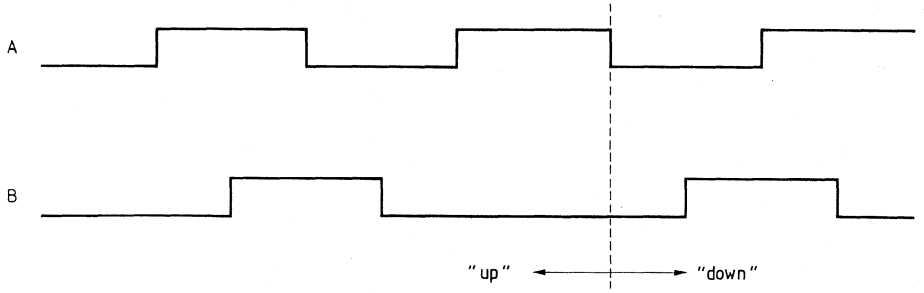
Characteristics

		Test conditions	min	typ	max	
H input voltage	V_{IH}		2			V
L input voltage	V_{IL}				0.8	V
Input terminal voltage	V_{IK}	V_{CC} = typ., I_I = −18 mA	−0.5		−1.5	V
H output voltage	V_{QH}	V_{CC} = min., I_{QH} = 0.4 mA	2.7	3.3		V
L output voltage	V_{QL}	V_{CC} = min., I_{QL} = 8 mA		0.35	0.55	V
L output voltage	V_{QL}	V_{CC} = max., I_{QL} = 8 mA		0.35	0.55	V
H input current[4]	I_{IH}	V_{CC} = max., V_{IH} = 2.7 V			0.02	mA
H input current[2]	I_{IH}	V_{CC} = max., V_{IH} = 2.7 V			0.06	mA
Input current at max. input voltage[2]	$I_{(BR)}$	V_{CC} = max., V_{IH} = 5.5 V			0.1	mA
L input current[2]	I_{IL}	V_{CC} = max., V_{IL} = 0.4 V	−0.4		0.4	mA
Short-circuit output current[3]	I_{QS}	V_{CC} = min., V_{QH} = 0.2 V	−15		−100	mA
Short-circuit output current[3]	I_{QS}	V_{CC} = max., V_{QH} = 0.2 V	−22		−100	mA
Output leakage current	I_{QIk}	V_{CC} = max., V_{QH} = 5.25 V			0.1	mA
Output tristate current	I_{ZH}	V_{CC} = max., V_{QH} = 5.25 V	−0.04		0.06	mA
Negative output current[4]	$I_{0\,neg}$	V_{CC} = max., V_{QL} = −0.5 V			−8	mA

1) only in conjunction with a series resistor
2) bidirectional pins in high-impedance state
3) not for "open-collector" pins
4) not for bidirectional pins

Signal description

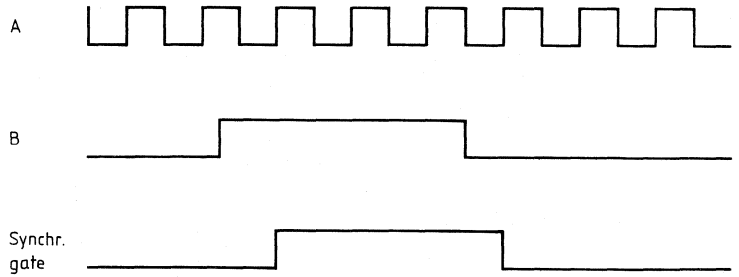
A, B Inputs for phase-shifted signals in case of quad/double/single mode
32-bit counter as well as 16-bit counter
Signal change A prior to signal change B indicates up-counting



In direct mode: A = clock input
B = gate

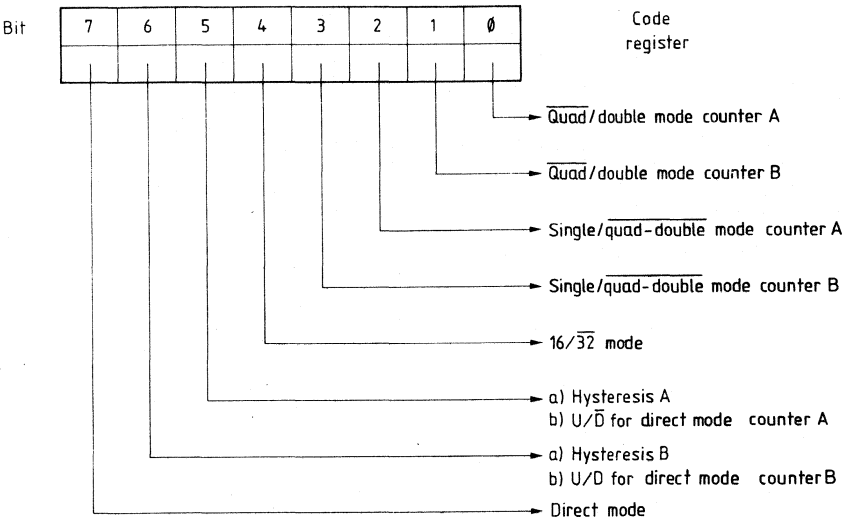
The gate input is synchronized by the clock.

C, D Same as A, B, however, with phase-shifted signal inputs for 16-bit counter B.



In direct mode: C = clock input
B = gate

Code register address (05) (write only)



Addressing

CS	A 2	A 1	A 0	Read RD WR	Write WR RD
0	0	0	0	Status register	Strobe instruction (processor)
0	0	0	1	Byte 0	Byte 0
0	0	1	0	Byte 1	Byte 1
0	0	1	1	Byte 2	Byte 2
0	1	0	0	Byte 3	Byte 3
0	1	0	1	–	Code register
0	1	1	0	inactive	inactive
0	1	1	1	inactive	inactive
1	x	x	x	inactive	inactive

16/32-bit mode is set by data bit D 4

L at D 4 32-bit mode
H at D 4 16-bit mode

In the 32-bit mode, either the quad/double/single clock selection circuit A or the direct mode is used. CB is the CARRY/BORROW output via 32 bits.

The up/$\overline{\text{down}}$ signal recognized in the clock selection circuit A is available at U/$\overline{\text{D}}$.

In the 16-bit mode, either the quad/double/single clock selection circuit A for counter A and the quad/double/single clock selection circuit B for counter B, or the direct mode (inputs A, B for counter A; inputs C, D for counter B) is used.

CB is the CARRY/BORROW output via 16-bit counter B. The up/down signal recognized in the clock selection is available at U/D.

Quad mode

In quad mode, the clock selection circuit generates a counting pulse from each edge of two phase-shifted signals. These signals must be applied to inputs A and B in the 32-bit mode. In the 16-bit mode, a second clock selection circuit is available for inputs C and D.

The signals A, B and C, D are strobed by the common clock CLK, and stored temporarily. That clock must have at least 4 times the frequency of signals A, B, C, D.

The clock selection circuits recognize the counting direction for the 16/32-bit counter from the phase shift of signal A to signal B or C to D, respectively.

Double mode

Function as in quad mode, however, only two of the four signal edges per period are evaluated.

Single mode

Function as in quad mode, however, only one of the four signal edges per period is evaluated.

Hysteresis

A hysteresis circuit is available in each of the quad/double/single clock selection circuits. It processes each time the first counting pulse after a reversal of rotation.

Direct mode

The two quad/double/single clock selection circuits turn inactive in the direct mode.

Each of the inputs A, B in 32-bit mode or A, B and C, D in 16-bit mode represents a clock gate circuit. Thus, frequency as well as pulse width measurements can be carried out. The CLK input is, therefore, to be applied to L. The 32-bit counter as well as both 16-bit counters can independently be set to up/down counting by bit D5 or bit D6 of the code register.

RESET

The control logic of the circuit is set to its initial state by setting the RES input to H; this requires a 32-bit counter, a quad/double/single signal edge evaluation circuit (controlled by A, B, and CLK) in quad mode. Hysteresis, direct mode, and the second quad/double/single signal edge evaluation circuit are not active.

By setting the CLR input to H, the 32-bit counter will asynchronously be set to L (0).

Loading

Counter

The 16/32-bit counter can be loaded via the 8-bit data bus.

The byte selection is achieved via address bus A0 to A2; $\overline{CS}$ and $\overline{WR}$ permit the loading procedure.

Latching

Transmission of the counter states of the latch is performed 32-bit, parallel, either via the external strobe input $\overline{EST}$, or by a µP write instruction to address 0 (A0 to A2, $\overline{CS}$, $\overline{WR}$).

The strobe signal is internally synchronized with counting pulses possibly occurring at the same time, so that no intermediate states are latched.

Output INTR (interrupt flag) is set by an external strobe signal.

Reading

Latch

The 32-bit latch is read via the 8-bit data bus. Byte selection is achieved via address bus A0 to A2; $\overline{CS}$ and $\overline{RD}$ permit read operation.

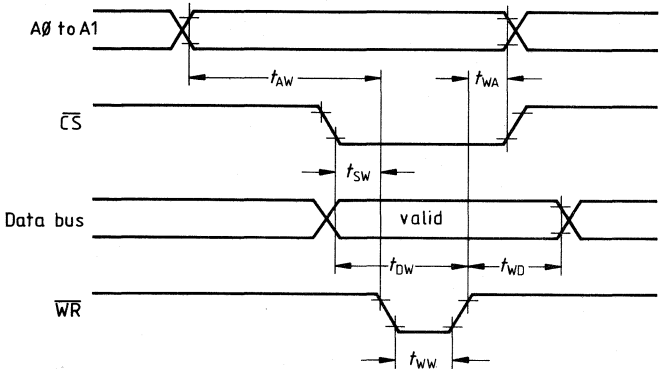
Status register

The status register is set by an external strobe signal (H at INTR).

The register can be read via address 0 within one read cycle.

Writing (load, strobe)

Loading of counter or code register is carried out by a μP write cycle on the 8-bit data bus.



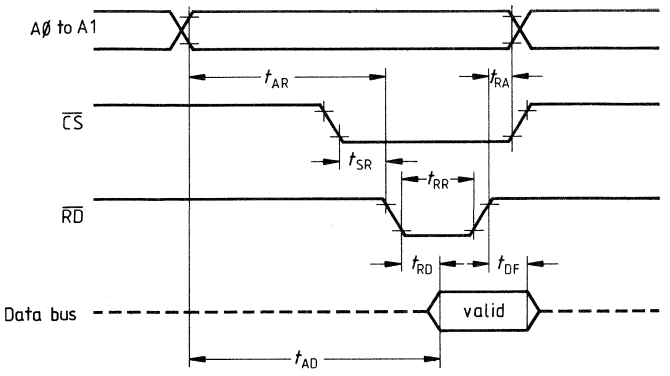
Switching times

T_{amb} = 0 °C to 70 °C; V_{CC} = 5 V ± 10%; V_{SS} = 0 V; V_{QH} = 2.0 V; V_{QL} = 0.8 V

Write cycle		min	
Address stable before $\overline{WR}$ ↓	t_{AW}	100	ns
$\overline{CS}$ stable before $\overline{WR}$ ↓	t_{SW}	100	ns
Address hold time $\overline{WR}$ ↑	t_{WA}	50	ns
$\overline{WR}$ pulse width	t_{WW}	200	ns
Data setup time before $\overline{WR}$ ↑	t_{DW}	200	ns
Data hold time after $\overline{WR}$ ↑	t_{WD}	50	ns
Instruction recovery time	t_{RV}	300	ns

Reading

Reading data from latch or status register is carried out by a μP read cycle on the 8-bit data bus.

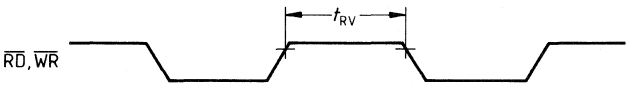


Switching times

T_{amb} = 0 °C to 70 °C; V_{CC} = 5 V ± 10%; V_{SS} = 0 V; V_{QH} = 2.0 V; V_{QL} = 0.8 V

Read cycle		min	max	
Address stable before $\overline{RD}$ ↓	t_{AR}	100	—	ns
$\overline{CS}$ stable before $\overline{RD}$ ↓	t_{SR}	100	—	ns
Address hold time after $\overline{RD}$ ↑	t_{RA}	50	—	ns
$\overline{RD}$ pulse width	t_{RR}	200	—	ns
Data delay of $\overline{RD}$ ↓	t_{RD}	—	200	ns
Data delay of address	t_{AD}	—	300	ns
$\overline{RD}$ ↑ to data in tristate	t_{DF}	—	100	ns
Instruction recovery time	t_{RV}	300	—	ns

Recovery time



Reset

The minimum pulse width for CLR (counter clear) is 20 ns, for RES (logic reset) 500 ns.

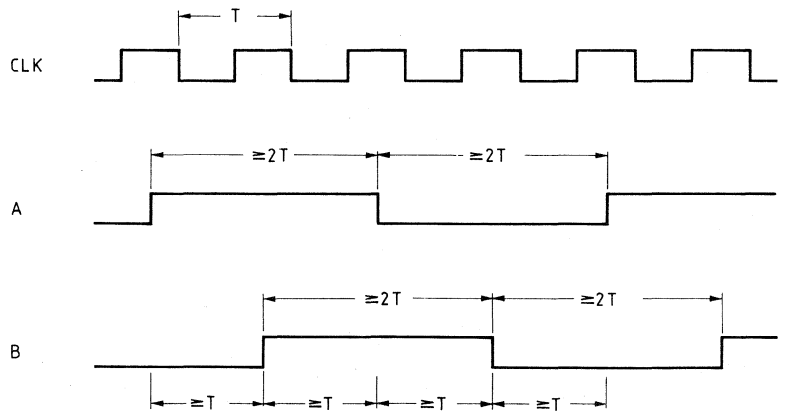
Signal specification

Clock

The maximum clock frequency is 3 MHz.

A, B, C, D

The signal edge evaluation circuit requires at least one cycle for signal evaluation or direction recognition.



The figure above shows, that not a phase shifting between signals A, B, and C, D is required, but a keeping of the minimum times which are referred to system clock. This results in a maximum frequency of 750 kHz for signals A, B, C, and D when using the signal edge evaluation circuit. In direct mode, the maximum clock frequency for inputs A and C is 3 MHz.

AF Amplifier for 1 V

S 1531 G

Preliminary data **Bipolar IC**

Type	Ordering code	Package	Color code	Fig. No.
S 1531 G	Q67000-A2063	similar to SO 8	orange/green	26

Functional description

The AF amplifier was designed for small operating voltages. It is, therefore, specially suited for use in battery-operated equipment.

The open collector outputs can be used to drive center-tapped speakers.

Circuit description

An unsymmetrically driven differential amplifier with negative feedback to achieve 20 dB voltage gain, is followed by a second differential amplifier that determines the upper cut-off frequency by means of integrated low-pass filters.

Current-controlled booster amplifiers with high current gain are connected to the antiphase outputs of this differential amplifier.

A negative feedback branch to the input of the second differential amplifiers sets the total gain of the circuit to 40 dB $\pm$ 3 dB.

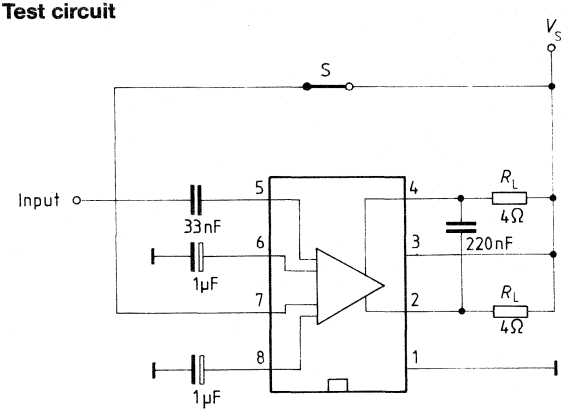
Additional circuitry prevents saturation of the prestage transistors, thereby achieving maximum output power at low harmonic distortion.

A regulating loop serves to make the quiescent current of the output transistors independent of temperature.

The amplifier can be switched on by a muting voltage; with no muting voltage, the amplifier is switched off, except for quiescent currents of some μA.

Maximum ratings		Test conditions	Test circuit	Lower limit B	typ	Upper limit A	
Supply voltage	V_S			−0.3		2.0	V
Peak output current	I_Q					250	mA
Muting input voltage	V_M					V_S	V
Junction temperature	T_j					125	°C
Storage temperature	T_{stg}			−40		125	°C
Ambient temperature	T_{amb}			−20		60	°C
Thermal resistance (system-air)	$R_{th\,SA}$					200	K/W
Operating range							
Supply voltage	V_S			1		1.7	V
Characteristics							
$V_S = 1.2$ V; $T_{amb} = -10$ °C to 40 °C							
Quiescent current	I_S	$V_M = V_S$	1		5	20	mA
	I_S	$V_M = 0$	1			20	µA
Output power	P_Q	$f = 1$ kHz, $THD = 10\%$, $R_L = 4\ \Omega$	1		120		mW
Voltage gain	G_V	$T_{amb} = 25$ °C	1	37	40	43	dB
	G_V		1	35	40	45	dB
Cut-off frequency	f_l	−3 dB	1	200			Hz
	f_u		1	5			kHz
Input resistance	R_I		1	30	50		kΩ
Saturation voltage	$V_{CE\,sat}$	$I_Q = 225$ mA	1		300		mV
Muting control current							
enabled	I_M			50			µA
disabled	I_M					5	µA
Signal-to-noise ratio	S/N	$P_Q = 50$ mW, $R_L = 4\ \Omega$	1		50		dB
Current consumption	I_S	$P_Q = 80$ mW, $R_L = 4\ \Omega$	1		140		mA
Efficiency	η	$P_Q = 80$ mW, $R_L = 4\ \Omega$	1		48		%
Total harmonic distortion	THD	$f = 0.2$ to 5 kHz, $P_Q = 80$ mW	1		5		%
Total harmonic distortion	THD	$f = 0.5$ to 2 kHz, $P_Q = 80$ mW	2		1.5		%

Test circuit



S closed : amplifier enabled
S open : amplifier disabled

Figure 1

Application circuit

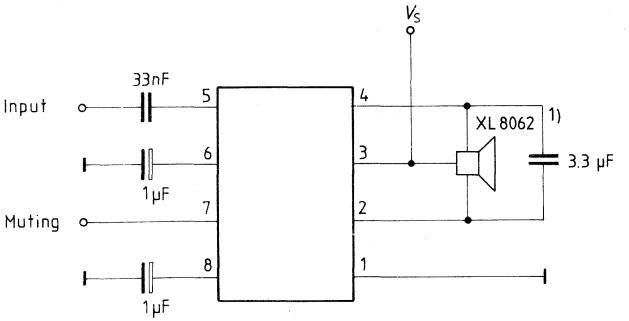


Figure 2

1) Designation of Messrs. Knowtes, USA.

MOS IC

Type	Ordering code	Package	Fig. No.
SLE 43215 P/SH 100	Q67120-C154	DIP 40	17

Brief description[1)]

The SLE 43215 P/SH 100 MOS integrated circuit is a combination of the SLE 43215 single-chip microcomputer and a special SH 100 ROM program to form a heating controller that is governed by the time of day and weather conditions.

Controllers of this kind are widely used to save energy in the heating installations of buildings. They control the temperature of the hot water that is circulated, this being performed as a function of changing outdoor temperatures to produce an indoor temperature that is very constant.

Furthermore, the heating energy is fed according to the individual times of use of a building, i.e. the supply temperature is reduced from the normal heating level by a timing program.

Conventional, temperature-dependent analog heating controllers with an automatic timer that is programmed on a daily or weekly basis control the temperature of the hot water that is circulated or the boiler temperature of a central-heating installation as a function of outdoor temperature and the time of day. They can produce savings in heating costs of as much as 20%.

The relationship between outdoor temperature and the temperature of the circulated hot water is given by what is called a heating characteristic. This can be set on the heating controller and the user or fitter of the heating system will adjust it according to the technically based heating requirements of a building. If this heating curve is properly set, the indoor temperature will remain constant despite fluctuations in outdoor temperature.

Through the use of the SLE 43215 P/SH 100 microcomputer heating controllers can be markedly improved in point of:

- An accurate control algorithm
- Self-monotoring
- An attractive price/performance ratio
- Enhanced ease of use

1) An application note (ordering No. B/3080-101) describes hardware and software of a complete controller as well as its operation.
Technical data on the SLE 43215 P/SH 100 can be obtained from the data sheet of the SAB 80215/SLE 43215 (ordering No. B/2509-101).

Functions of the heating controller

Combination with the program of the SLE 43215 P/SH 100 produces a heating-controller circuit with the following features:

- programmed temperature reduction over a period of seven days
- two reduction periods daily
- setting of the slope of the heating characteristic
- setting of indoor temperature through a parallel shift of the heating curve
- setting of the reduction temperature
- automatic timing
- protection of the timer (day/hrs/mins) and all input data against power failure for up to six hours
- device for measuring and indicating two temperature values with accuracy of at least ± 2 K (standard DIN 32729)
- monitoring of the sensors for line breaks and shorts (alarm signal, self-protection)
- control with adjustable integration response
- simple and safe operation
- requirement-based pump control

Features of the SLE 43215 P/SH 100

The SLE 43215 P/SH 100 comprises a complete, standard 8-bit μC and various peripheral circuits on a single chip. The core of the computer corresponds to the SAB 8021, but with 2 Kbytes of ROM and 128 bytes of RAM.

The periphery integrated into the chip and which is of particular importance for the heating controller, primarily consists of the following:

- 8-bit A/D converter with three multiplexed inputs
- timer
- multiplexed interface for 20 input functions, e.g. keys
- multiplexed interface for 40 input functions, e.g. four 7-segment and 12 LED displays
- standby supply of 5 mA for RAM, timer, and other functions
- timer/counter for 4, 8 and 12 bits

SLE 43215, interfacing with periphery

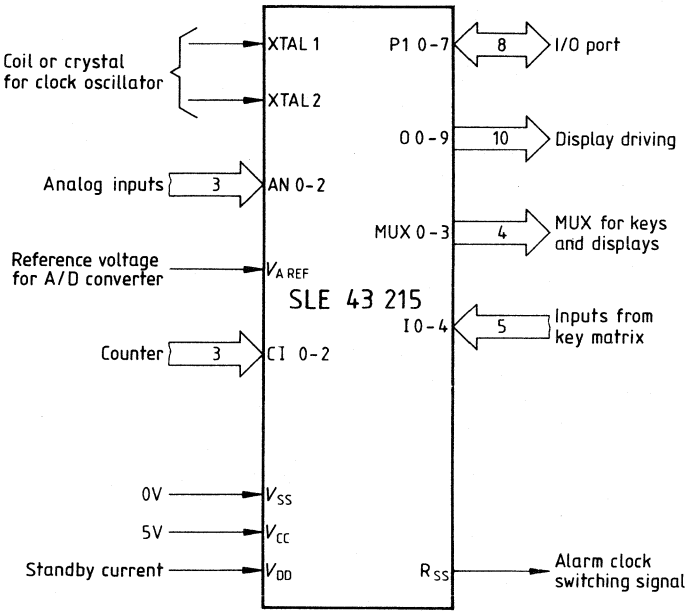
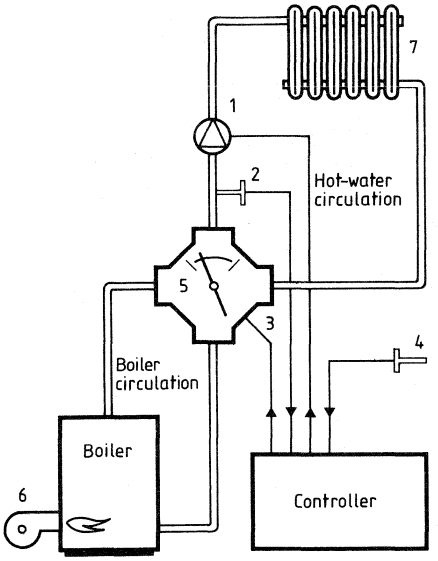


Figure 1

Schematic diagram of the lines of action of the controller in an oil heating system



1 Pump
2 Circulation sensor
3 Mixer motor
4 Outdoor-temperature sensor
5 Mixer valve
6 Burner
7 Radiator

Figure 2

Monovalent heating controller with SLE 43215 P/SH 100 (block diagram)

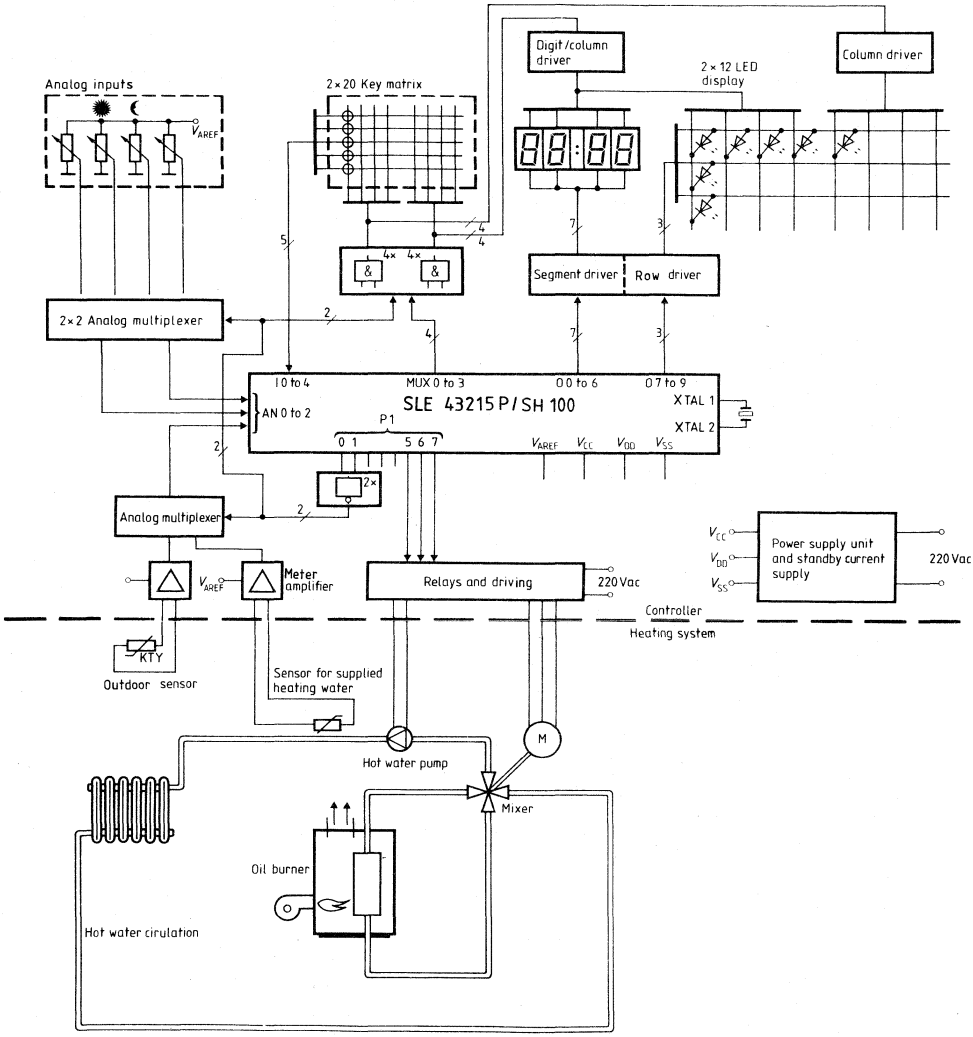


Figure 3

Figure 4 shows an example of a weekly program in schematic form. On each day of the week two normal heating phases are provided for. Between two normal heating phases there is a reduction phase during which the circulation temperature is reduced to save energy. The timing program consists of a sequence of stored switching points, set in increments of 10 min, at which the circulation temperature is increased or reduced. The programming of a complete week's program therefore calls for the entry of 4 x 7 = 28 switching points.

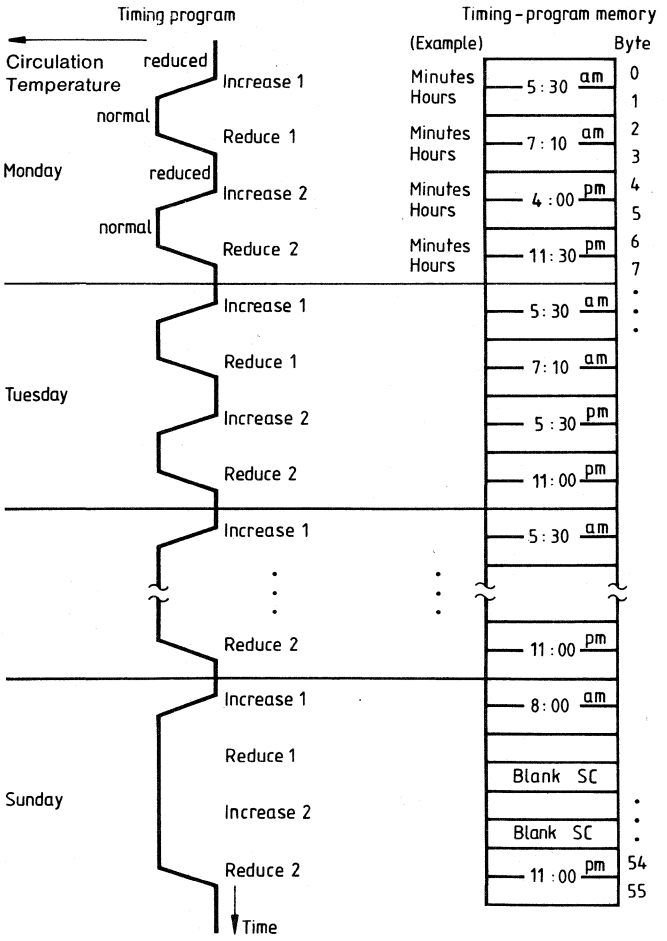


Figure 4

Description of the program structure (outline)

Program flowchart of the heating-controller software

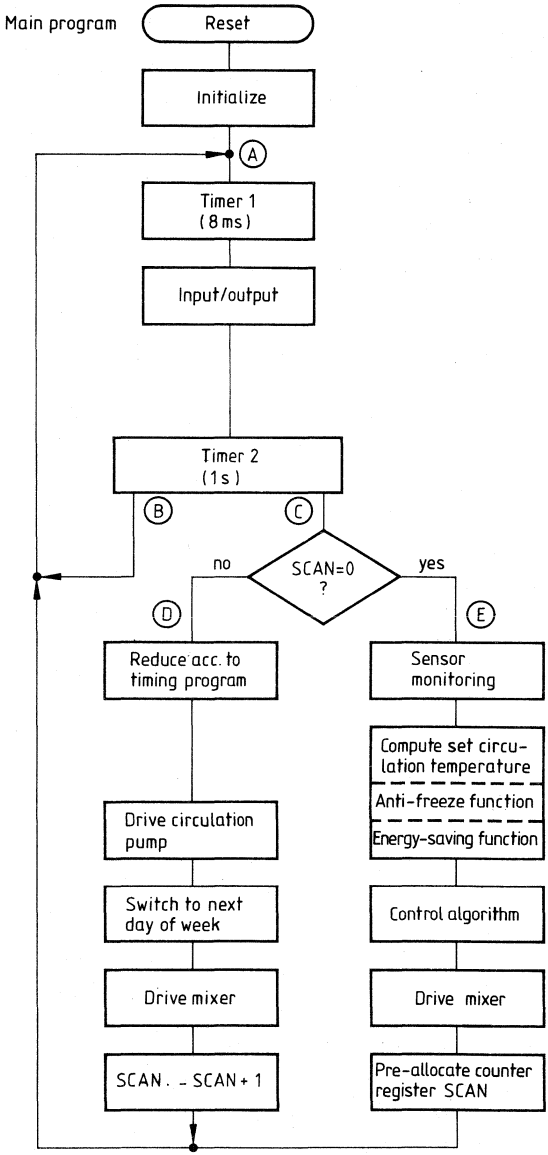


Figure 5

Schematic diagram of the control panel of the heating controller

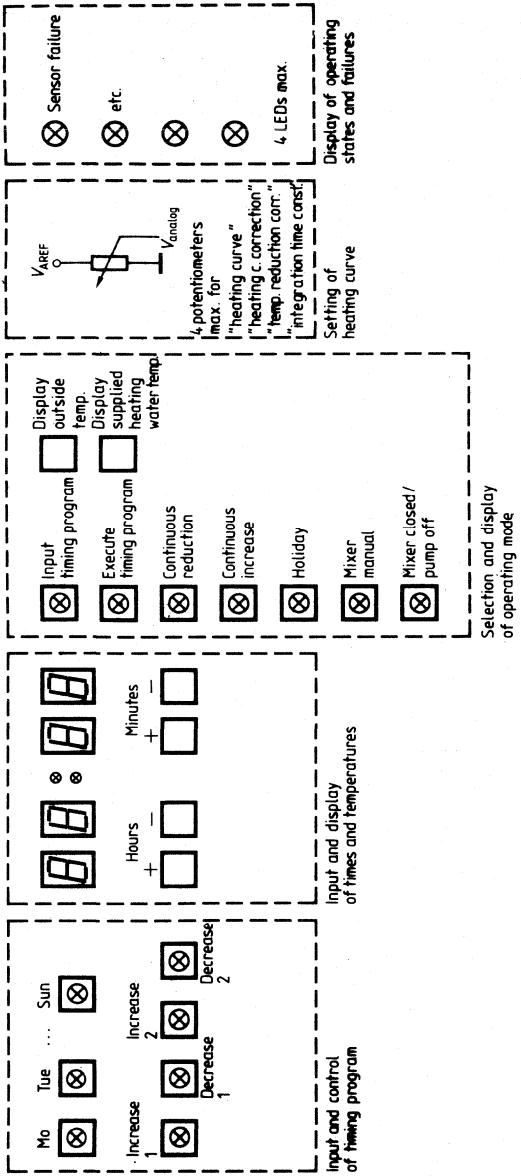
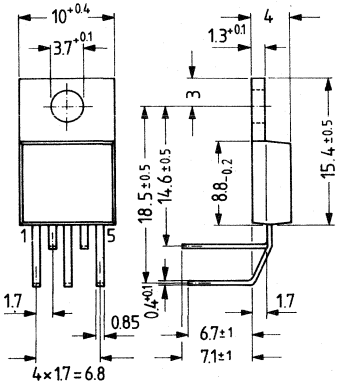


Figure 6

Package Outlines

Package Outlines

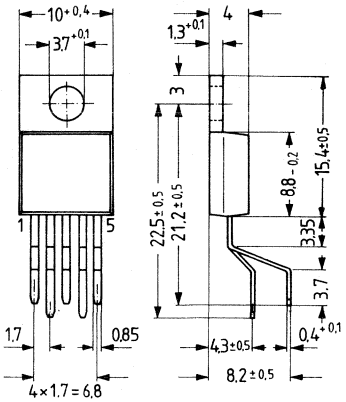
Plastic power package, similar to TO-220
(with cooling strip and 5 pins)



Approx. weight 2.1 g

Figure 1

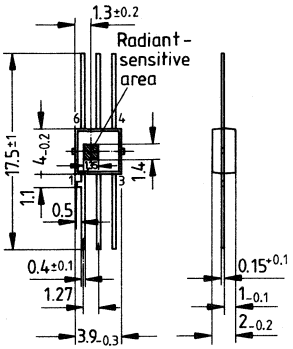
Plastic power package, similar to TO-220
(with cooling strip and 5 pins)



Approx. weight 2.1 g

Figure 2

Transparent plastic miniature package
6 pins

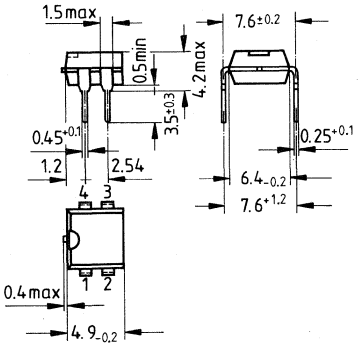


Approx. weight 0.1 g

Figure 3

Package Outlines

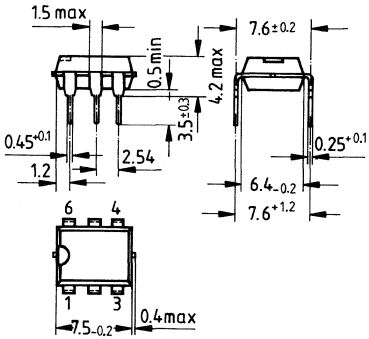
Plastic plug-in package 20 A 4 DIN 41866
4 pins, DIP



Approx. weight 0.5 g

Figure 4

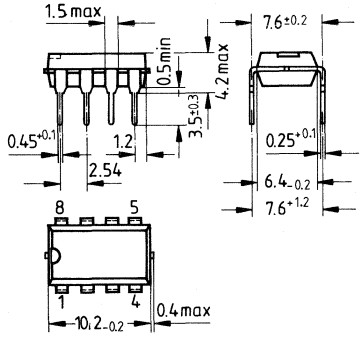
Plastic plug-in package 20 A 6 DIN 41866
6 pins, DIP



Approx. weight 0.7 g

Figure 5

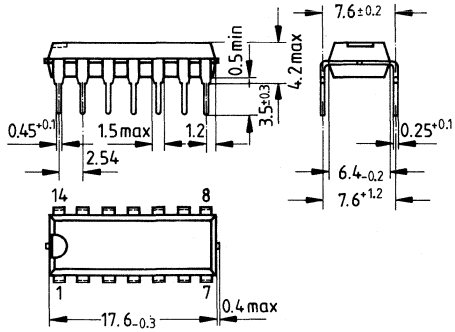
Plastic plug-in package 20 A 8 DIN 41866
8 pins, DIP



Approx. weight 0.7 g

Figure 6

Plastic plug-in package 20 A 14 DIN 41866
14 pins, DIP

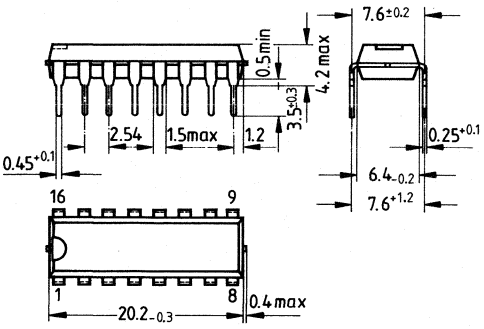


Approx. weight 1.1 g

Figure 7

Package Outlines

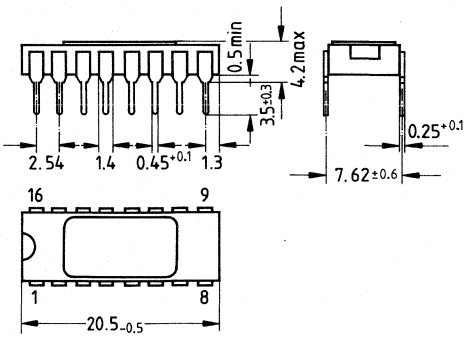
Plastic plug-in package 20 A 16 DIN 41866
16 pins, DIP



Approx. weight 1.2 g

Figure 8

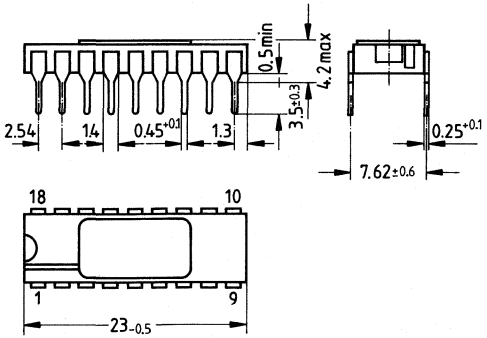
Ceramic package
16 pins, DIC



Approx. weight 1.4 g

Figure 9

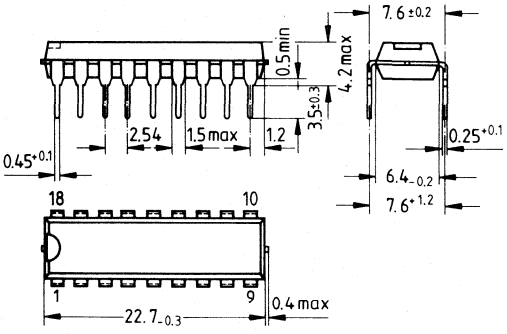
Ceramic package
18 pins, DIC



Approx. weight 2.7 g

Figure 10

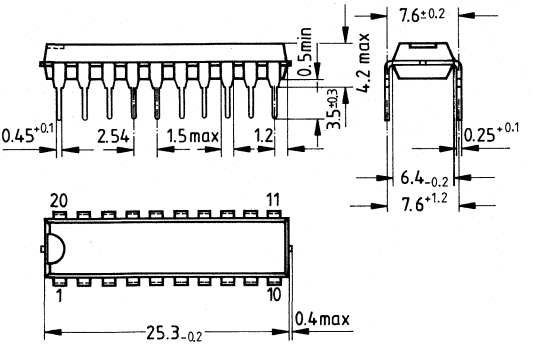
Plastic plug-in package 20 A 18 DIN 41866
18 pins, DIP



Approx. weight 1.3 g

Figure 11

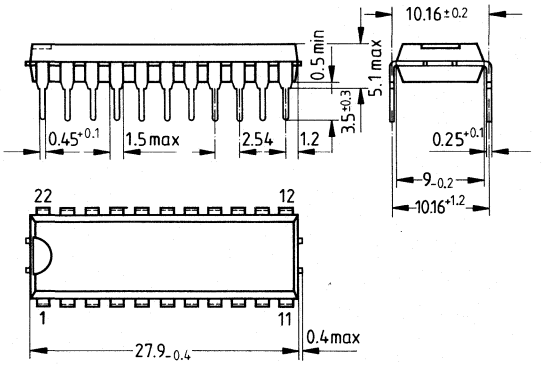
Plastic plug-in package 20 A 20 DIN 41866
20 pins, DIP



Approx. weight 1.5 g

Figure 12

Plastic plug-in package 20 D 22 DIN 41866
22 pins, DIP

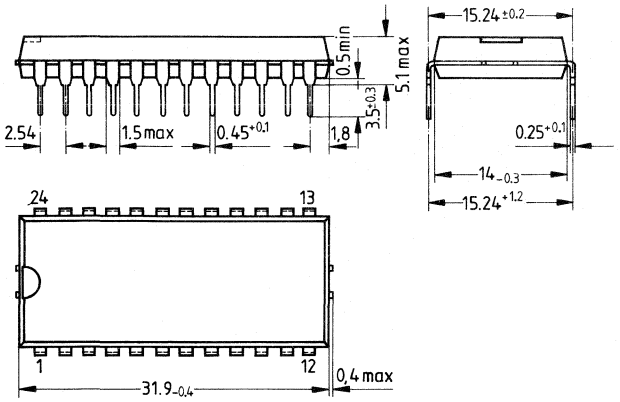


Approx. weight 2.1 g

Figure 13

Package Outlines

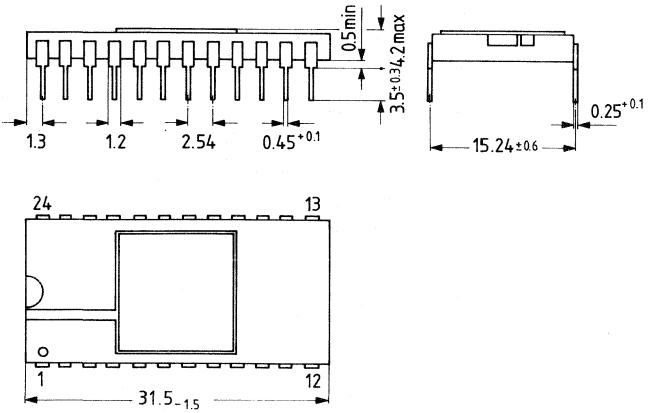
Plastic plug-in package 20 B 24 DIN 41866
24 pins, DIP



Approx. weight 2.5 g

Figure 14

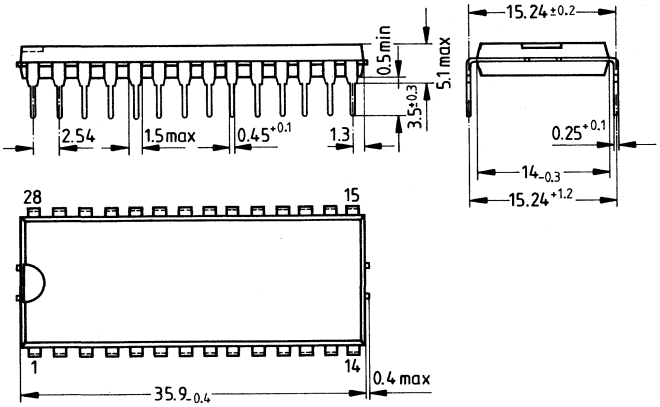
Ceramic package
24 pins, DIC



Approx. weight 3 g

Figure 15

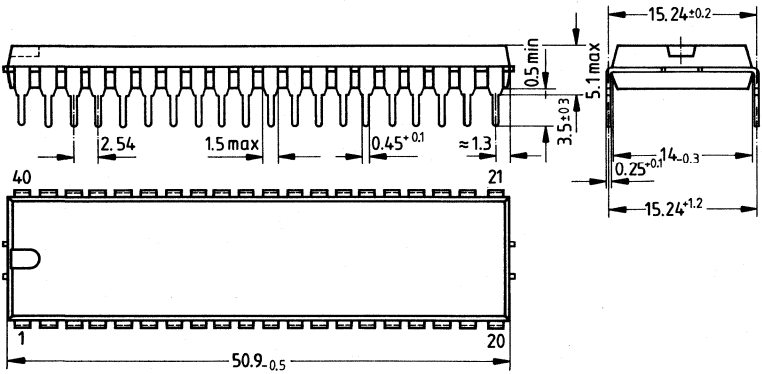
Plastic plug-in package 20 B 28 DIN 41866
28 pins, DIP



Approx. weight 3 g

Figure 16

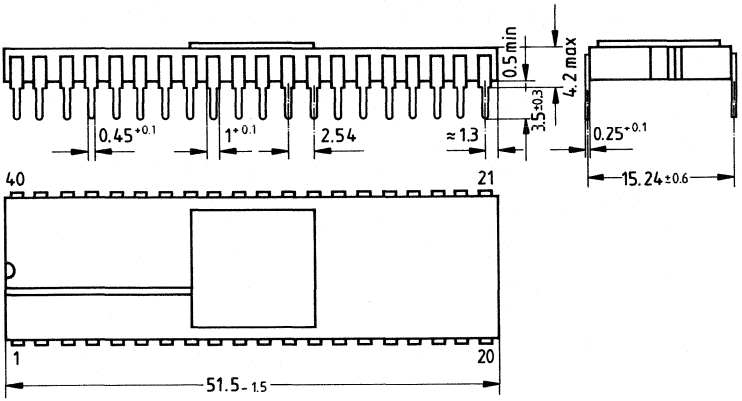
Plastic plug-in package 20 B 40 DIN 41866
40 pins, DIP



Approx. weight 5.9 g

Figure 17

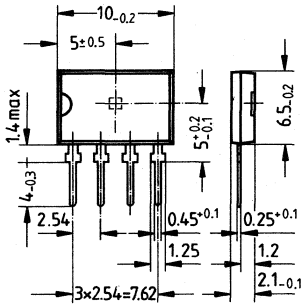
Ceramic package
40 pins, DIC



Approx. weight 6.8 g

Figure 18

Plastic flatpack

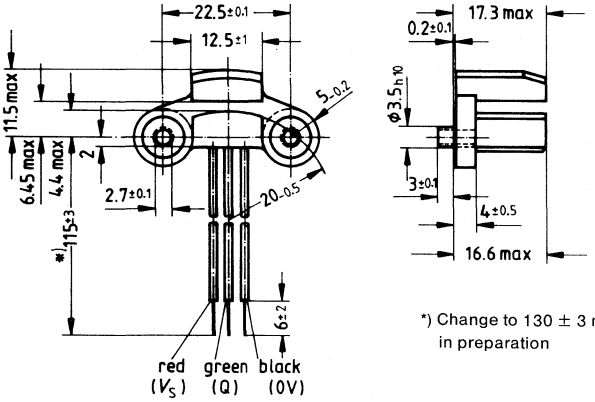


Approx. weight 0.5 g

Figure 19

Package Outlines

Special package

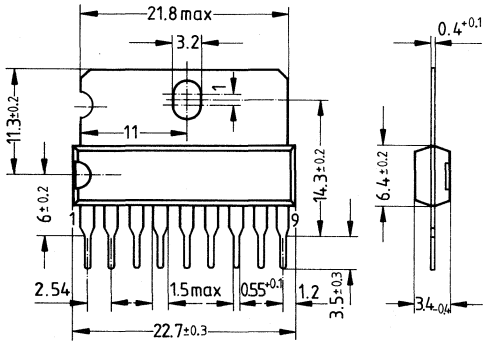


*) Change to 130 ± 3 mm in preparation

Approx. weight 8.5 g

Figure 20

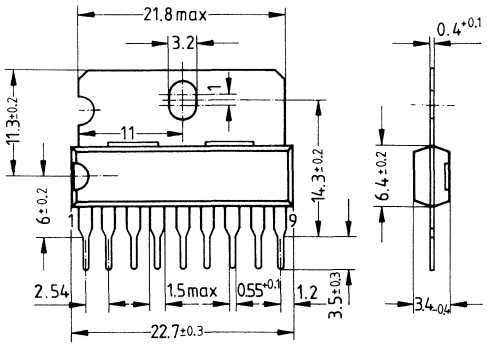
Plastic power package, with cooling fin and 9 pins, SIP



Approx. weight 1.9 g

Figure 21

Plastic power package, with cooling fin and 9 pins, SIP

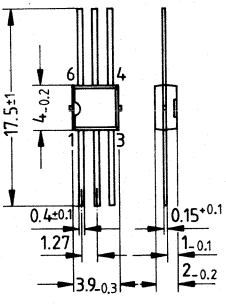


Approx. weight 1.9 g

Figure 22

Package Outlines

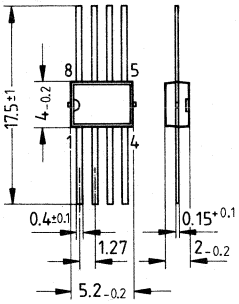
Miniature plastic package
6 pins



Approx. weight 0.1 g

Figure 23

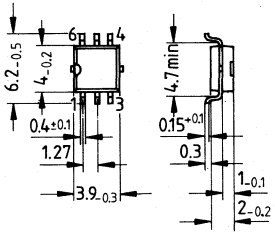
Miniature plastic package
8 pins



Approx. weight 0.15 g

Figure 24

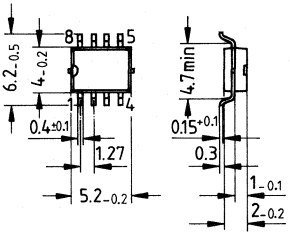
Miniature plastic package (G)
6 pins (similar to SO 6)



Approx. weight 0.1 g

Figure 25

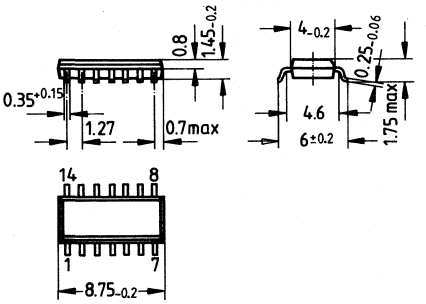
Miniature plastic package (G)
8 pins (similar to SO 8)



Approx. weight 0.15 g

Figure 26

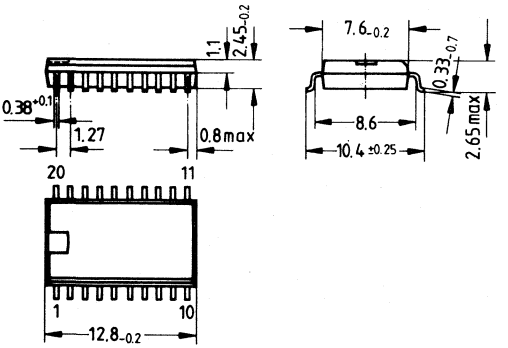
Miniature plastic package (G)
14 pins (SO 14)



Approx. weight 0.13 g

Figure 27

Miniature plastic package (G)
20 pins (SO 20 L)



Approx. weight 0.6 g

Figure 28

MICROPACK

Dimensions of perforation in acc. with DIN 15851, sheet 2

TCA 205 K

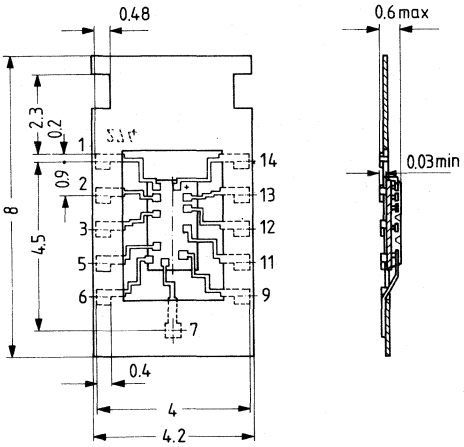


Figure 29

TCA 955 K

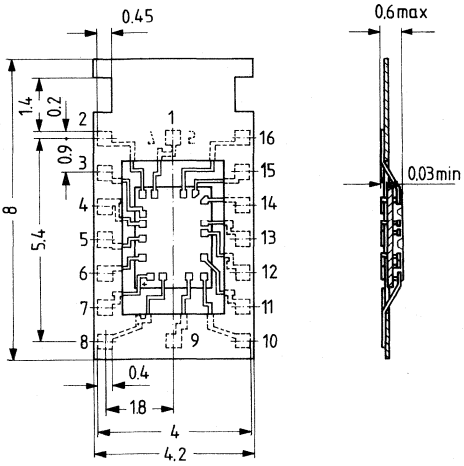


Figure 30

SAS 231 L

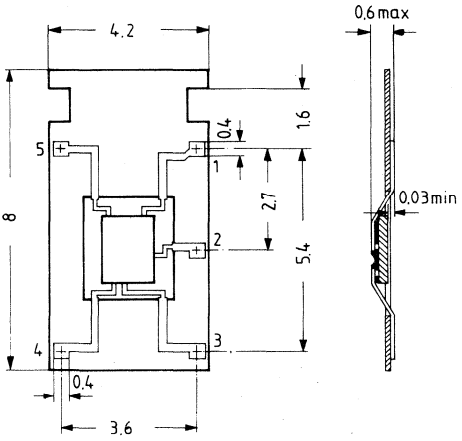
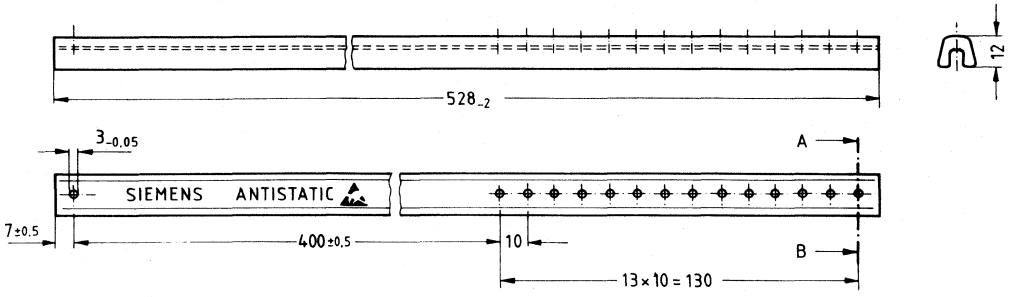
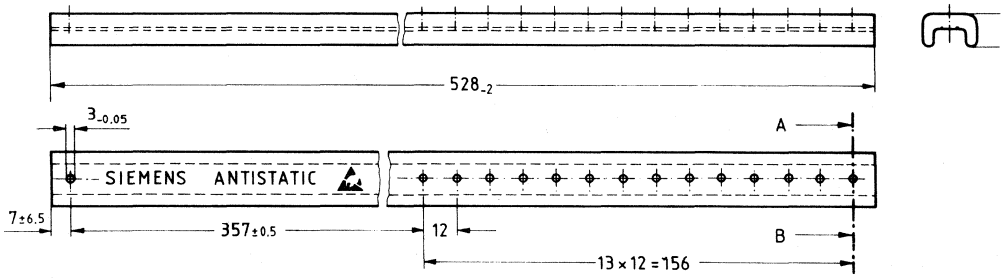


Figure 31

Package Outlines

Packaging tubes





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Comparators, Threshold Switches

ICs for Switched-Mode Power Supplies, Control ICs

Driver and Interface Circuits, Driver Stages, Level Converters, LED Display Drivers, Transistor Arrays

Control ICs for Thyristors and Triacs

A/D Converters

Timer ICs

Audible Signal ICs

Remote Control Systems

ICs for Radiotelephone Apparatus

DC Motor Drivers

ICs for Sensors, Proximity Switches, Hall-Effect Devices, Light Sensors

Nonvolatile Memories

Miscellaneous ICs

Package Outlines

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